

Multi-channel pulse counter based on the Altera field programmable gate array

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Currently active work on preparation of JUNO reactor neutrino experiment in China is underway. The primary goal of the experiment is the determination of neutrino mass hierarchy. Alongside with that the precision of some other neutrino mixing parameters can be improved. In order to reach these ambitious goals the detector of the experiment is supposed to have unprecedented resolution on the incident particles energy (3%/MeV). It places high demands on the photomultiplier tubes (PMT) efficiency and the properties of the scintillator. PMTs are being thoroughly examined and tested. They must have high degree of uniformity of gain and photon detection efficiency along the photocathode surface. Besides that this experiment is supposed to be ongoing at least for twenty years after its beginning. When the experiment starts there will be no possibility to replace non-working PMTs. Concerning this the long-term PMT stability tests come to play. Multi-channel pulse counters are required to carry out such tests. The operation of such counters will be implemented on the basis of Intel (Altera) field programmable gate arrays. The report will describe the schematic diagram of the device as well as the implementation of basic functional units by means of Verilog hardware description language.

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