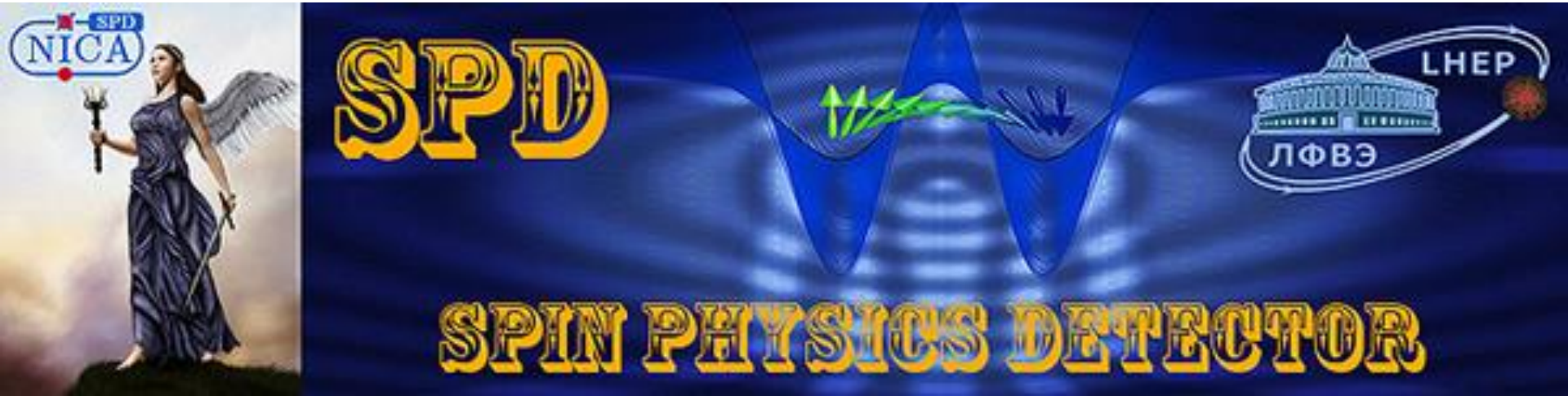
SPD at NICA 2019

4-8 June 2019, Dubna, Russia

Zero degree calorimeter readout

Igor Alekseev (ITEP, Moscow)



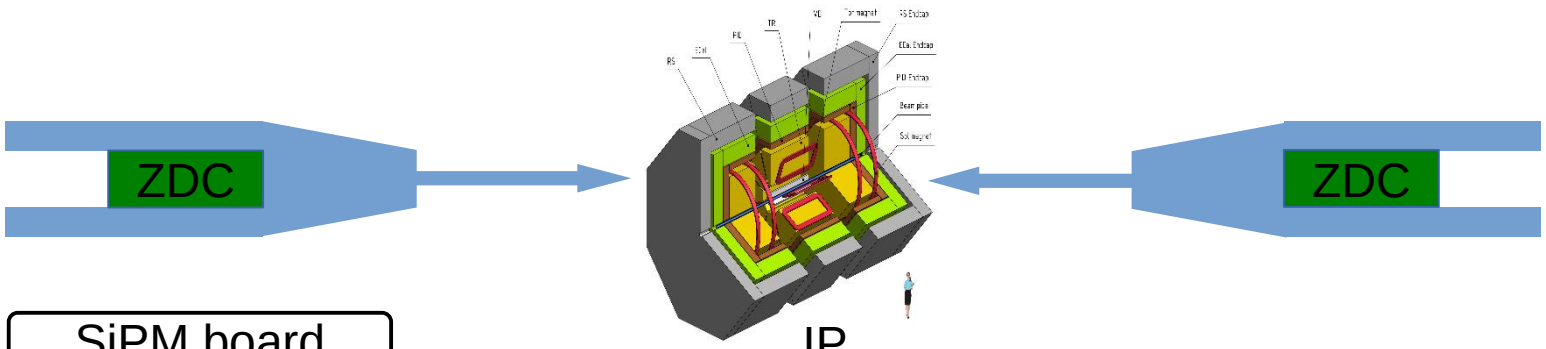
Main task of the Zero degree calorimeters in the SPD experiment is to tag neutrons going at very small angles

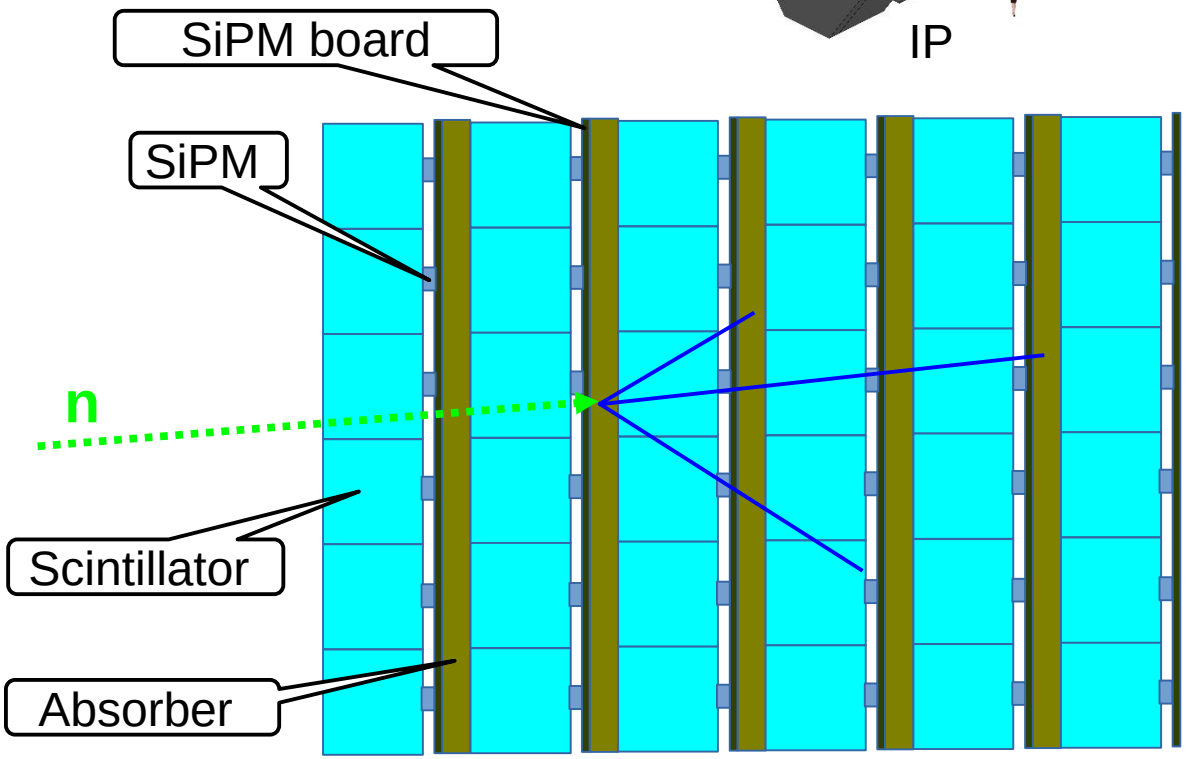
- Physics applications – talk by Stepan Shimanskiy yesterday
- Luminocity monitor
- Local polarimetry with neutrons – utilized at Phenix at RHIC

Requirements:

- Good neutron registration efficiency
- Measure neutron energy in the range 1-10 GeV with maximum precision
- Measure neutron entry point with a precision of a cm
- Fit into the selected site

Conceptual design



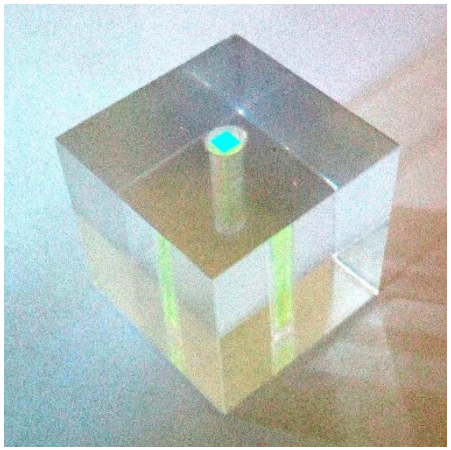


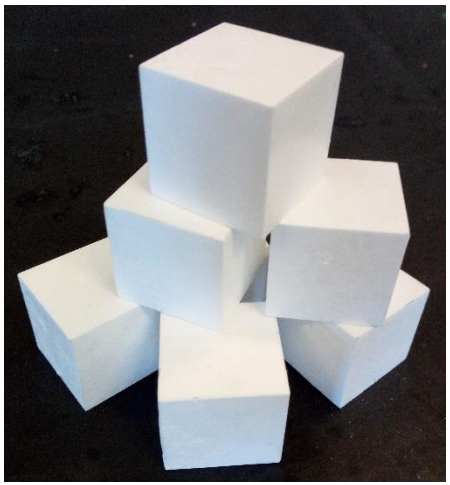
- Sampling calorimeter with fine segmentation
- SiPM light readout
- About 1500 channels
- Optimization based on MC and measurements with prototype is required
- Readout system based on electronics designed for the DANSS neutrino experiment at Kalininskaya NPP

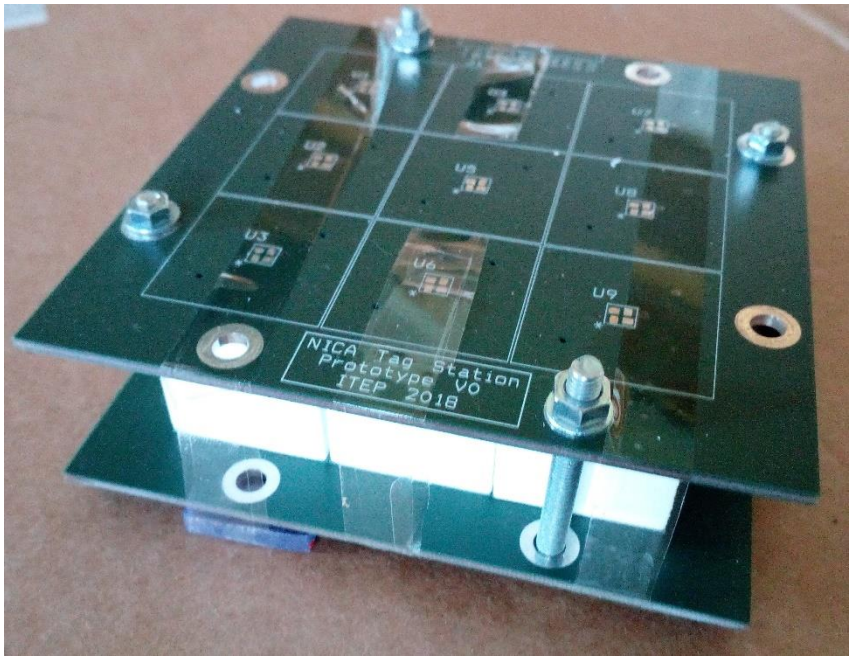
The first prototype

- 3x3x6 scintillator cubes 3x3x3 cm^3 each
- 3X3 mm^2 SENSL 30050 SiPM (2668 pixels)
- Two types of light collection:

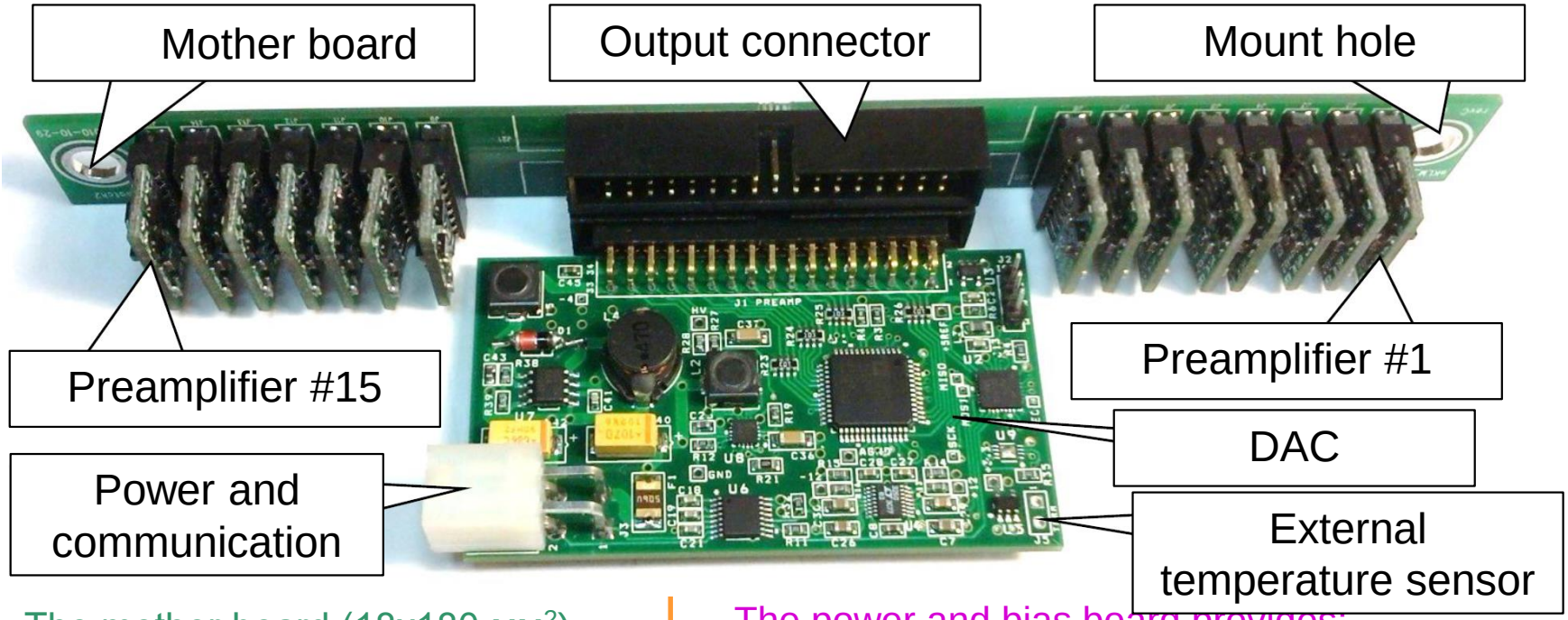
- Polished cubes with wavelength shifting fiber – more light, but could be a problem with SiPM dynamic range and more complex mechanical design
- Whitened cubes with direct readout – less light, but significantly more simple mechanics







SiPM bias and preamplifiers



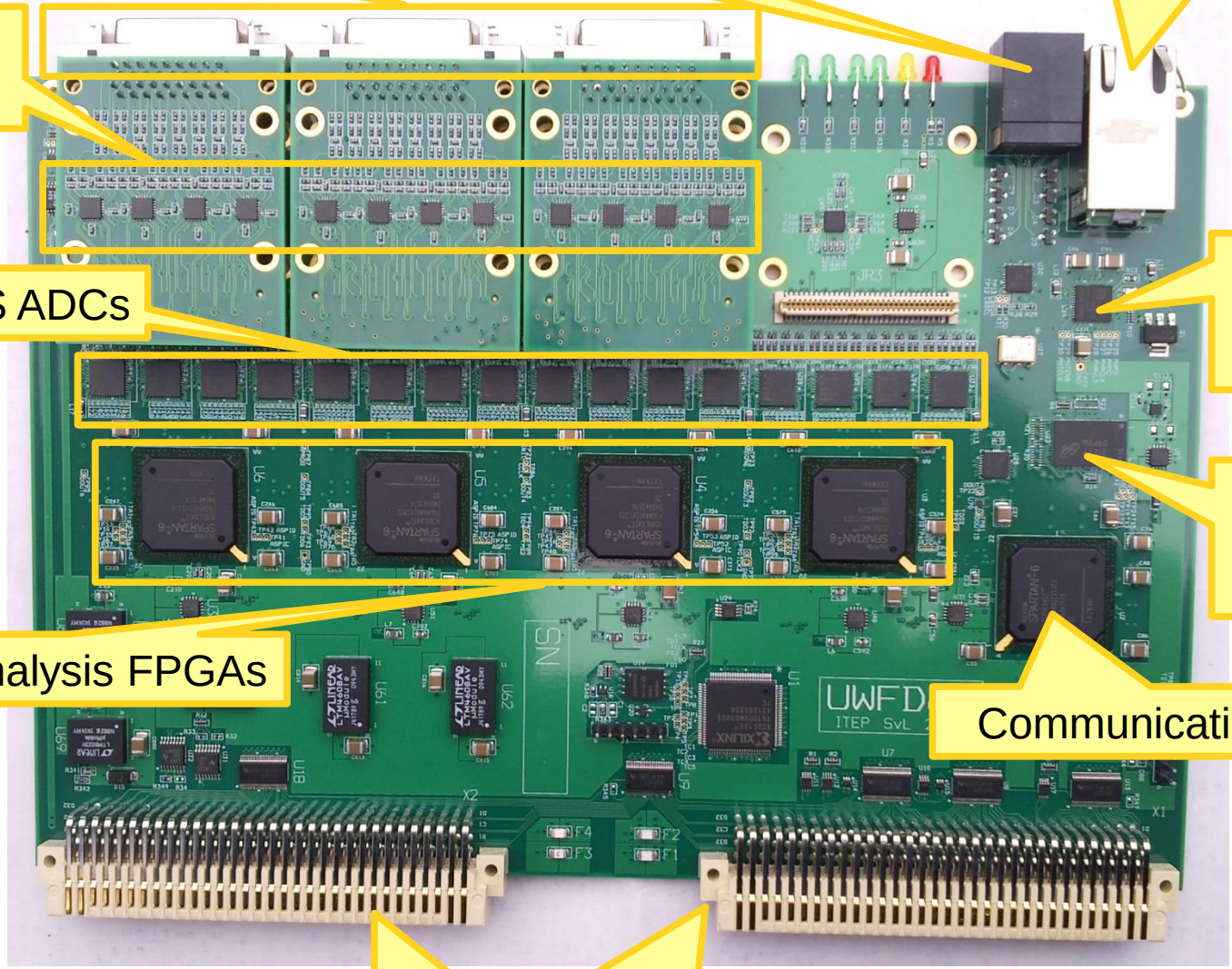
The mother board (18x180 мм^2) hosts:

- 15 preamplifiers
- Power and bias board
- Output connector

The power and bias board provides:

- Power for preamplifiers and its control
- Common cathode voltage for SiPMs, its precise setting and measurement in the range 10-65 V
- Setting and monitoring of the individual anode voltages in the range ±10V
- Readout of common bias current
- Readout of the external temperature sensor as well as onboard CPU and DAC temperatures

64-channel WFD

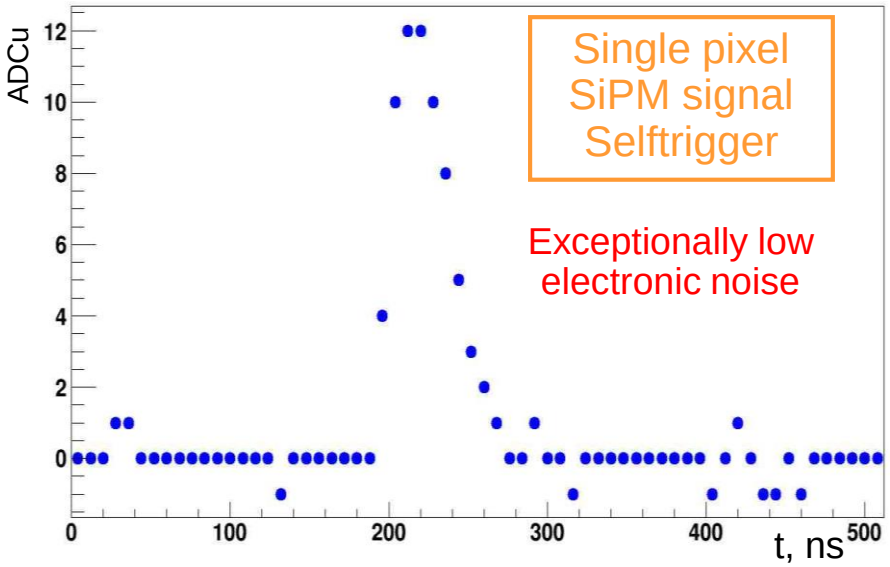


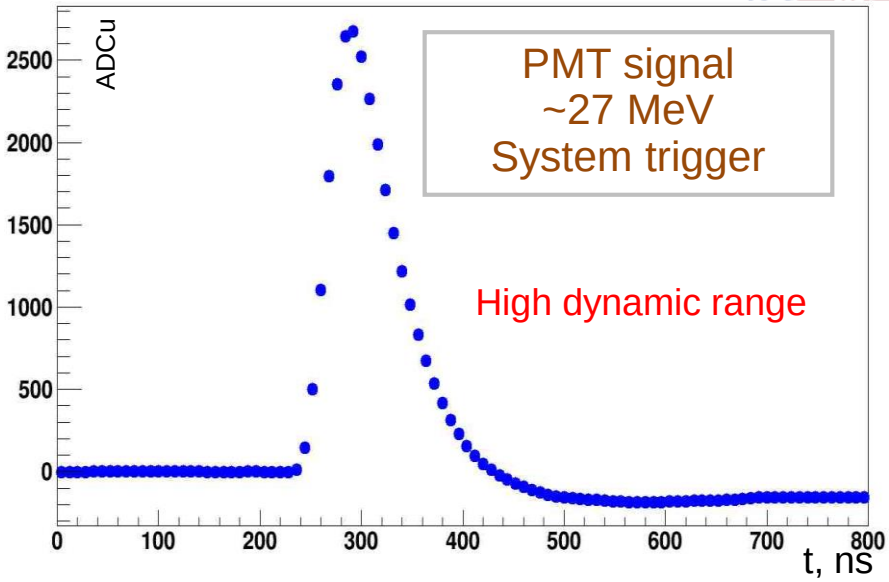
64-channel WFD

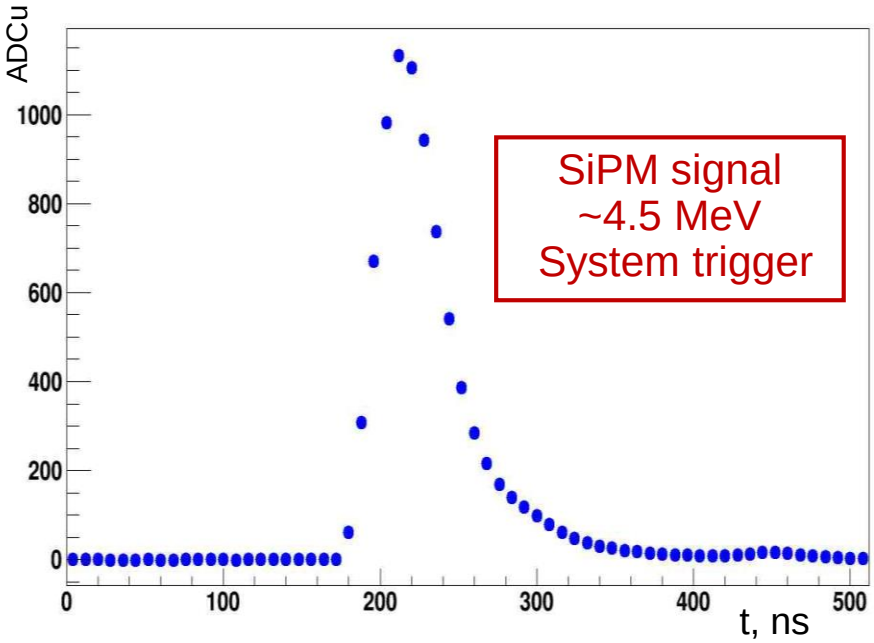
- 64 channels of 125 MSPS 12 bit flash ADCs
- VME 64x standard 6U single slot width board
- 64-bit block transfer support
- Xilinx Spartan-6 FPGAs for digital signal processing and communication
- 4 Gbit of SDRAM for data storage
- 1 Gbit Ethernet connection for faster readout
- Multitrigger and **triggerless** operation
- Base line subtraction and zero suppression for wave form storage
- Selftrigger with prescale for SiPM noise measurements
- Internal or **external** clock operation
- Deadtimeless operation
- Input amplifier board can be changed to get 32 channels at 250 MSPS or 16 channels at 500 MSPS
- Possible ADC chip replacement to get 14 bits

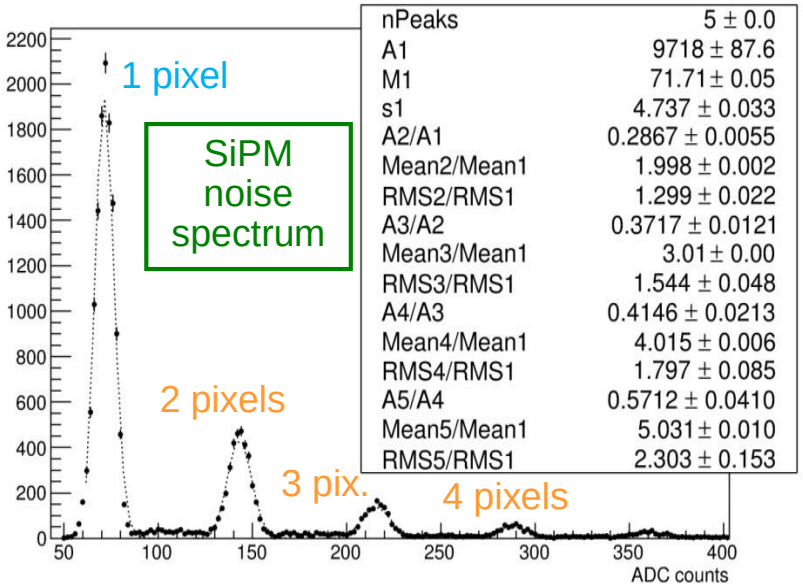
Instruments and Experimental Techniques, 2018, Vol. 61, No. 3, pp. 349–354.

Performance at DANSS









Future plans

- The first prototype assembly and tests
- Profound Monte-Carlo simulations of neutrons and gammas in the calorimeter
- Development of neutron reconstruction algorithms based on neural networks
- Optimization of the ZDC geometry
- Production of the second prototype
- Tests of the prototype with hadron beams