# Status of the TIGER ASIC tests

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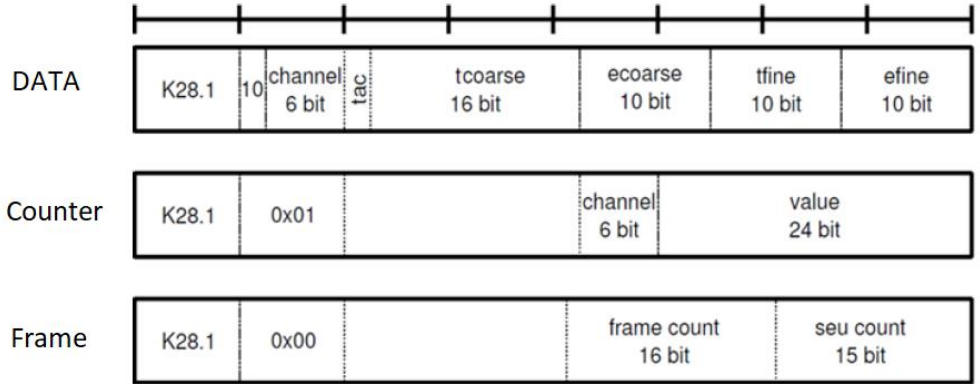
# Torino Integrated Gem Electronics Readout (TIGER)

## TIGER ASIC specifications

| Parameter | Value |
|---|---|
| Number of channels | 64 |
| Clock frequency | 160-200 MHz |
| Input capacitance | up to 100 pF |
| Input dynamic range | 2-50 fC |
| Front-end gain | 12 mV/fC |
| Energy branch ENC | <1500 $e^-$ |
| Time branch jitter | <5 ns |
| Time measurement | Leading edge discriminator + analogue TDC |
| TDC time binning | 30-50 ps |
| Charge measurement | Peak sampling + ADC or Time-over-Threshold |
| Maximum event rate | 60 kHz/channel |
| Readout Mode | Trigger-less |
| TX links | 4, LVDS |
| Max. output data rate | 1.6 Gb/s (200 MHz, DDR) |
| Configuration | 10 MHz SPI-like |
| Power consumption | 10-12 mW/channel |
| Process | CMOS 110 nm |

## TIGER Data Format

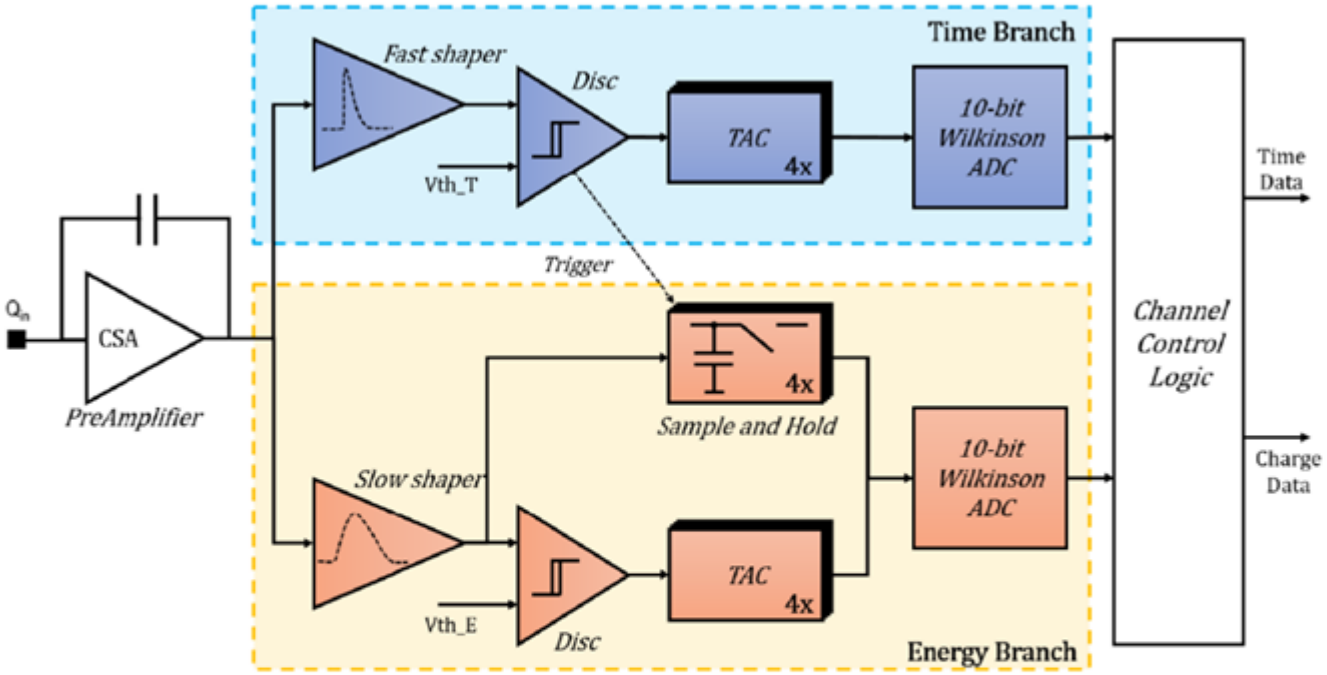



## TIGER Event word content

| Bits | Parameter | Description |
|---|---|---|
| 63:56 | K28.1 | Start of the 64-bit word identifier |
| 55:54 | 0b10 | Event word identifier |
| 53:48 | Channel_id | Channel identifier |
| 47:46 | TAC_id | TAC index |
| 45:30 | Tcoarse | Leading edge coarse time tag |
| 29:20 | Ecoarse | Falling edge coarse time tag (ToT mode)<br>Sampling stop time tag (S&H mode) |
| 19:10 | Tfine | T-branch TDC fine time measurement |
| 9:0 | Efine | E-branch TDC fine time measurement (ToT mode)<br>ADC charge value (S&H mode) |

Fabio Cossio - A mixed-signal ASIC for time and charge measurements with GEM detectors; Doctoral Dissertations, 2019

# TDC and Energy branches



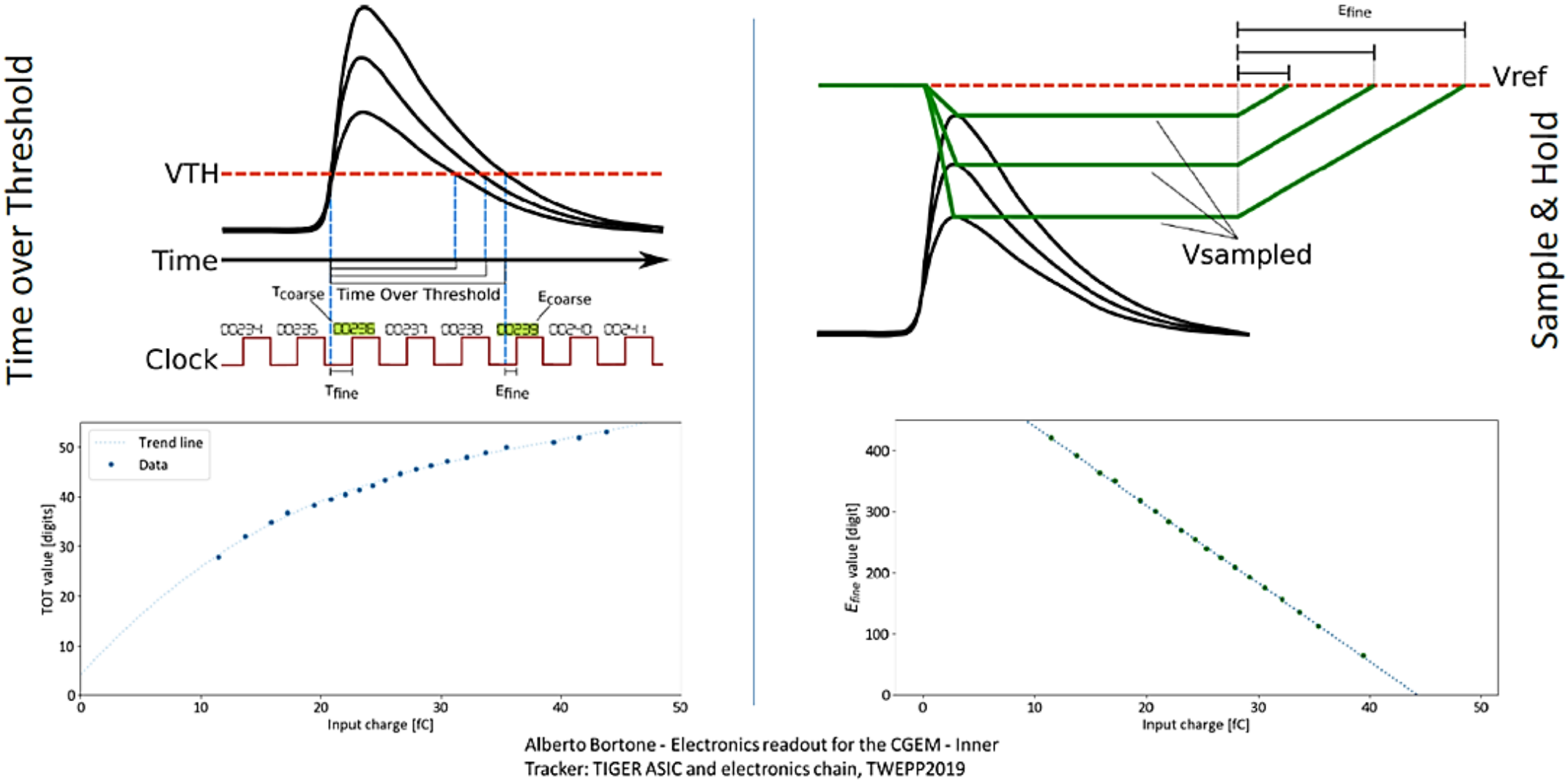

Time branch : 60 ns peaking time for low jitter timing measurement

Energy branch : 170 ns peaking time for signal to noise ratio optimization

- **Front-End**: charge sensitive amplifier + 2 shapers (Time & Energy), single or double threshold readout
- **Timestamp** on the rising edge of the fast branch
- **Charge** measurement with Time-over-Threshold or S/H circuit:
  - **ToT**: time stamp on rising/falling edge (sub 50 ps binning of quad-buffered TDC)
  - **S/H**: slow shaper output sampled and digitized with a 10 bit Wilkinson ADC

Maxim Alexeev - TIGER: A front-end ASIC for timing and energy measurements with radiation detectors; 4th Collaboration Meeting of the BM@N Experiment at the NICA Facility, 14.10.19

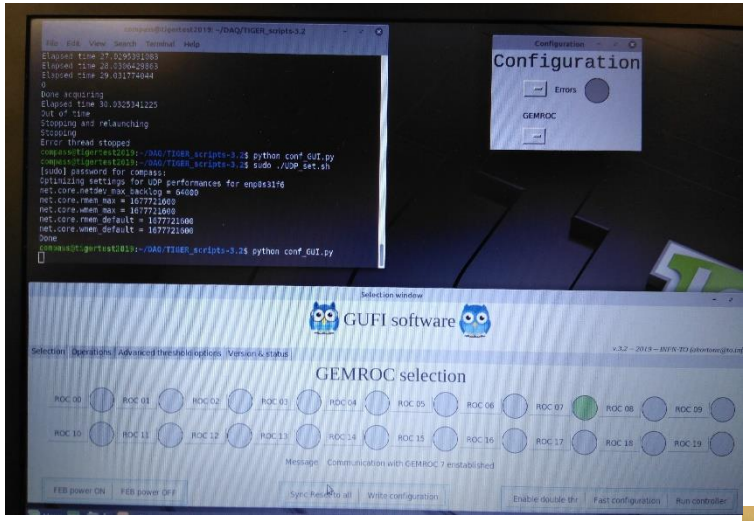
# Charge measurement

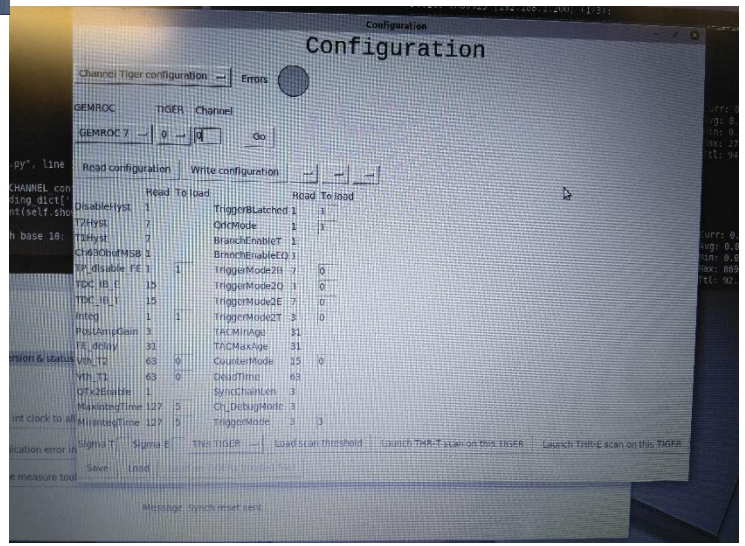



Alberto Bortone - Electronics readout for the CGEM - Inner Tracker: TIGER ASIC and electronics chain, TWEPP2019

Maxim Alexeev - TIGER: A front-end ASIC for timing and energy measurements with radiation detectors; 4th Collaboration Meeting of the BM@N Experiment at the NICA Facility, 14.10.19

# TIGER configuration

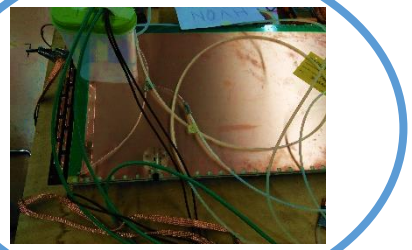



How to configure the TIGER?

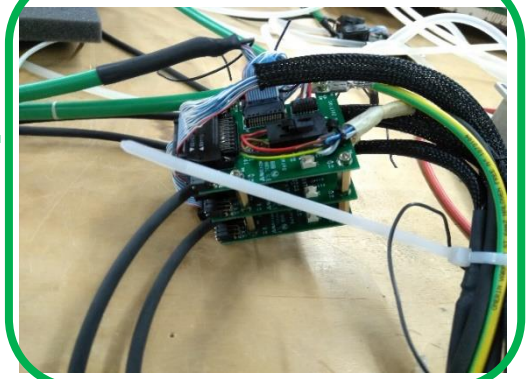
1. Open Terminal and run *sudo ./UDP_set.h* for network driver settings;
2. Run *python conf_GUI.py* to run GUI;
3. In Configuration window choose GEMROC. If the lamp is green, the network connection is OK;
4. In Operation Tab click *Set init clk to all* to run external clock to FPGA;
5. Click *Sync reset to all;*
6. Then *FEB power on;*
7. Tab Operation -> *Write configuration* (click twice) to configure default global and local registers;
8. *Sync reset to all*;
9. *Open configuration error interface -> GEMROC #_ error -> Acquire errors since last reset.* There should be 0 errors on working TIGER chips;
10. *Launch TDC scan on all GEMROCKs*;
11. *Load TD from TD delay file;*
12. *Sync reset to all*;
13. *Acquire errors since last reset.* Should be 0 errors.
14. *Configuration -> channel TIGER configuration.* Choose GEMROC#, TIGER#, channel 0, run *GO.* Then *Read configuration.*
15. *Launch Thr-T scan on this TIGER;*
16. *Launch Thr-E scan on this TIGER;*
17. Do these scans for all needed TIGERs;
18. In configuration window choose channels or *All channels*;
19. Run *Read configuration;*
20. Set *trigger mode* equals 0;
21. Run *Write configuration;*
22. *Read configuration* to check written value;
23. Set *Sigma T_* and *Sigma E_*;
24. Click *Load scan threshold;*
25. Back to GUFI: *Operation tab-> Set trigger-less mode to all -> Sync reset to all*;
26. *Selection tab -> Run controller*;
27. Choose ROC, folder. Click *trigger-less file name* button.
28. *Run acquisition.*
29. Open terminal and run *python load_bin_folder.py* to decode data.

# Experimental setup

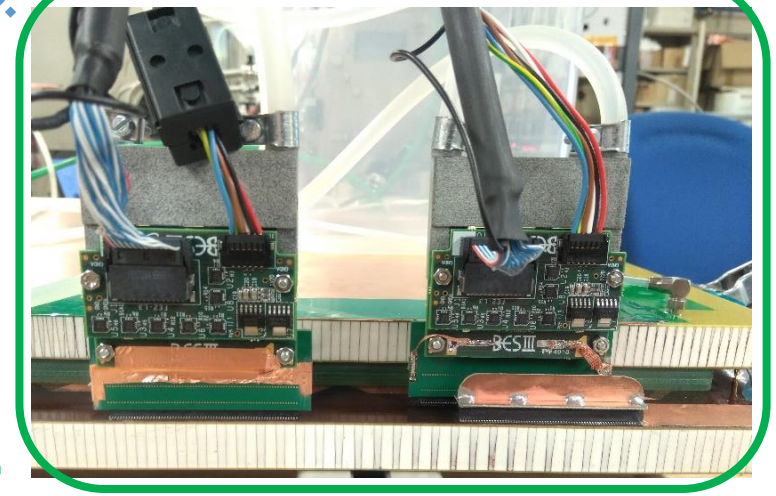


Cooling system +

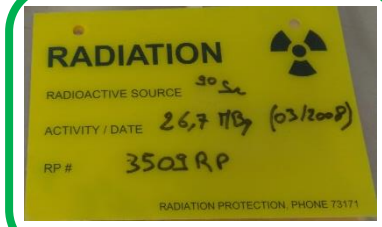
Front-End Board on GEM detector +

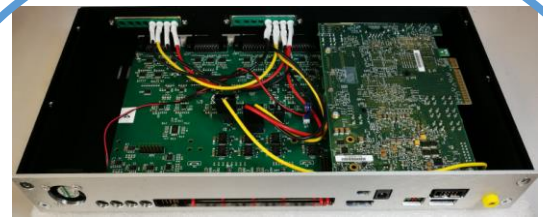


+ GEMROC module



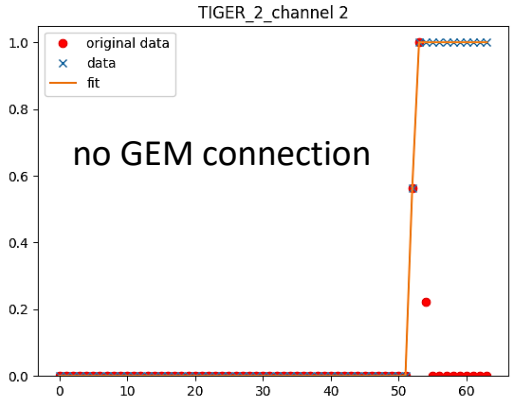
$^{90}Sr$ +

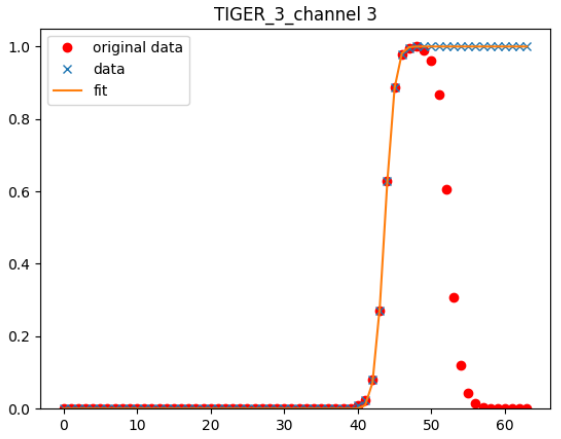


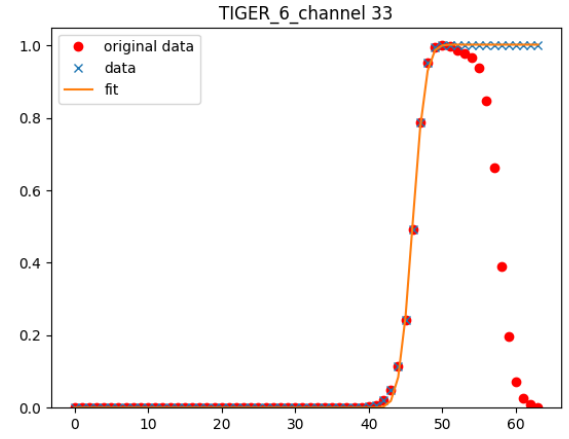



Fabio Cossio - A mixed-signal ASIC for time and charge measurements with GEM detectors; Doctoral Dissertations, 2019

# Input capacitance

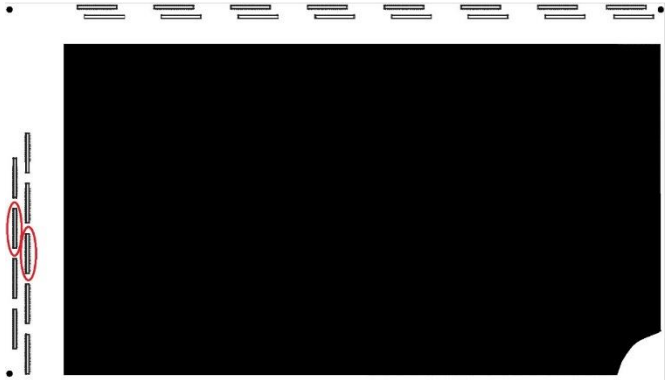


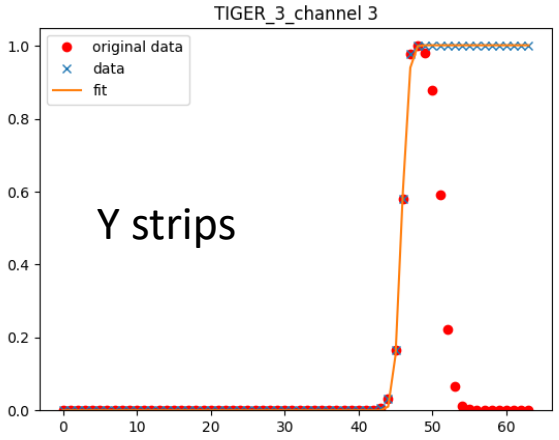



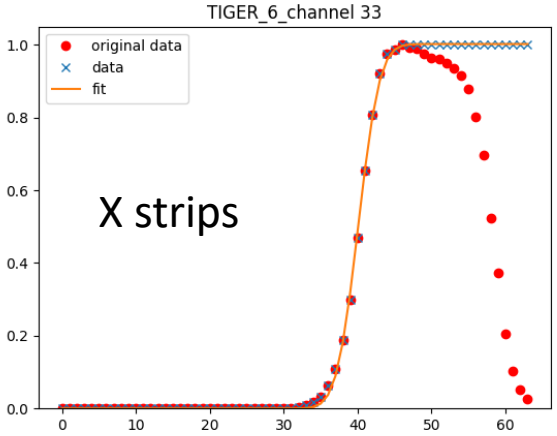




X (0˚) and Y (15˚) strips test run with TIGER

Hot Zone test run with TIGER





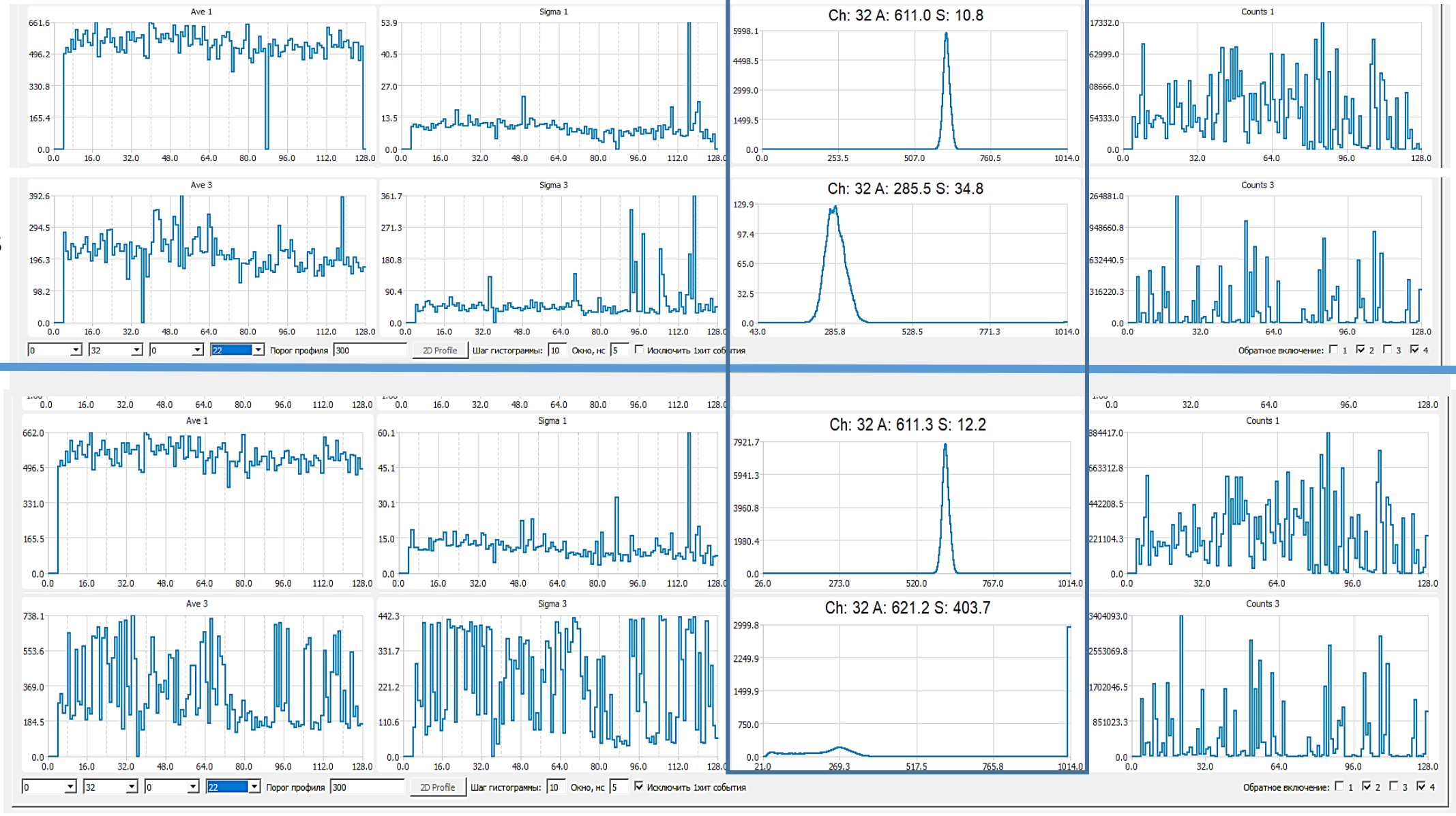
# X and Y strips RUN

$E_{fine}$

no $^{90}$Sr

Y strips

X strips

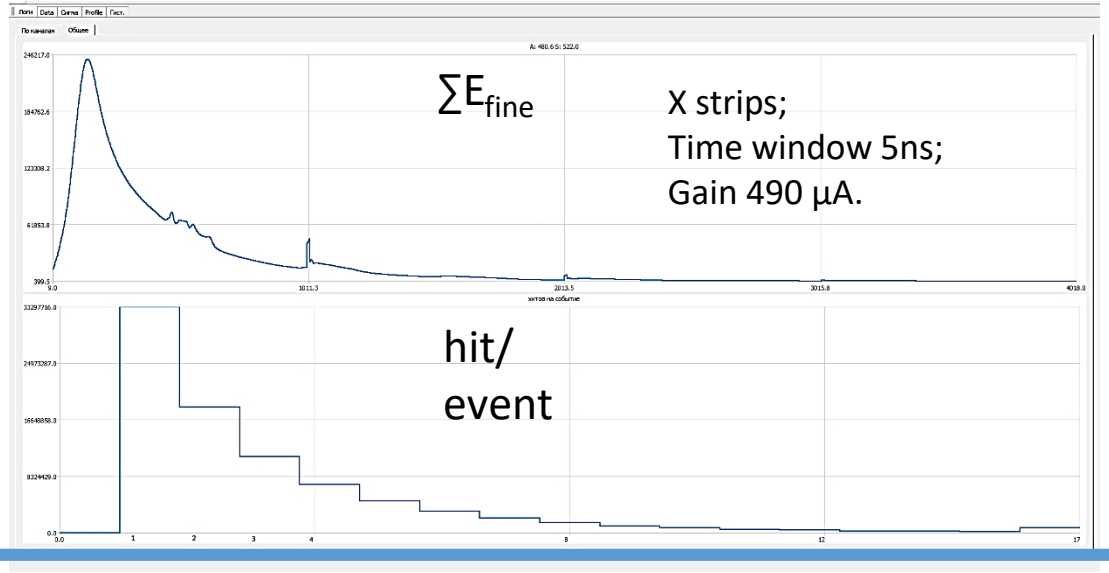



$^{90}$Sr

Y strips

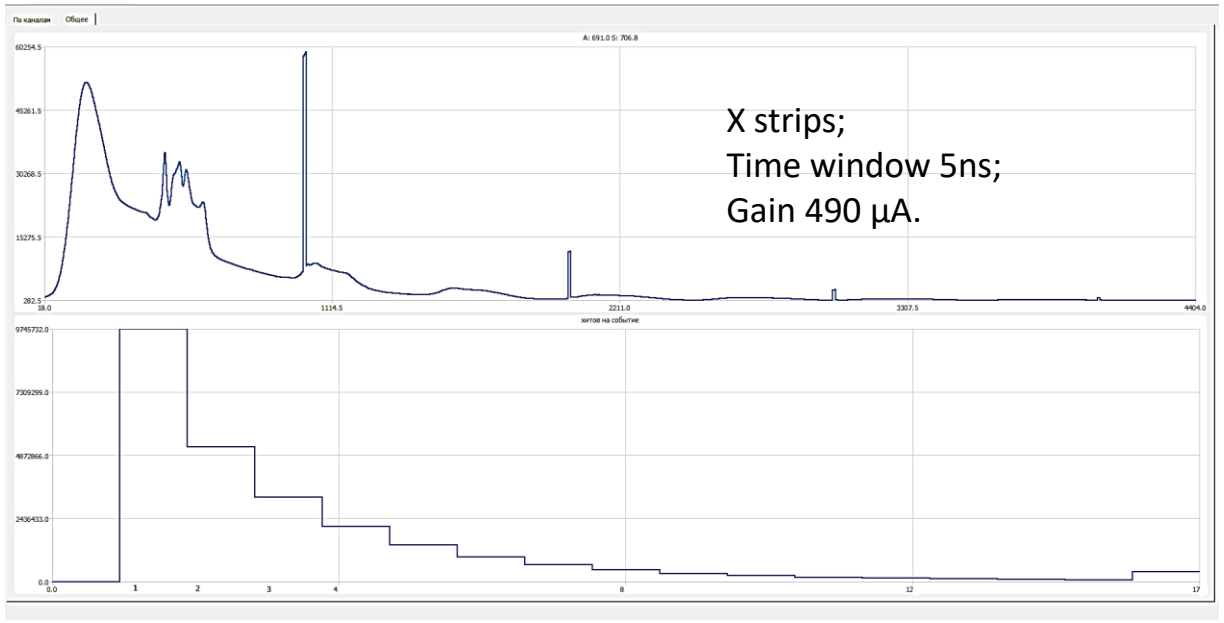
X strips

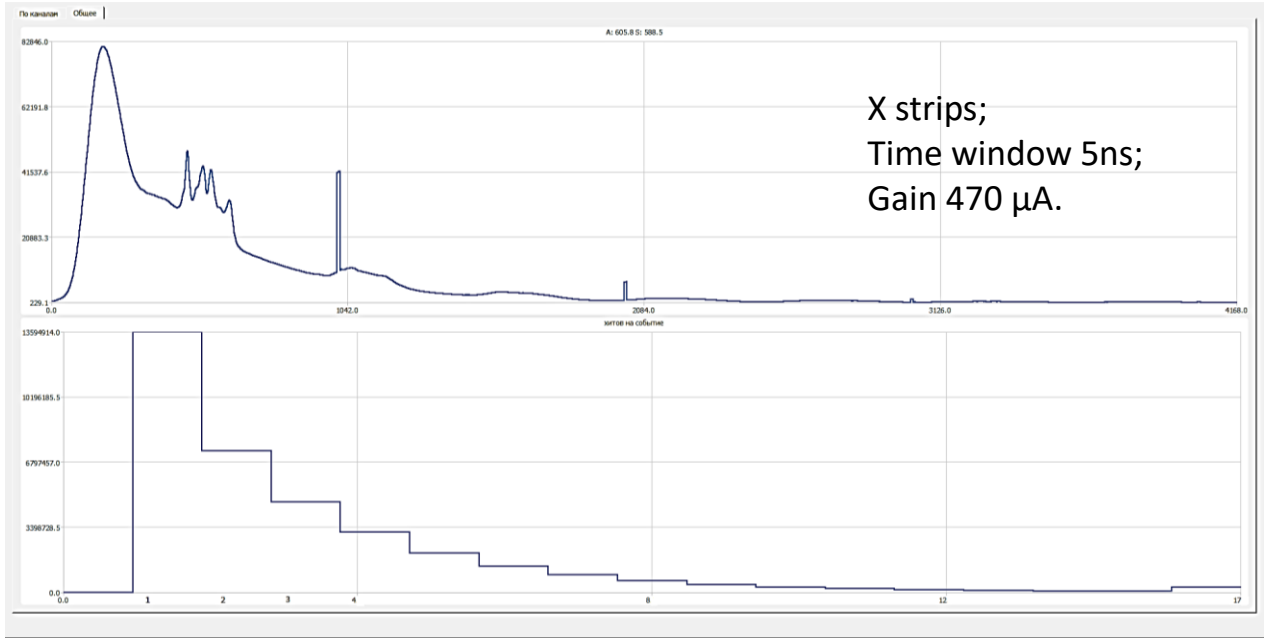
no $^{90}Sr$




Events inside the Time window

$^{90}Sr$



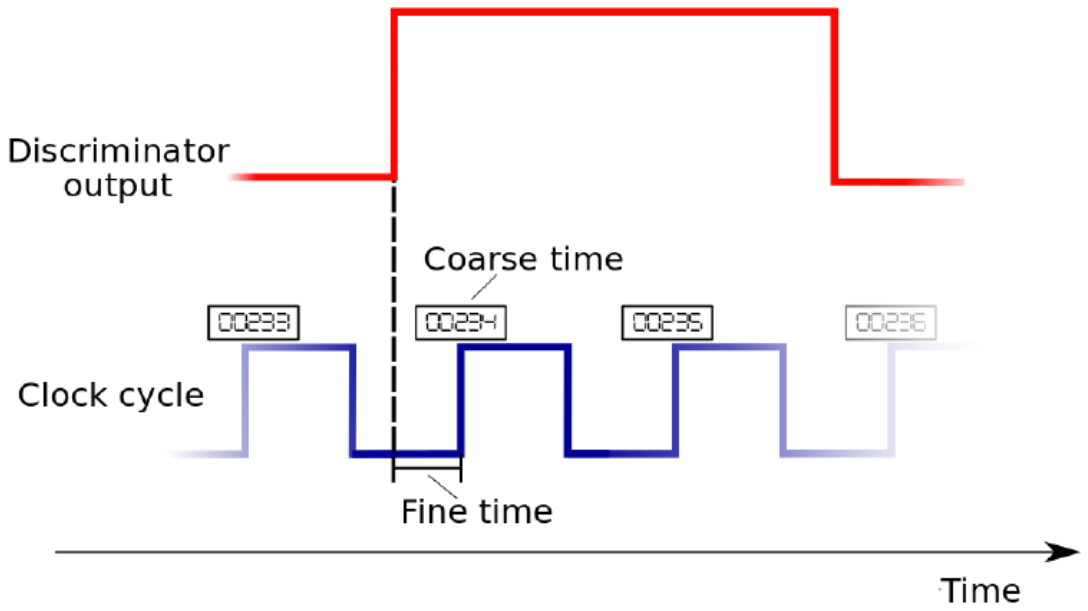
# Conclusions

- Now it is known about TIGER architecture, charge measurement and configuration;
- First run of TIGER FEE boards on GEM detector;
- Mean noise of the TIGER channel in 250 ADC digits is a question;
- GEMROC module and TIGER FEE boards will be in JINR in spring 2020.

# Plans

- Make TIGER FEE board for Silicon Strip Detector and test it with GEMROC module in 2020.

# Time measurement




## Three accuracy levels @160 MHz:

**Frame-word**

Clock counter cycles roll over

204.8 µs time resolution

**Coarse time**

Hit clock cycle (16 bit counter)

6.25 ns time resolution

**Fine time**

Time to the next clock cycle

50 ps binning

**Low-power analogue TDC** based on time interpolation

Interpolation factor 128 -> 50 ps time binning @160 MHz

Quad-buffered TACs for **event de-randomization**

$$T = \text{Coarse} \times 6.25\ \text{ns} - (\text{Fine} - \text{min}) \times \text{binning}$$

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