Forward Silicon Detectors

upgrade status

Bogdan Topko on behalf of Forward Silicon Detectors team

5th Collaboration Meeting of the BM@N Experiment at the NICA Facility,

21 April 2020

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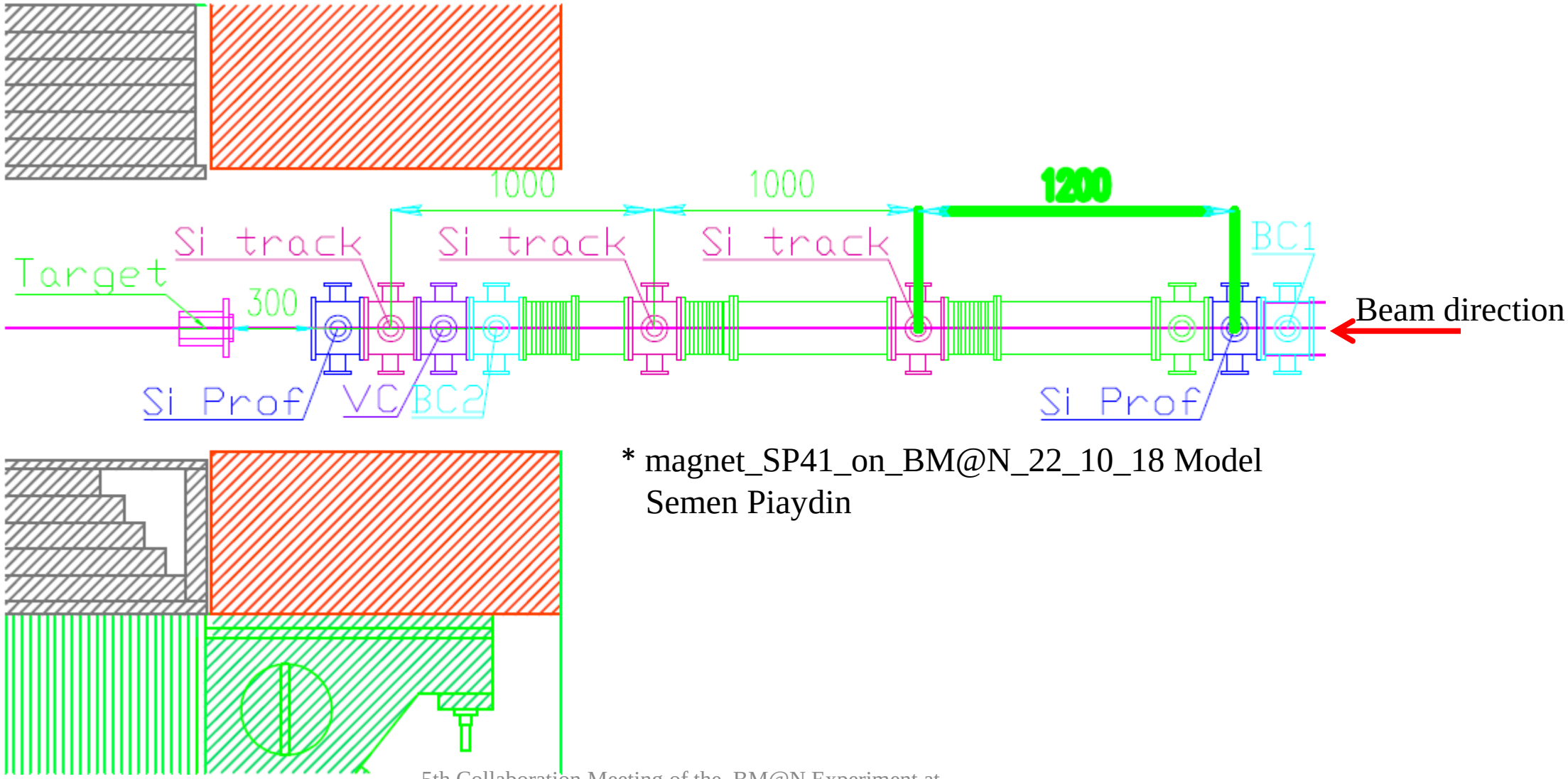
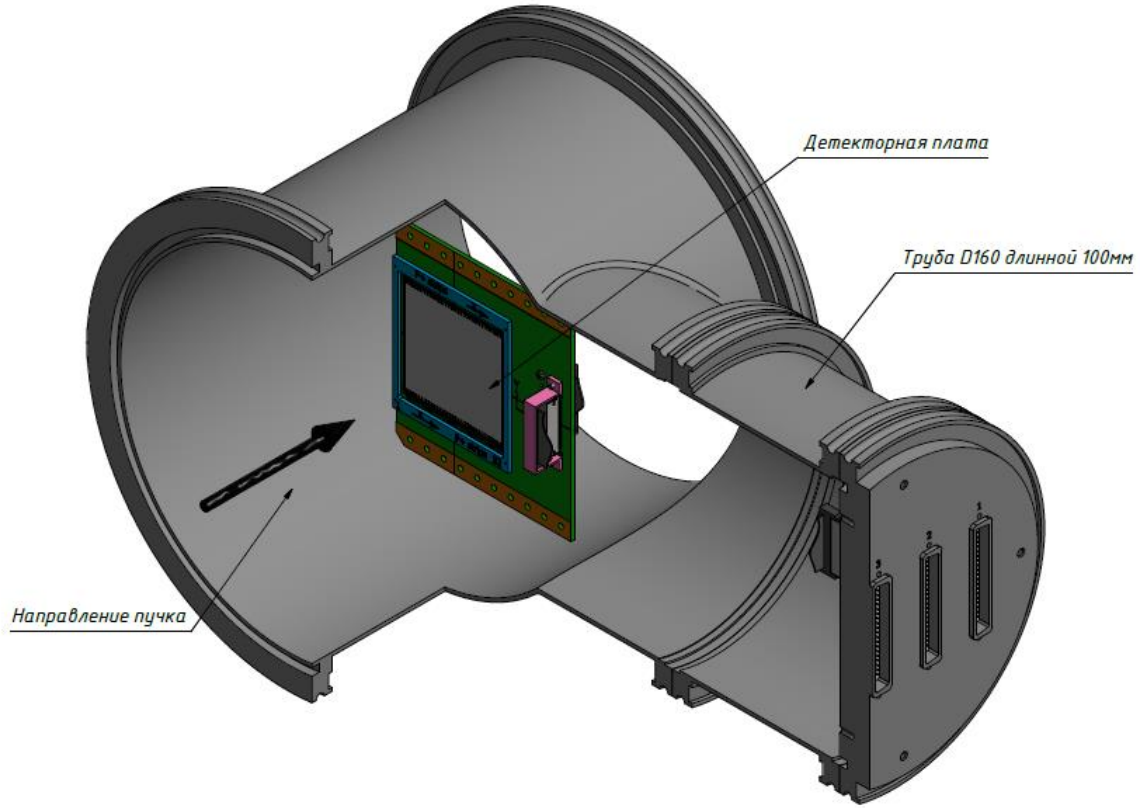
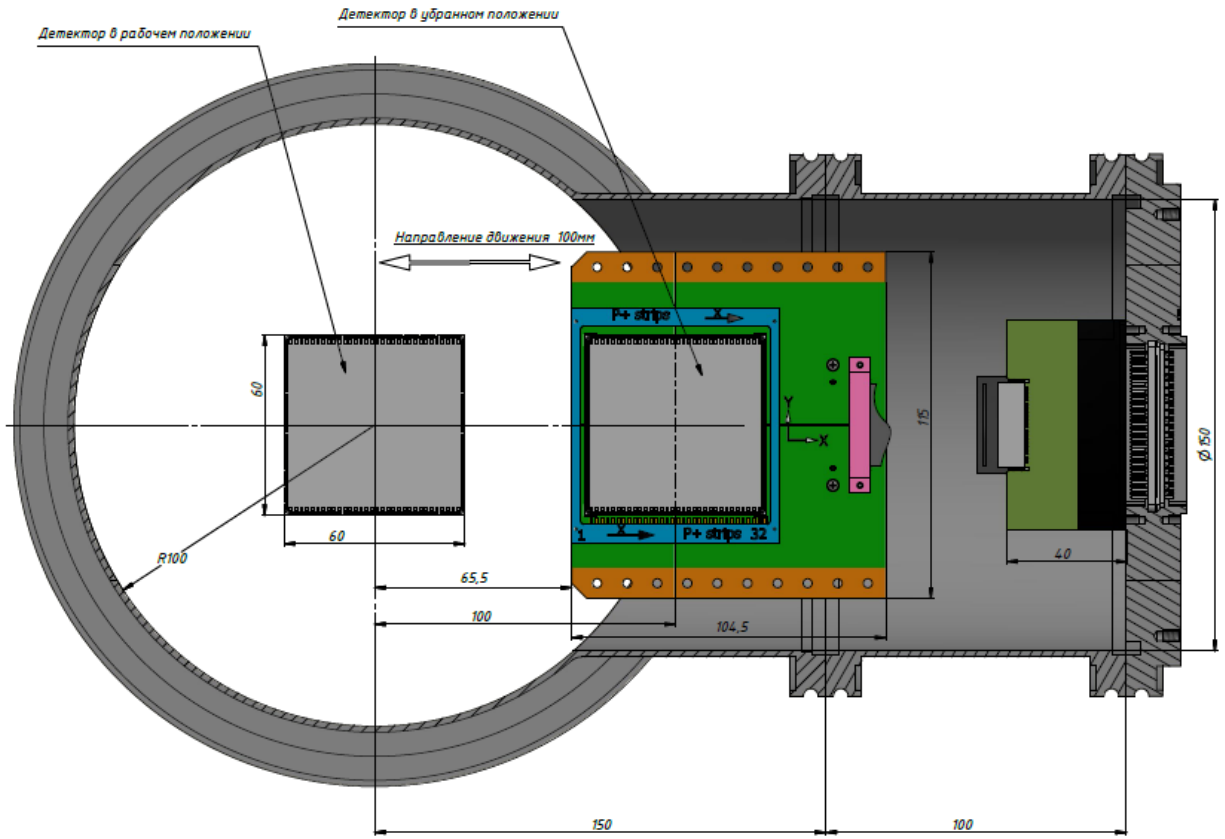
Detectors before the analyzing magnet



* magnet_SP41_on_BM@N_22_10_18 Model
Semen Piaydin

Detectors before the analyzing magnet

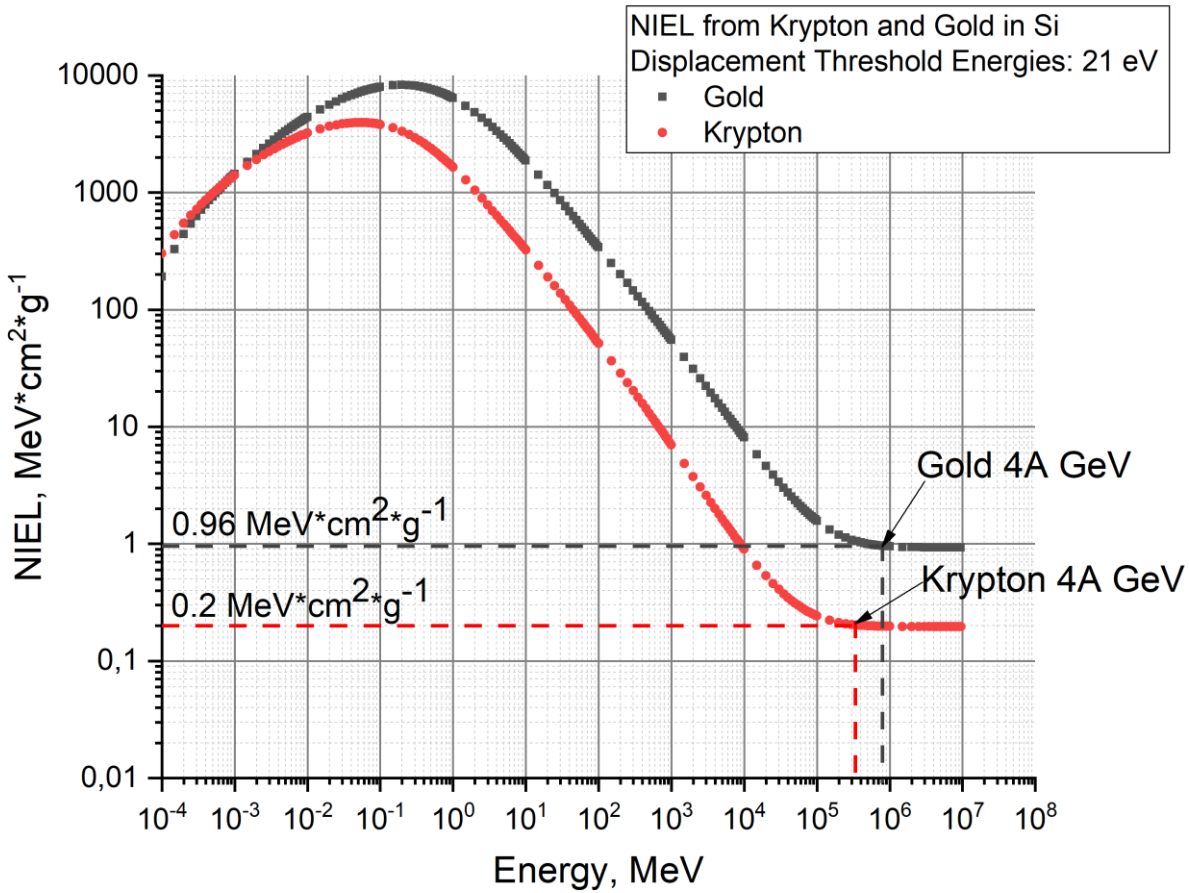




Beam profilometer (32x32 strips, thickness 175 um) inside beam-pipe

See Yu. Ivanova talk

Detectors before the analyzing magnet



SR-NIEL modeling results of NIEL in silicon detector for Kr^{36+} (red) and Au^{79+} (black) ions.

NIEL from 1 MeV neutron in Si (ASTM Standard E722-09):
NIELn=0.00204 MeV*cm^2* g^{-1}
Hardness factor of 4A GeV Gold: NIELgold/NIELn≈470;
Hardness factor of 4A GeV Krypton: NIELkrypton/NIELn≈98;

Radiation conditions in beam tracker positions:

Beam diameter: d=3 cm;
Flux of ^{197}Au: F=10^6 nucl./sec;
Time of irradiation: t=2 months;

$NIEL_{Au}(4\ GeV/nucl)$=$9.6107 \cdot 10^{-1}\ MeV \cdot cm^2 \cdot g^{-1}$;

$$\Phi_{1MeV} = \frac{NIEL_{Au}(4\ GeV/nucl)}{NIEL_{neutrons}(1\ MeV)} \cdot \Phi_{Au} =$$
$$= \frac{NIEL_{Au}(4\ GeV/nucl)}{NIEL_{neutrons}(1\ MeV)} \cdot \frac{4 \cdot F \cdot t}{\pi \cdot d^2} \approx 3.45 \cdot 10^{14}\ cm^{-2}$$

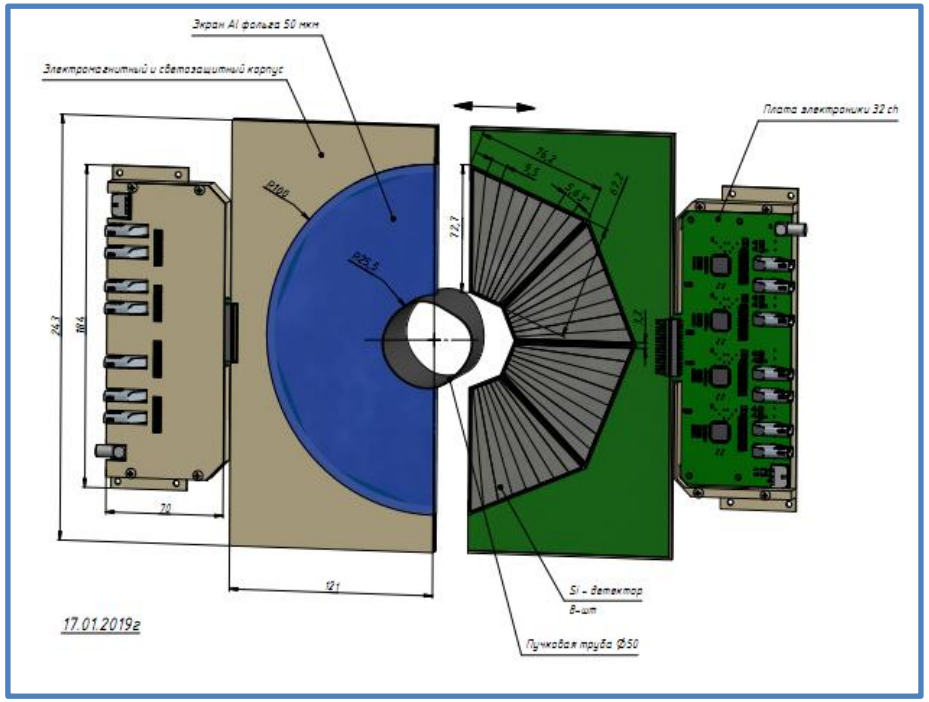
Expected total dark current increase after 2 months at +20 Cº (without self annealing):

$$\Delta I = \alpha \cdot S_{beam} \cdot h_{detector} \cdot \Phi_{1MeV} =$$
$$= 5 \cdot 10^{-17} \cdot 7.07 \cdot 175 \cdot 10^{-4} \cdot 3.45 \cdot 10^{14} = 2.13\ \text{mA}$$

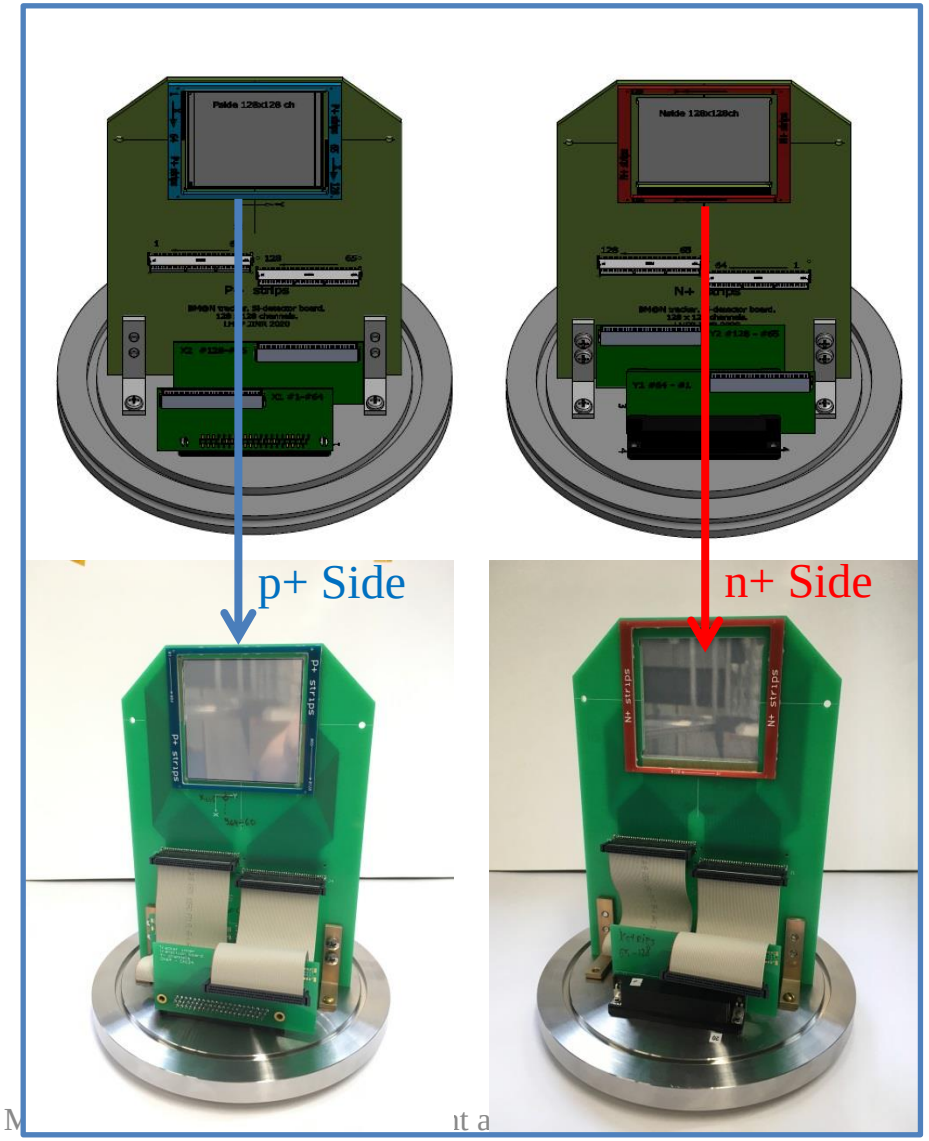
Expected dark current increase of 1 strip in beam zone: $\Delta I \approx 35$ μA

Expected max. power dissipation at V_{bias}= 20 V : $P \approx 42.6$ mW

Detectors before the analyzing magnet

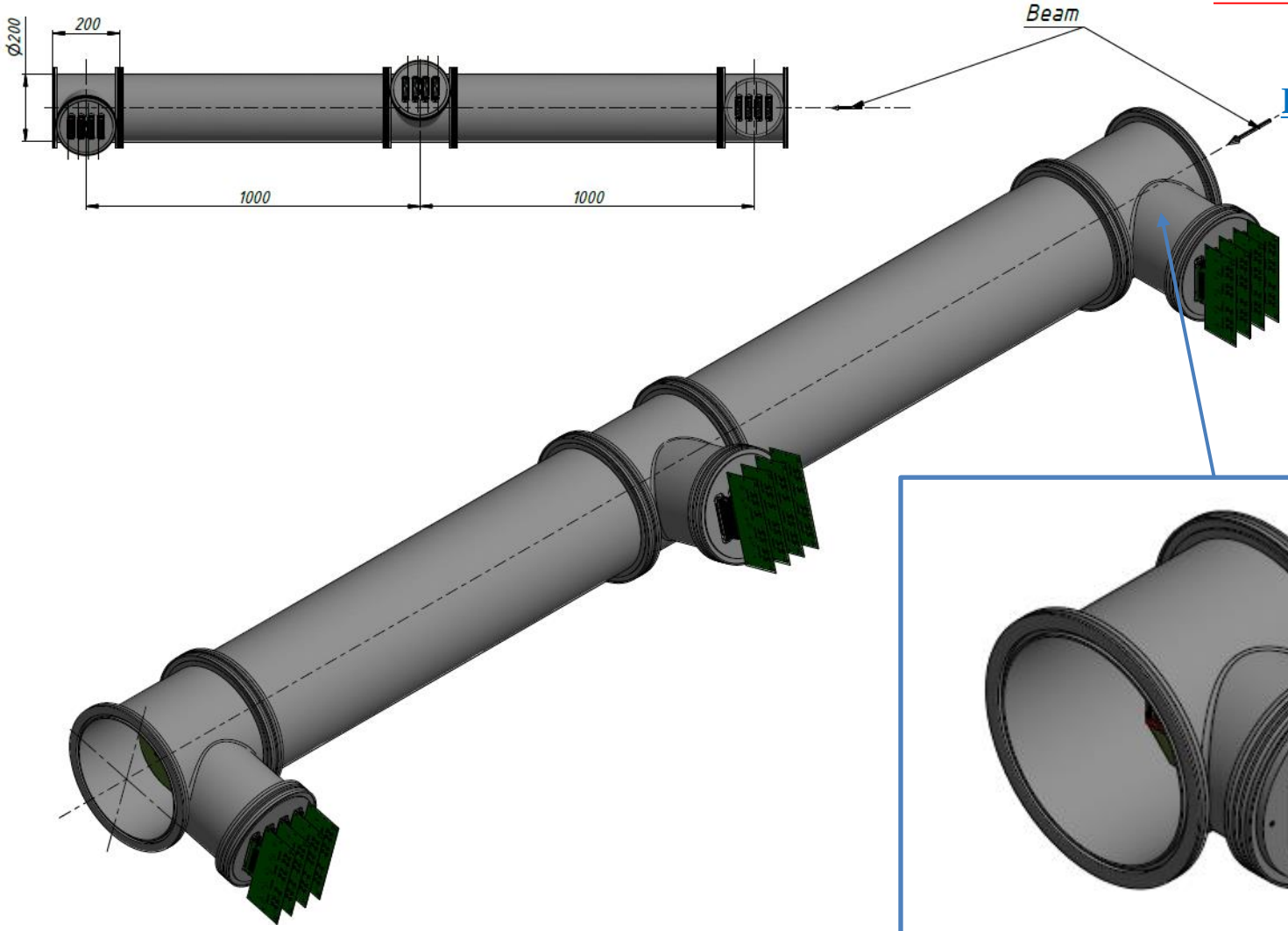


General view of multiplicity trigger which consists of 2 half-planes (8 silicon strip trapezoid detectors, thickness 525 um) and 2 FEE boards.



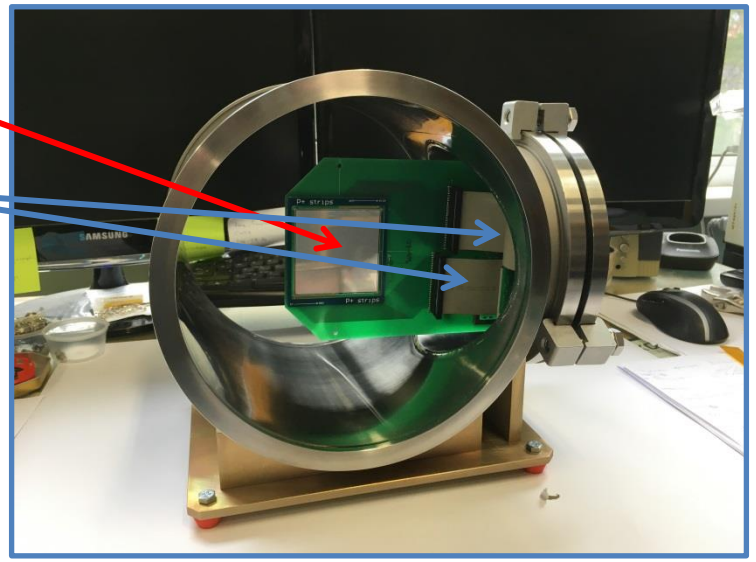
Beam tracker coordinate plane (128x128 strips, thickness 175 um) assembled at vacuum flange.

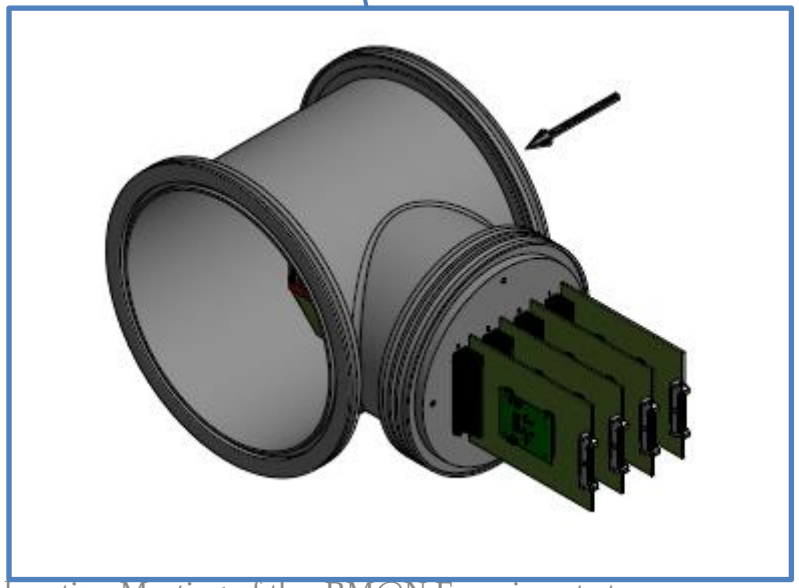
Beam pipe section with beam tracker modules ±15°

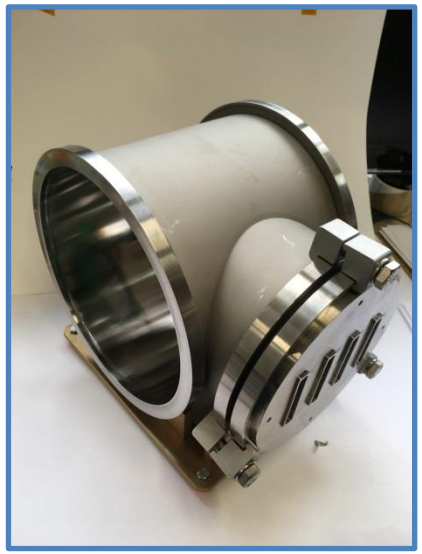


Beam tracker sensor

Readout cables



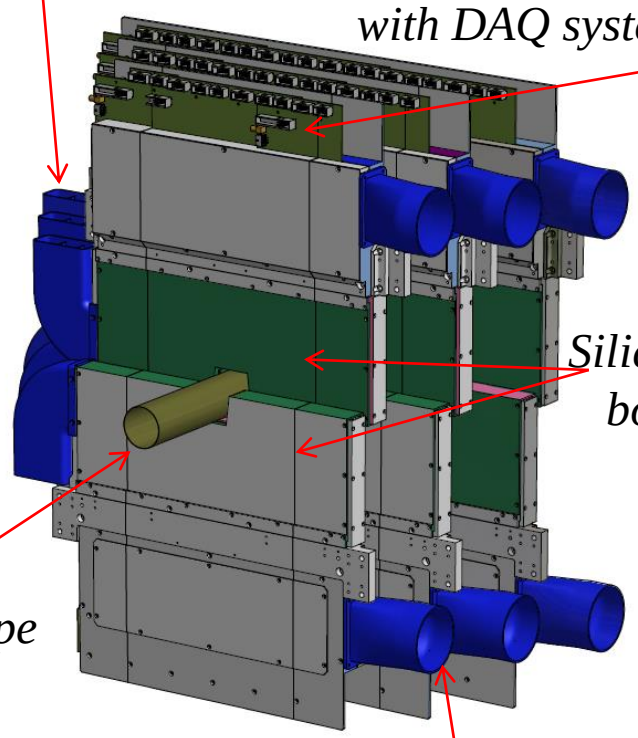


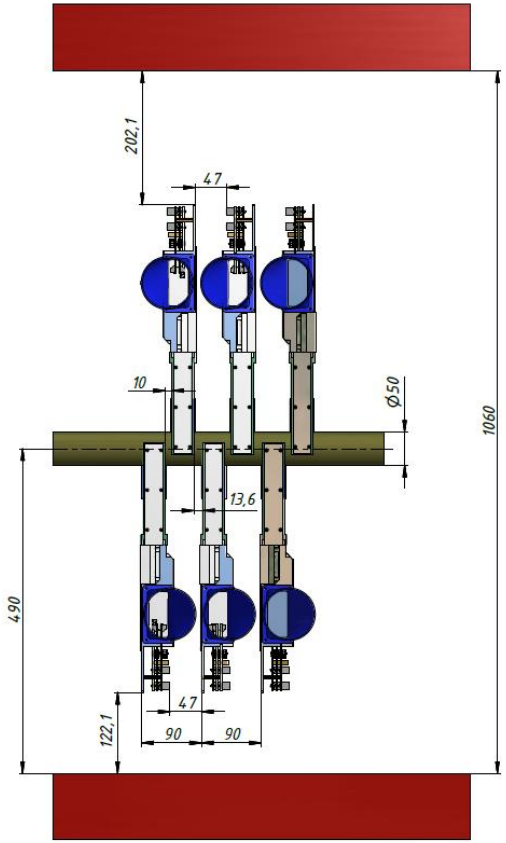


Assembly status for detectors before the analyzing magnet

Part	Planned	Delivered	Contracts №	Ready to assembly and tests
DSSD beam profilometer	10	10	100-1419	✓
DSSD beam tracker	15	15	100-1419	✓
SSSD multiplicity detector	16	16	100-1740	✓
Beam profilometer ASICs VA162				✓
Beam tracker ASICs (VATA64HDR16)	20	20	190091276-74	✓
Beam profilometer PCB	design in progress			
Beam tracker PCB	design in progress			
Multiplicity detector PCB	existing electronics will be used			
Mechanical support	design in progress			

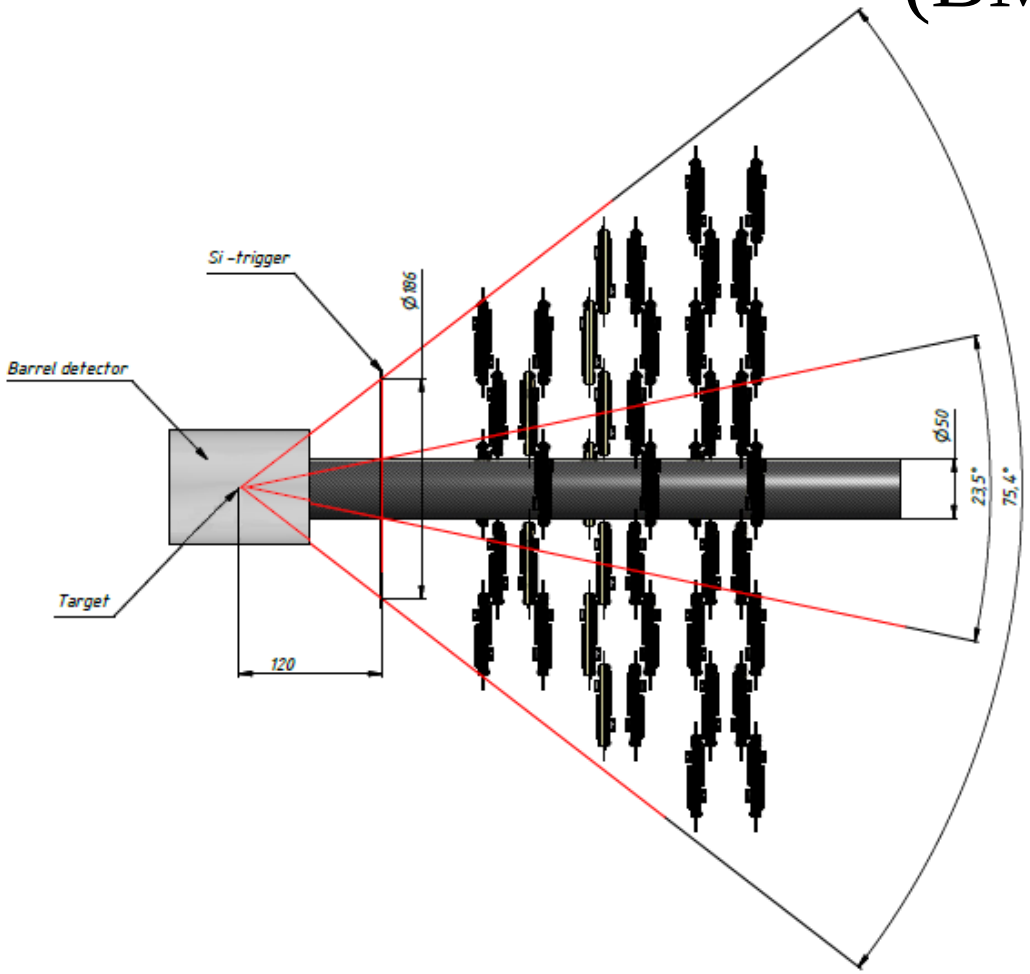
Forward Silicon Detectors Configuration (BM@N – 2020)

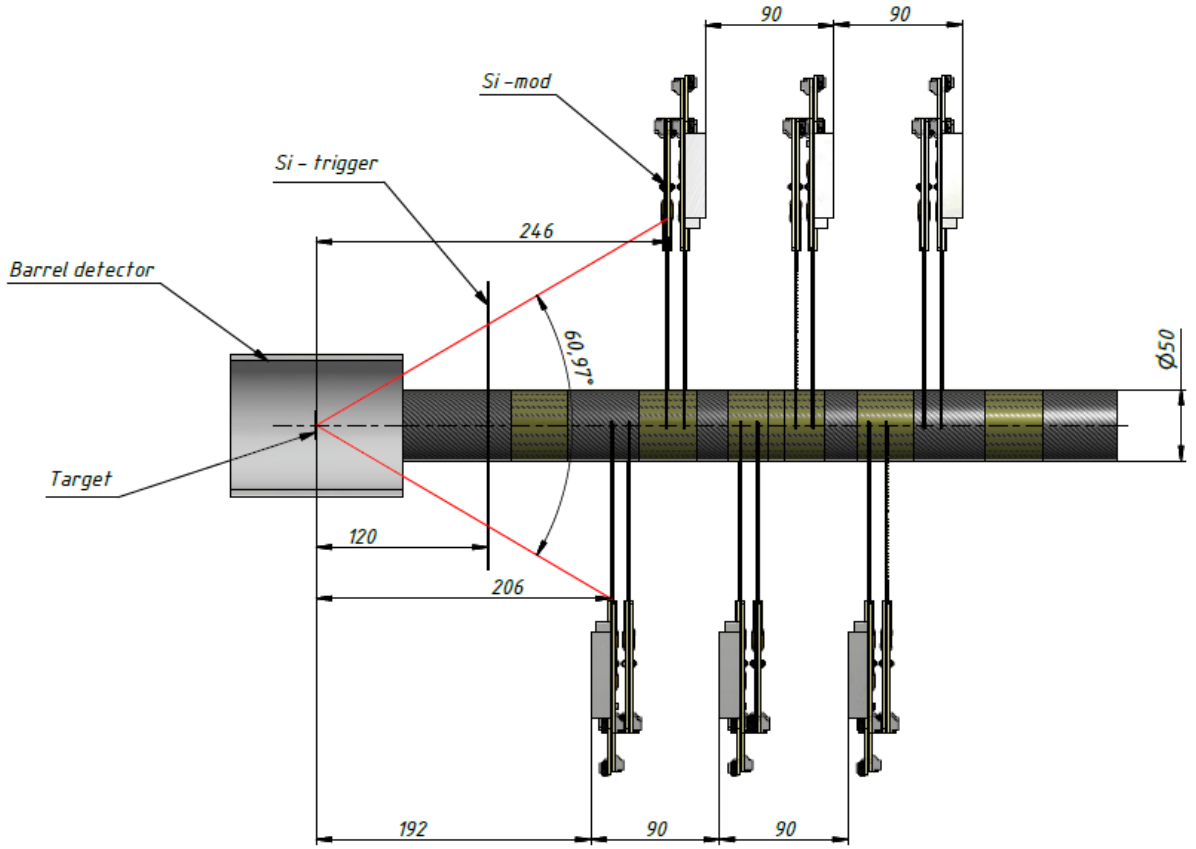




Forward Silicon Detectors in analyzing magnet

Forward Silicon Detectors Configuration (BM@N – 2020)



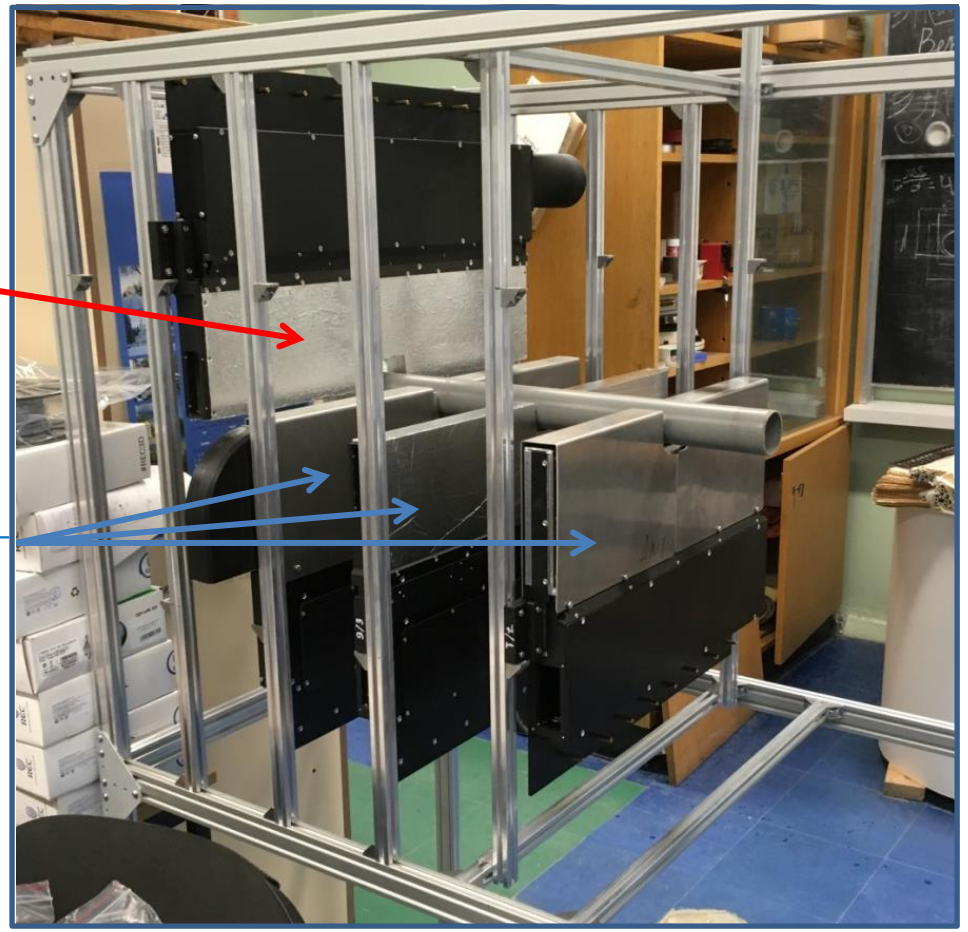


Positions of Si-planes on the beam-channel XZ (left) and YZ (right)

Forward Silicon Detectors Configuration (BM@N – 2020)

Light+EM-shielding

Mechanical protection of detectors during assembling

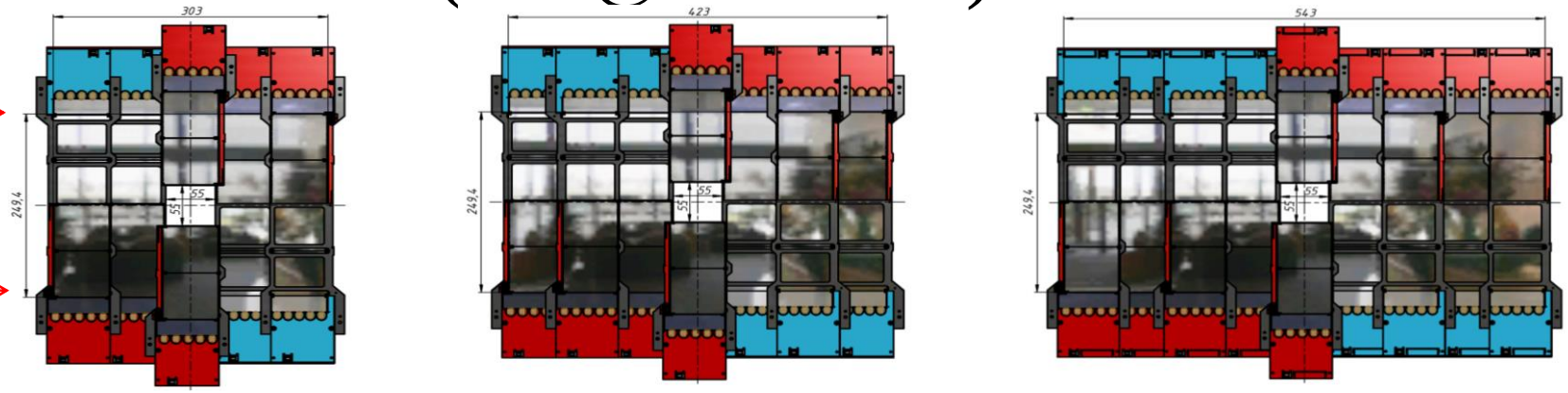


Prototype of mechanical support for Forward Silicon Detectors planes

Forward Silicon Detectors Configuration (BM@N – 2020)

Upper half-planes →

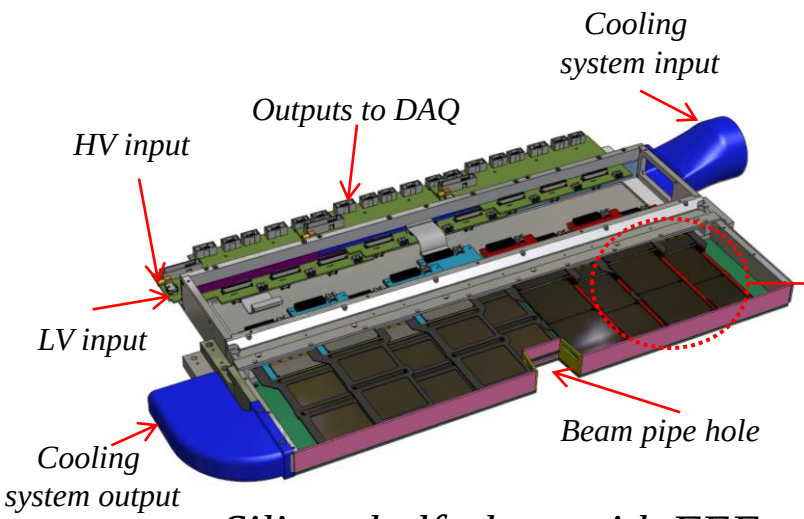
Bottom half-planes →



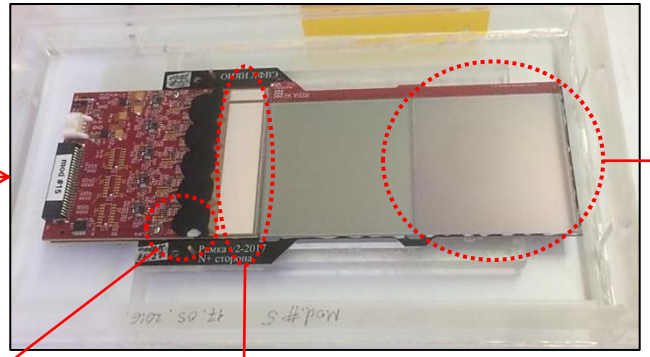
Three tracking silicon planes with FEE boards (using only one type of Silicon Detector Module!)

Number of	First Plane	Second Plane	Third Plane	Total
Si-modules 60x120 mm^2	10	14	18	42
DSSDs	20	28	36	84
ASICs (temp. <= +25 C°)	100	140	180	420
Power dissipation	28,16 W	39,42 W	50,69 W	118,27 W
PAs	20	28	36	84
FEE PCBs	20	28	36	84
Channels	12800	17920	23040	53760
Area, m^2	0.073	0.102	0.132	0.307

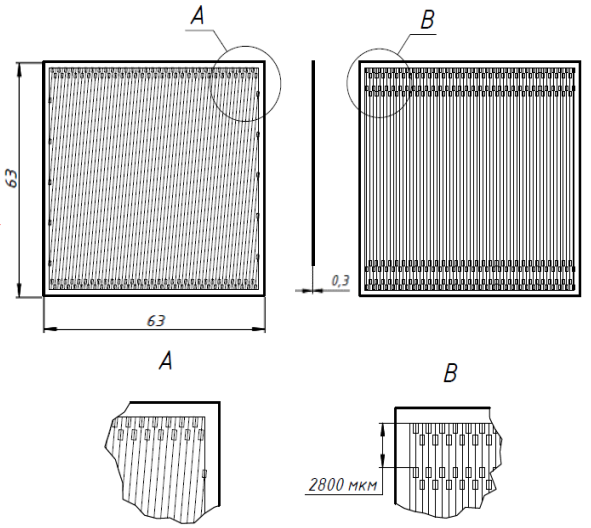
Silicon Detector Module

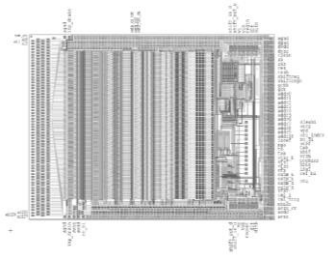


Silicon half-plane with FEE

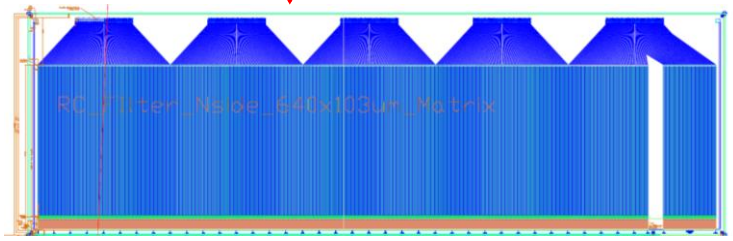


Silicon Detector Module





ASIC VATAGP7.1 (5 chips on each side of module)
Number of CSA: 128 channels
Dynamic range: ±30 fC
Peaking time (slow/fast shaper): 500 ns/ 50ns
Noise (ENC): 70e +12e/pF (typ.)
Voltage supply: +1.5 V, -2.0 V
Gain from input to output buffer: 16.5 μA/fC
Output Serial analog multiplexer clock speed: 3.9 MHz
Power dissipation per channel: 2.2 mW

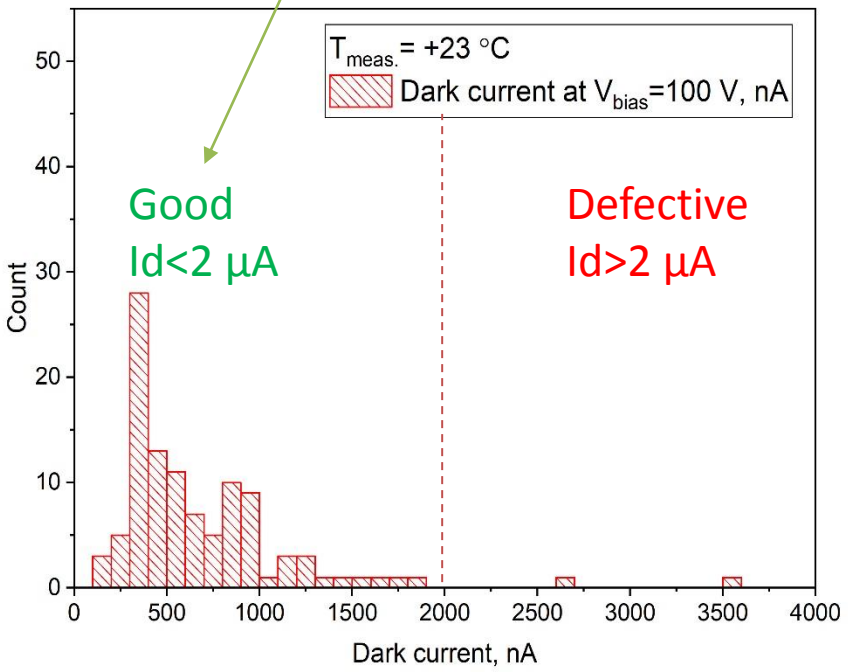


Pitch Adapter (n+) side
sapphire plates with an epitaxial layer of silicon (SOI)
Number of channels: 640
Value of poly-Si resistors: ≈ 1 MΩ
Value of integrated capacitors: ≈ 120 pF
Capacitor working voltage: 100 V
Capacitor breakdown voltage: >150 V

Size: 63x63x0,3 mm^3 (on 4" – FZ-Si wafers)
Topology: double sided microstrip (DSSD)
(DC coupling)
Pitch p^+ strips: 95 μm;
Pitch n^+ strips 103 μm;
Stereo angle between p^+/n^+ strips: 2.5^0
Number of strips/DSSD: 640 (p^+)× 614(n^+)
Number of strips/module: 640 (p^+)× 640(n^+)

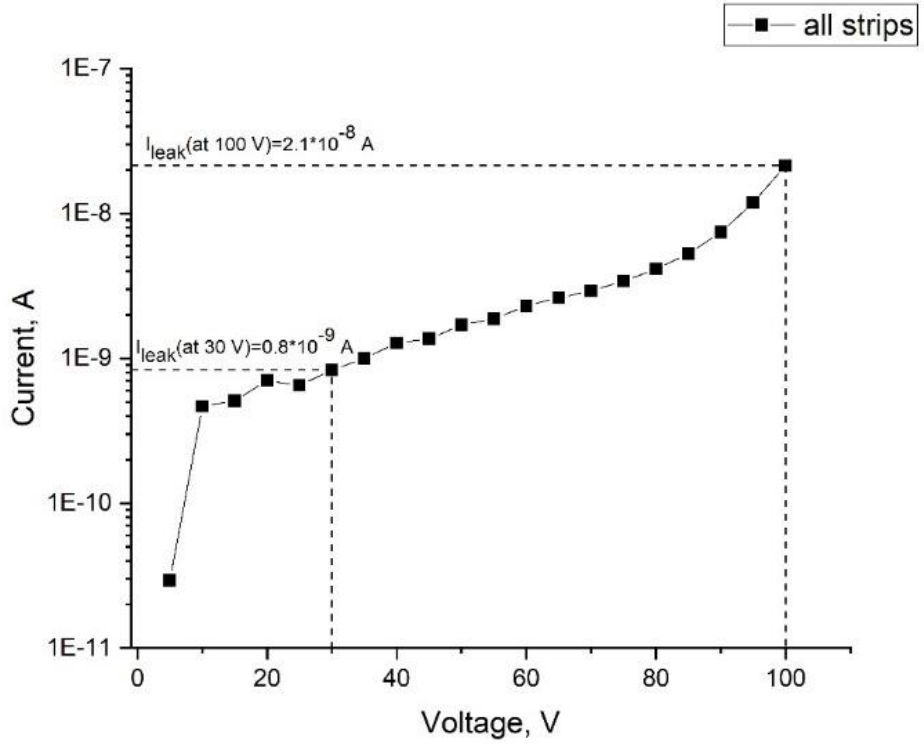
DSSD (640x640 strips) and PA tests

Satisfy with specification requirements



Summary DSSD's Dark Currents at Vbias = 100 V and T= +23 ^{0}C

From 105 DSSDs – 103 marked as Good

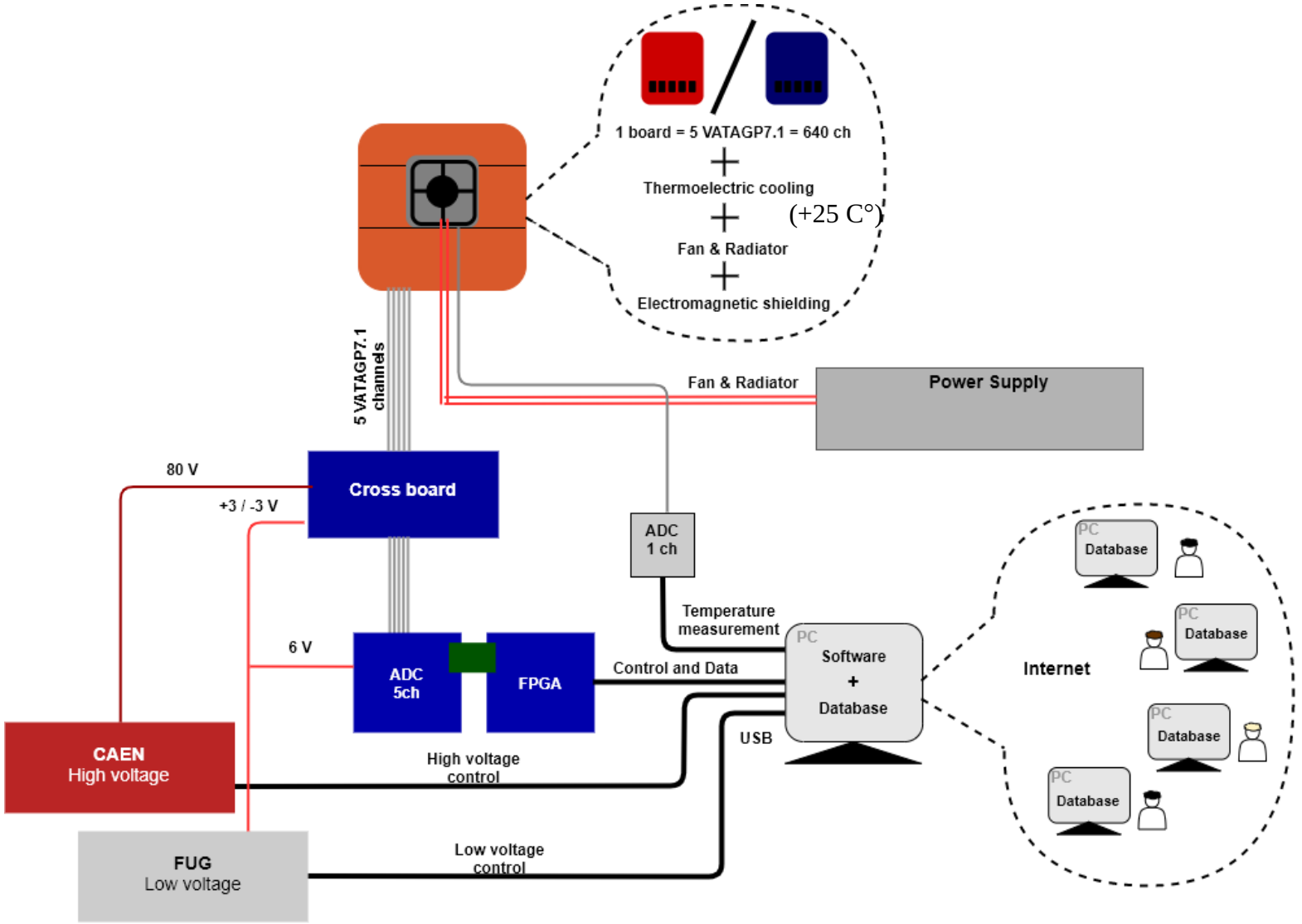


Summary leakage current for all PA's (n+ side) strips

See E. Streletskaya talk

Front-end electronics test steps

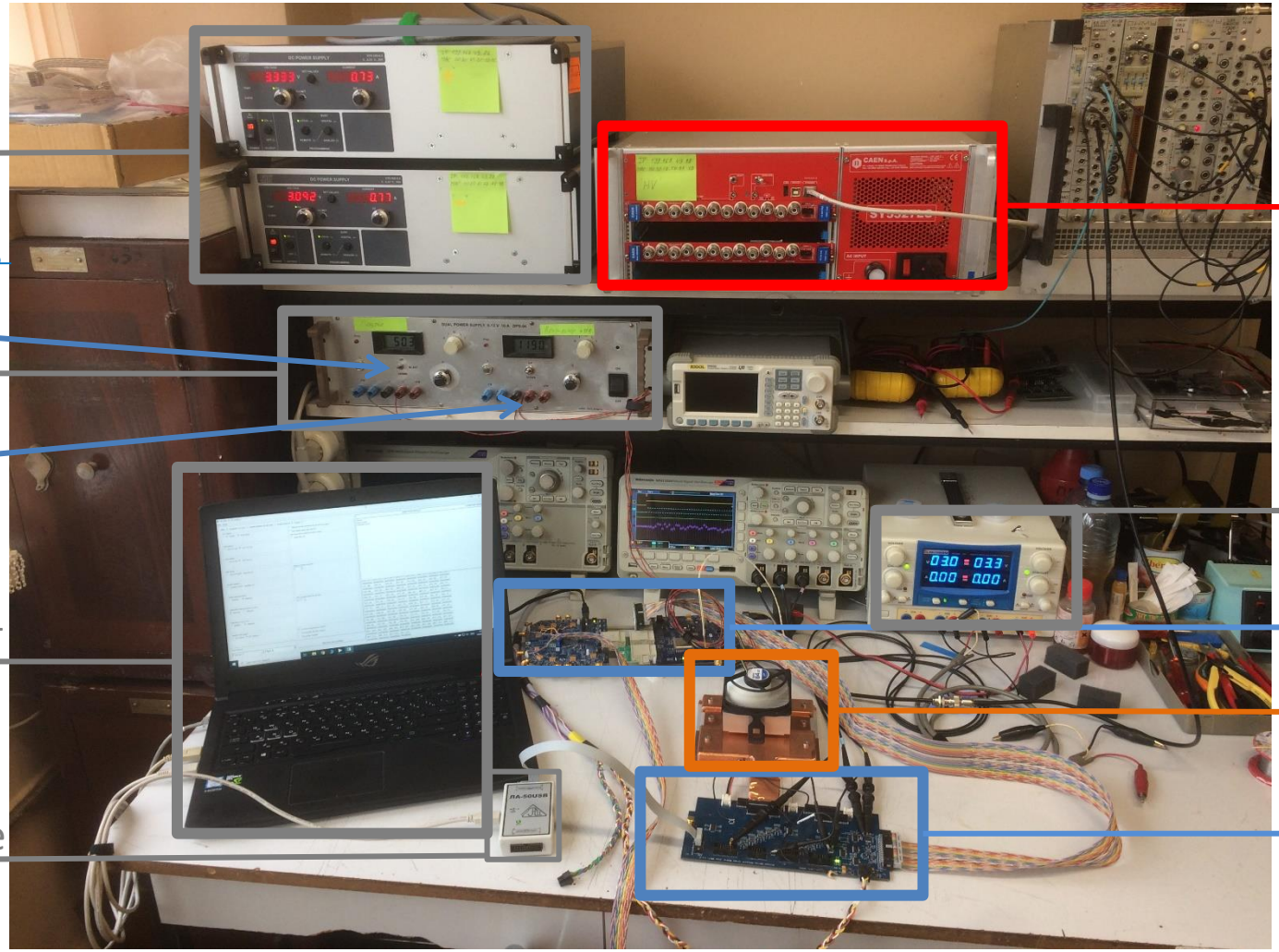
Front-end electronics test stand



Testing scenario:

1. Connect PCB to stand (HV, LV and temperature will be measured whole time) in cooling and EM shielding box;
2. Make pedestal run for each chip without HV at pitch-adapter, save raw data;
3. Send configuration data to each chip;
4. Measure crosstalk between neighbor channels (external test signal);
5. Measure I(PA)= f(U_{HV}) leakage current of PA-640n+ (only for n+ PCB);
6. Measure ENC= f(U_{HV}) (only for n+ PCB);
7. Save data to the database.

Front-end electronics test stand

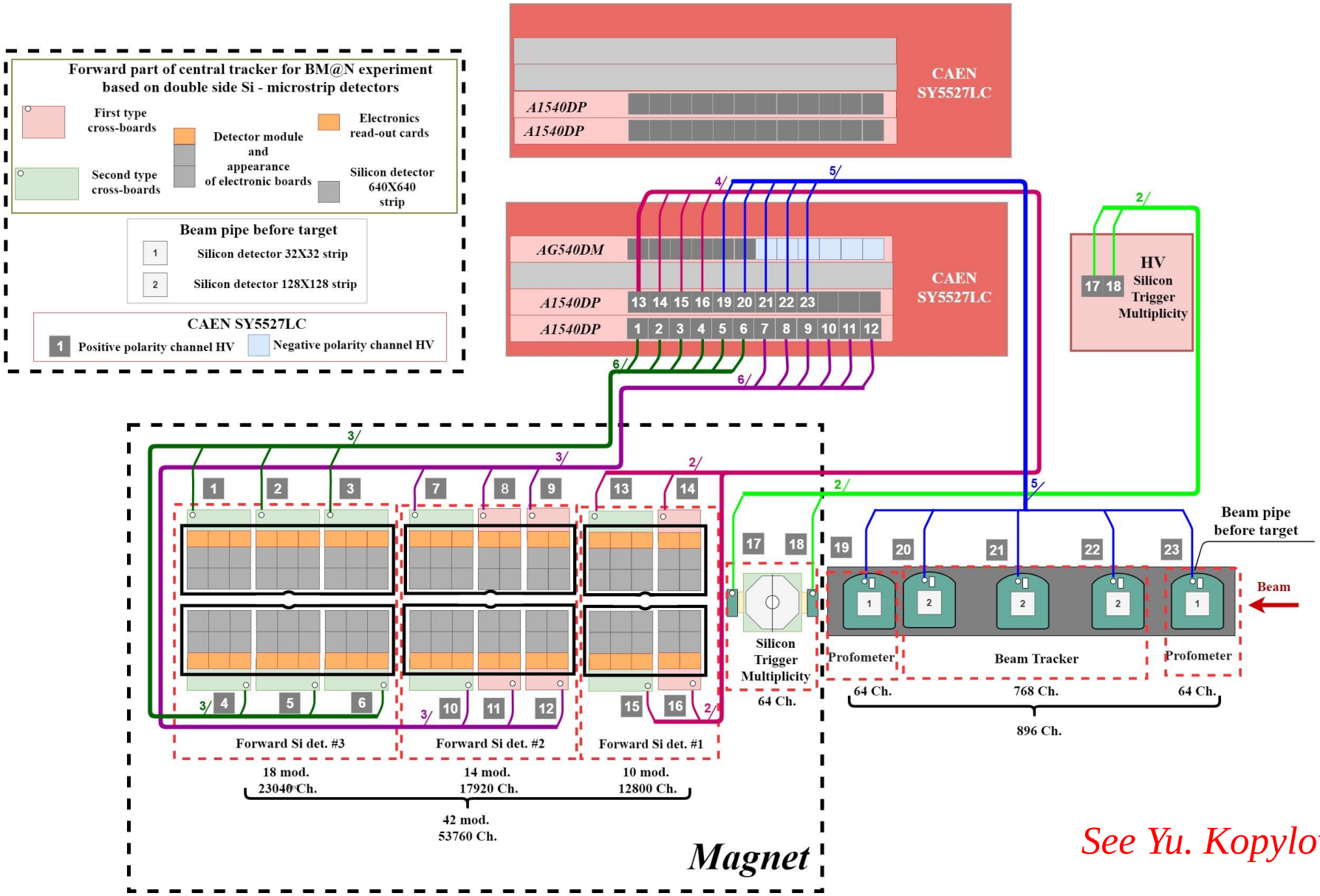


Front-end electronics test stand

Status of test stand components

Cooling and EM shielding box ✓	CAEN HV ✓	FUG LV ✓
Cross board ✓	FPGA ✓	ADC ✓
Database ✓	Control software	

HV power supply



See Yu. Kopylov talk

Assembly status

Part	Planned	Delivered	Contracts №	Ready to assembly and tests
DSSD	85	90	100-1338	✓
Pitch adapters	50 (n+ side) and 50 (p+ side)	70 (n+ side) and 70 (p+ side)	100-1199	✓
ASICs VATAGP7.1	500	500	100-959 100-1236	✓
FEE PCBs	50 (n+ side) and 50 (p+ side)	50 (p+ side) 50 (n+ side)	29437	✓
ADCs and Control Units	8 + 8	8 + 8		✓
Power supply (High voltage)	1 crate, 3 HV blocks CAEN	1 crate, 3 HV block	100-1274	✓
Power supply (Low voltage)	4 FUG Electronik	4	100-1641	✓
Cross boards	design in progress			
Cooling system	1 air conditioner Weltem WPC-4000	1	У32651	✓
Mechanical support for FSD planes	design in progress			

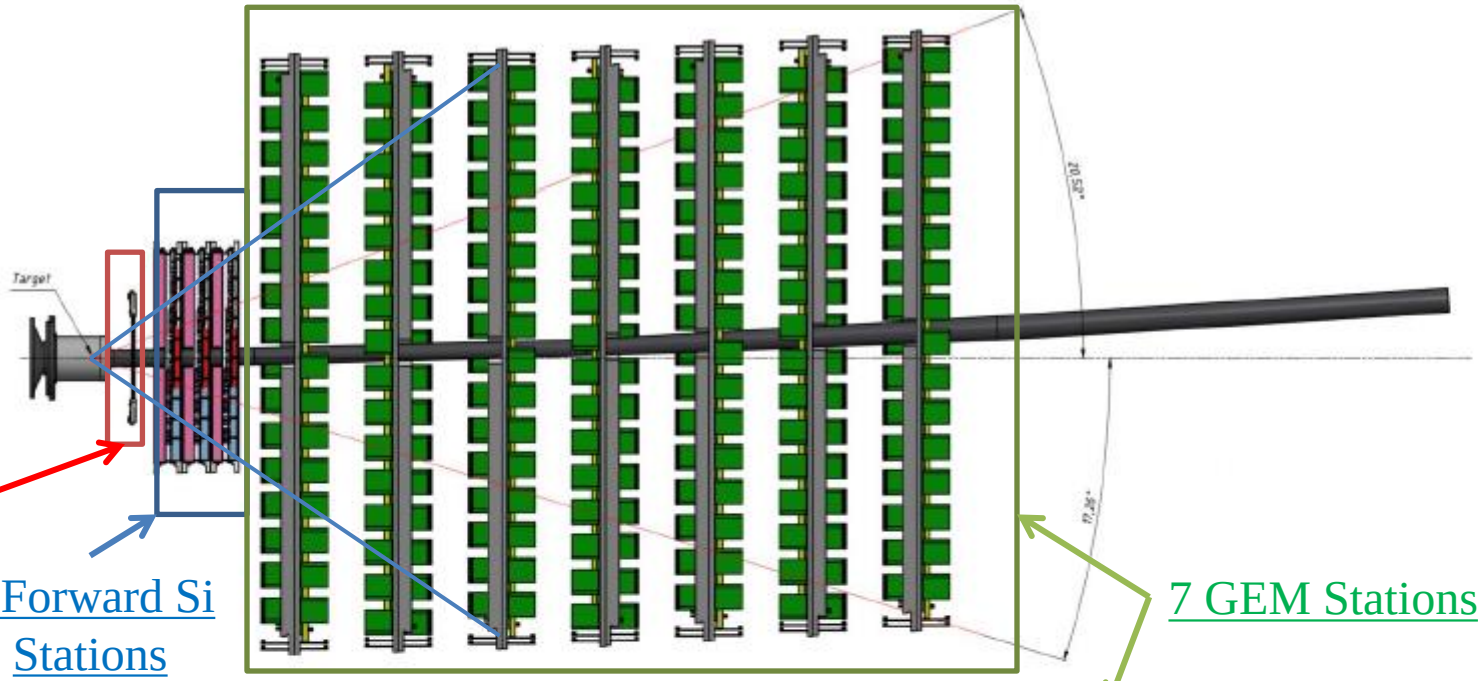
Conclusions

- Detectors PCBs for beam trackers are designed and produced;
- FEE boards for detectors before the analyzing magnet are being designed now (for multiplicity detector existing electronics will be used);
- At the moment a new Forward Silicon Detector design has been developed based on Silicon Detector Modules, which had been used in previous BM@N runs;
- Prototype of mechanical support for Forward Silicon Detectors planes are designed and produced;
- Testing of DSSDs (for all Si-subsystems) and Pitch Adapters in progress;
- Design of test stand for FSD FEE electronics are done. Main components of stand are assembled. Development of stand control software in final stage;
- Most of the Detectors before the analyzing magnet and Forward Silicon Detector's components are procured and delivered at VBLHEP;
- All pitch adapters have been assembled with FEE PCBs, all modules will be assembled at September'20 – March'21

Backup slides

Forward Silicon Detectors + GEMs configuration

XZ – projection

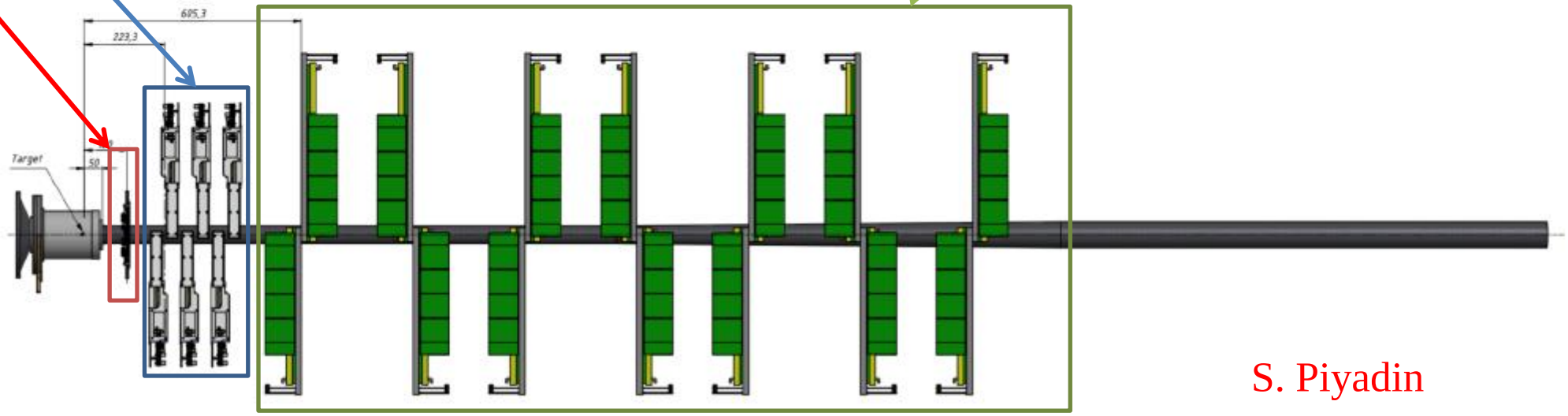


Si multiplicity trigger

3 Forward Si Stations

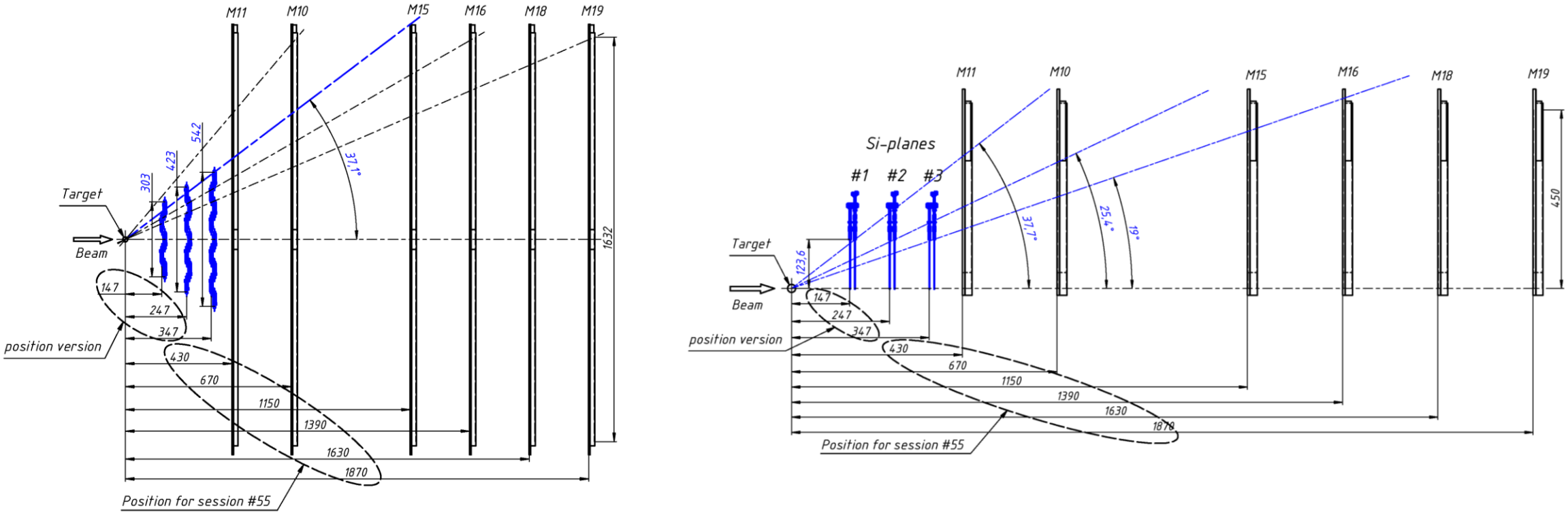
7 GEM Stations

YZ – projection



S. Piyadin

Forward Silicon Detectors Configuration (BM@N – 2020)



Positions of Si-planes on the beam-channel XZ (left) and YZ (right)