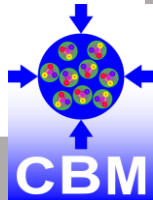
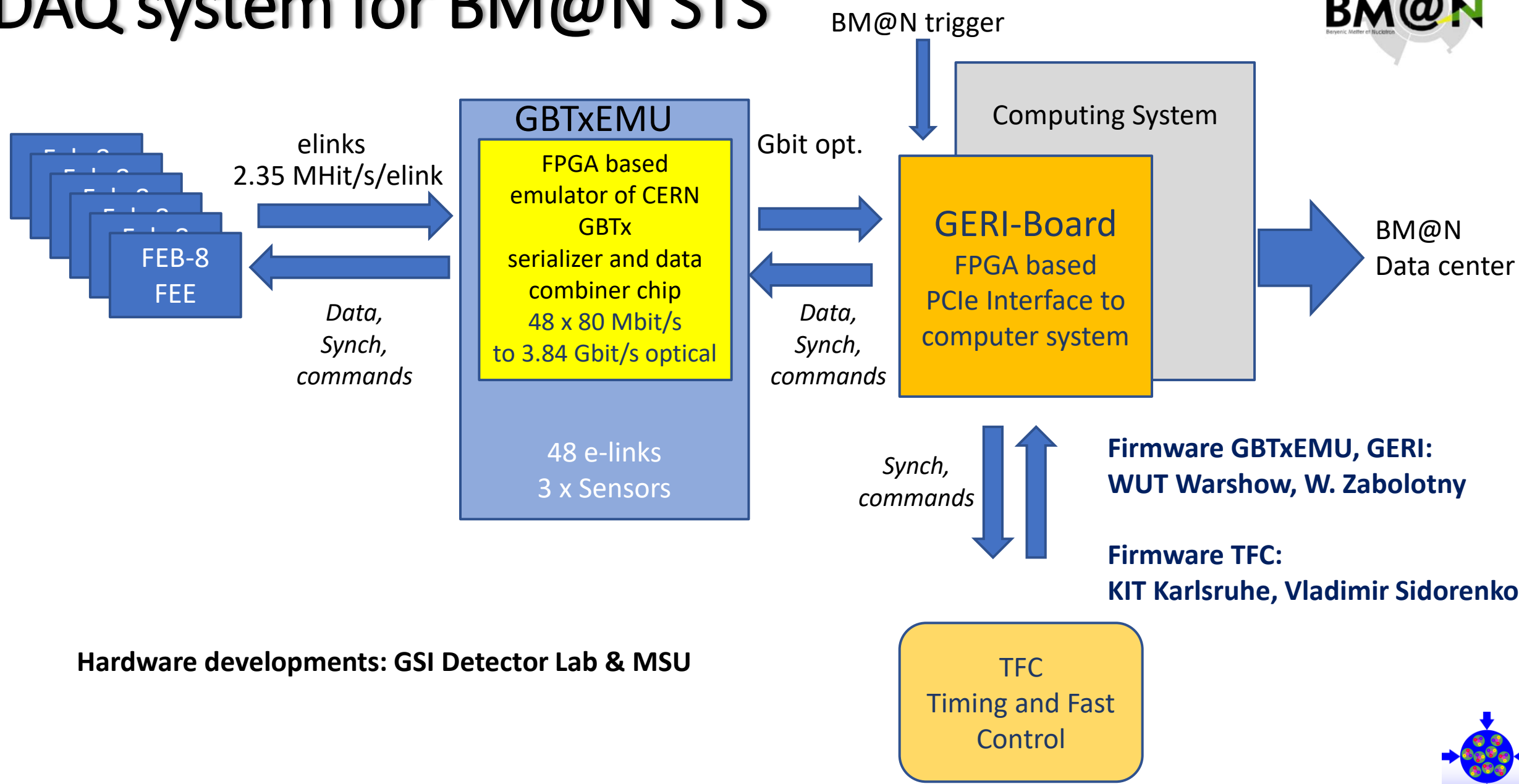


DAQ for BM@N STS

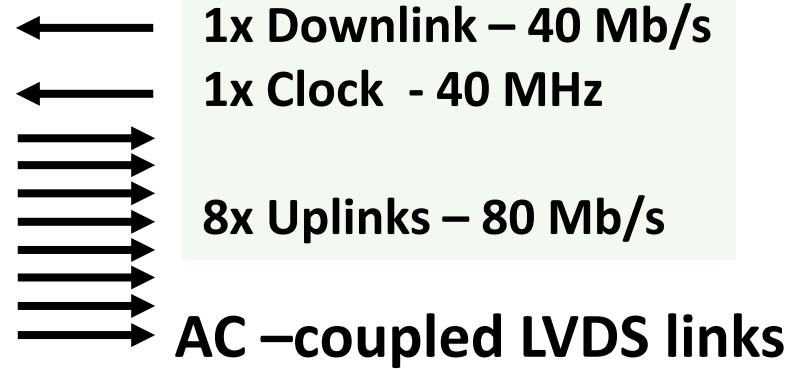
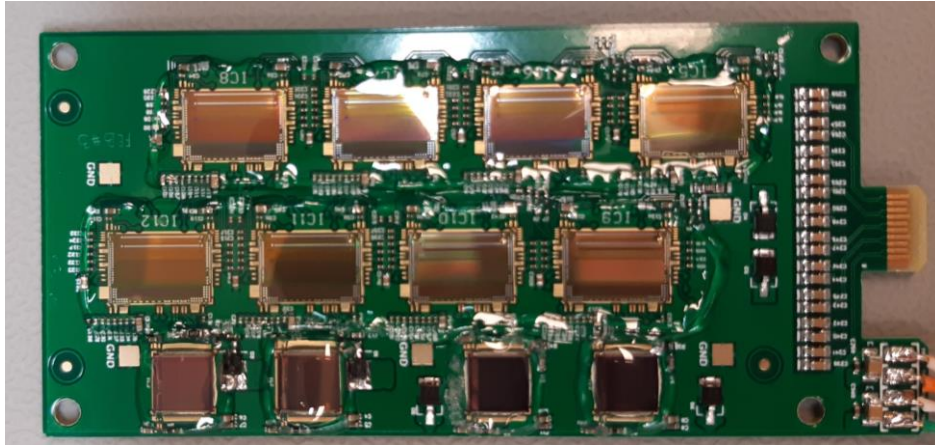
**Dmitrii Dementev, Wojciech Zabołotny, Marek Gumiński
and Michał Kruszewski for STS DAQ group**

5th Collaboration Meeting of the BM@N experiment at NICA Facility
20-21 April 2020, JINR-VBLHEP, Dubna

DAQ system for BM@N STS



Front-end Boards



8x STS-XYTER ASICs on board
Self-triggered readout
provides digitized hits:

- 5bit pulse height
- 14bit timestamp

Hit frame: 30 bits

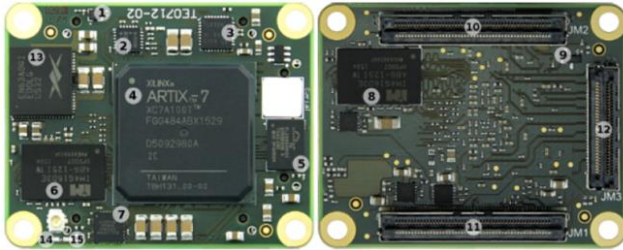
~ 10 m electrical connection to GBTxEMU

Each STS-XYTER is capable of delivering data of up to 50 MHits. The FEB-8 to be employed for BM@N will have connectivity for 10 MHits per chip. The FEB may be operated at lower clock speeds down to 40 MHz.

In such a mode of operation the maximum hit rate per ASIC is then 2,5 MHits per second.

According to the simulations the hit rate per ASIC will be lower than 0,32 MHits/s

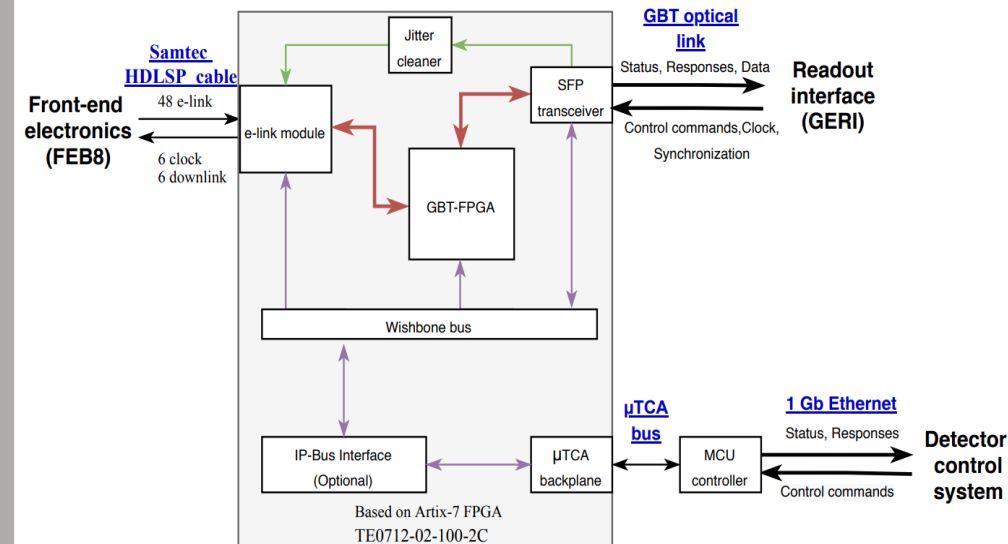
GBTxEMU



Trenz TE0712-02-100-2C
platform from Xilinx

- ❑ Emulates functionality of GBTx ASIC on FPGA
- ❑ Platform: Trenz TE0712-02-100-2C from Xilinx
- ❑ 48 elinks with 40 MHz clock and 80 Mb/s data rate
- ❑ Control interface: IPbus via 100 Mb/s Ethernet
- ❑ Clock recovery with Si5338 chip

GBTxEmulator board

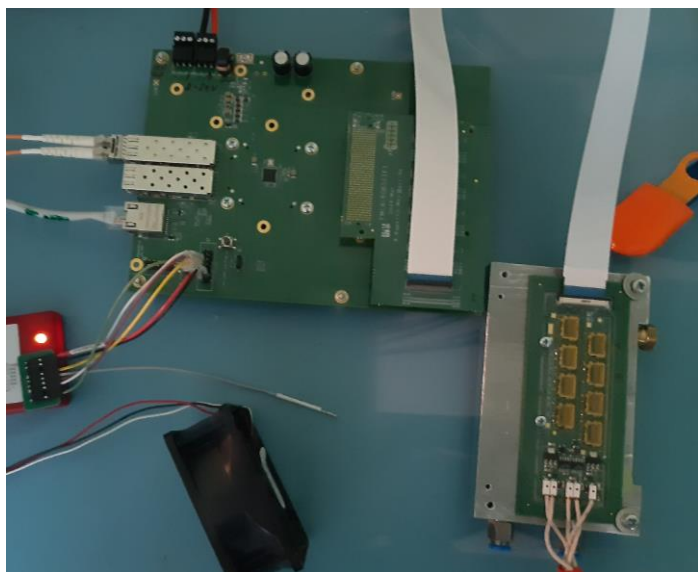
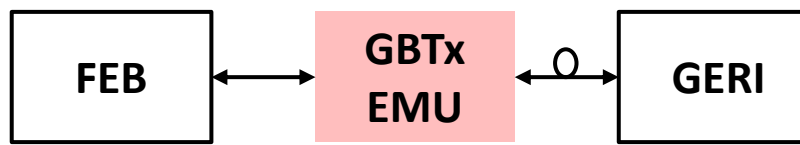


Hardware developments: [C.J. Schmidt et al](#) at GSI Det. Lab.

Firmware developments: [Wojtek Zabolotny et al](#) at Warsaw University of Technology (WUT)

Software developments: WUT and JINR (M. Shitenkow)

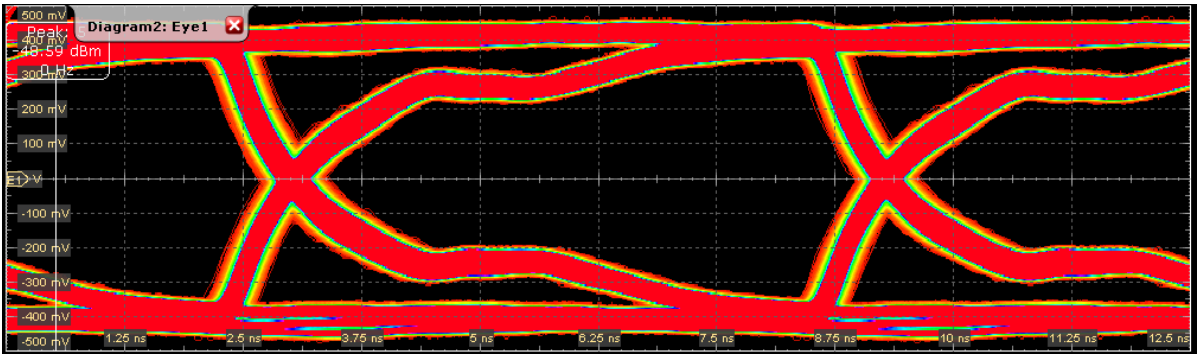
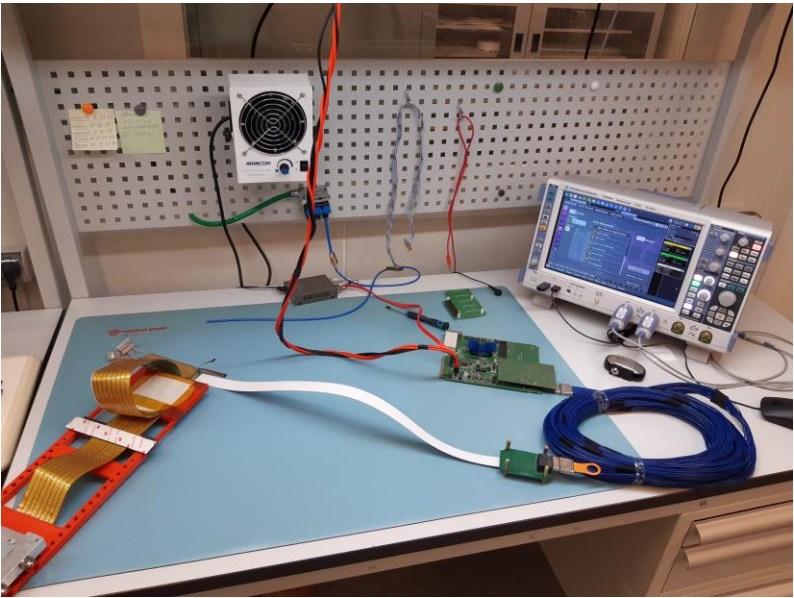
GBTxEMU: status



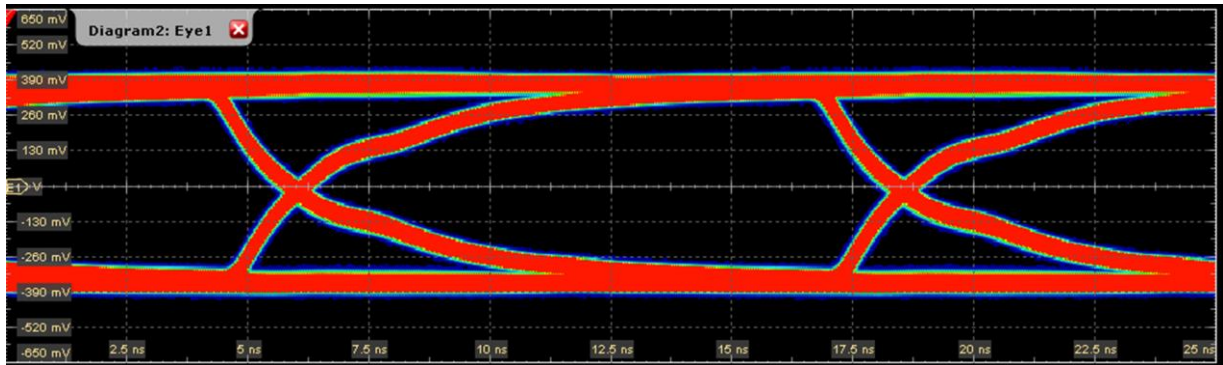
Test bench with GBTxEMU at JINR

- GBTxEMU boards available and with FEB-C and STS FEB-8 as sample e-link front end boards
 - e-links operative
 - clock recovery and jitter cleaning works from Gbit optical links
 - downgrade e-link 160 MHz → 40 MHz

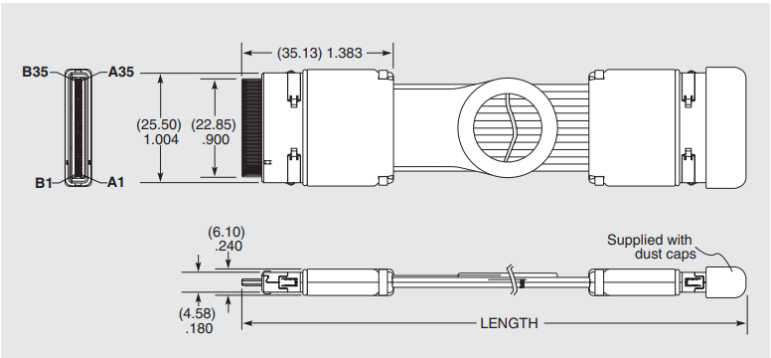
Performance of STS-HCTSP with long cables



Eye diagram of the Dwn-link signal at 160 MHz Clck

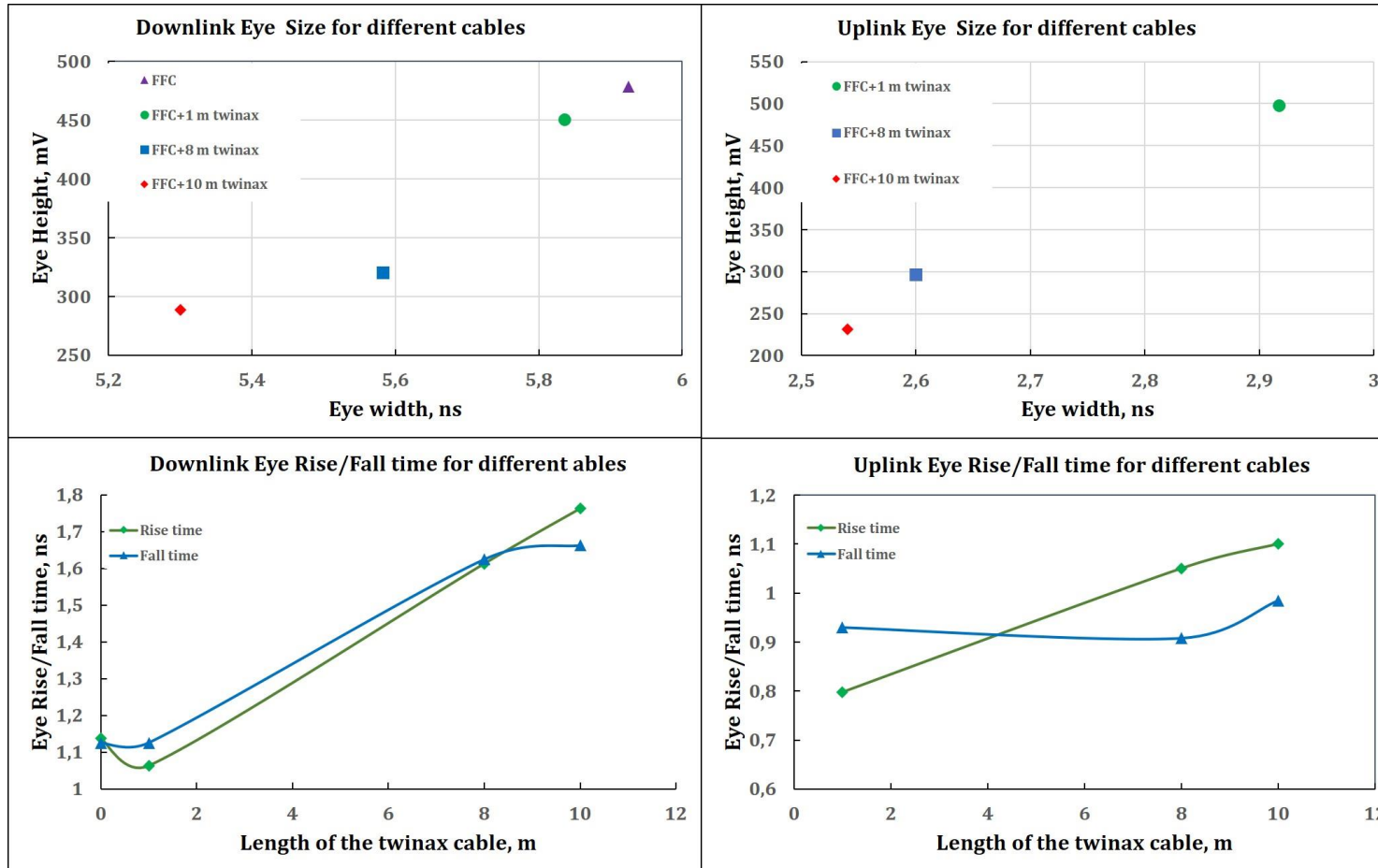


Eye diagram of the Dwn-link signal at 80 MHz Clck

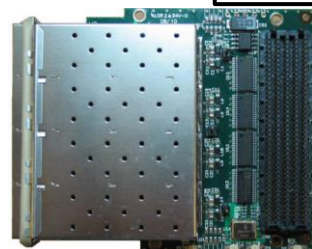


Samtec HDLSP twinax cable

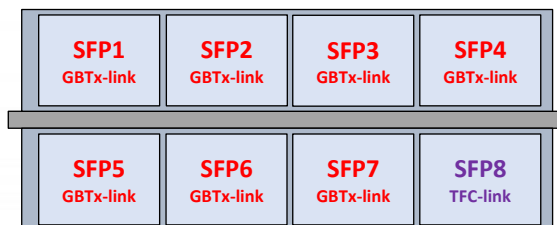
Performance of STS-HCTSP with long cables



10 m data cable connection was tested with different types of the cables
Samtec HDLSP twinax cable was opted
It is capable to transmit data even at speed of 320 Mbit/s



FM-S18 FMC



TRENTZ TEC0330-4 PCIe Gen2 Interface Board



Compute node with data processing boards

GBTxEMU Readout Interface (GERI)

Is based on the commercial platform: TRENTZ TEC0330-4

- ☐ FPGA based
- ☐ Preprocessing of the data
- ☐ Timing and control interfaces
- ☐ Trigger interfaces
- ☐ Up to 7 GBTxEMU boards could be connected
- ☐ Refactoring of the DPB FW is ongoing

FW developments by WUT group:

Wojciech Zabołotny,
Marek Gumiński,
Michał Kruszewski

Implementation of the TRIGGER mode of operation

Proposal by F/W group from WUT:

Wojciech Zabołotny,

Marek Gumiński,

Michał Kruszewski

Where we can implement the TRIGGER?

- It would be perfect to filter the data as soon as possible, limiting the load for further data links.
- From that point of view, it would be good to do that in GBTxEMU.
- Unfortunately, if we want to maintain GBTxEMU \leftrightarrow GBTX compatibility, it can't be done. GBTX does not provide buffering of data. Adding that feature in GBTxEMU would make it a completely new design with different data flow.
- The GBTxEMU (like GBTX) transfers the data transparently. It is almost impossible to add the data analysis function to it.
- Therefore the right place for data filtering according to trigger decision is GERI.

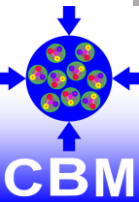
Heap sorter-based readout architecture (version for CBM)

- ❑ The sorters must store the data for the amount of time longer than the maximum „decorrelation time” – ie. 1024 hits cycles/E-Link
- ❑ Even for 1 link and for 320 Mb/s transmission it gives 96μs!
- ❑ So the sorter delay itself allows implementation of the trigger with latency of 5μs.
- ❑ The trigger may be implemented as a filter located at the output of the sorters.
- ❑ However, that architecture was postponed, as it poorly performed with highly fluctuating data streams.

A new bucket sorter architecture



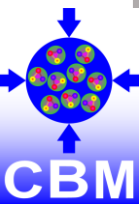
- ❑ At high data rates the incoming data could overflow the sorter and cause „time jumps” in collected data.
- ❑ A new proposed architecture uses the bin sorter (bucket sorter), where data are simply split into „bins” covering consecutive time periods.
- ❑ Inside of the bin the data are not sorted.
- ❑ That architecture better performs at fluctuating data rates (e.g., the superfluous data may be discarded, and that fact may be marked in the bin flags)
- ❑ That architecture is also highly flexible. We may easily define the maximum delay of the data, after which the delayed incoming data should be discarded.



Possibility of implementation of the trigger in bucket sorter-based solution



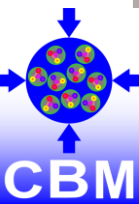
- ❑ The solution based on bucket sorter is extremely convenient for implementation of the trigger.
- ❑ If the trigger didn't occur in the time period covered by the bin, the whole bin may be immediately skipped at no additional cost
- ❑ If the trigger occurred in the time period covered by the bin, the data should be transmitted.
- ❑ If the time period associated with the trigger is shorter than the bin time period, the data may be filtered out when reading the bin (the data in the bin are unsorted).



Current status of the FW



- The new readout architecture is currently tested in CBM
- The bin length is set to $3,2 \mu\text{s}$ and the number of bins is 16, that makes possible to implement the trigger with latency of $5\mu\text{s}$!



Bandwidth of the system

- ❑ 49 GBTxEMU boards
- ❑ 14 GERI boards in server nodes
- ❑ 1 TFC with 1:16 synch fanout


- ❑ Cables GBTxEMU - GERI:
98x SM LC-LC duplex optical fibers
- ❑ Cables GERI nodes - BM@N Data Center:
4x 100G ethernet -?
- ❑ Trigger cables:
14 pcs

Total bandwidth of the system (up to STS nodes):

*80 Mbps*16 ASICs*292 modules = 374 Gb/s*

Estimated maximum data rate with Au beam and interaction rate $5 \cdot 10^6$ Hz:

*$5 \cdot 10^{-4}$ hit/ev./strip * 2*1024 strips/module*292 modules * 30 bit* $5 \cdot 10^6$ Hz =*
45 Gb/s – in a free-streaming mode



Thank you for
your attention!

Timing and Fast Control (TFC) hardware



Picture source: Creotech website

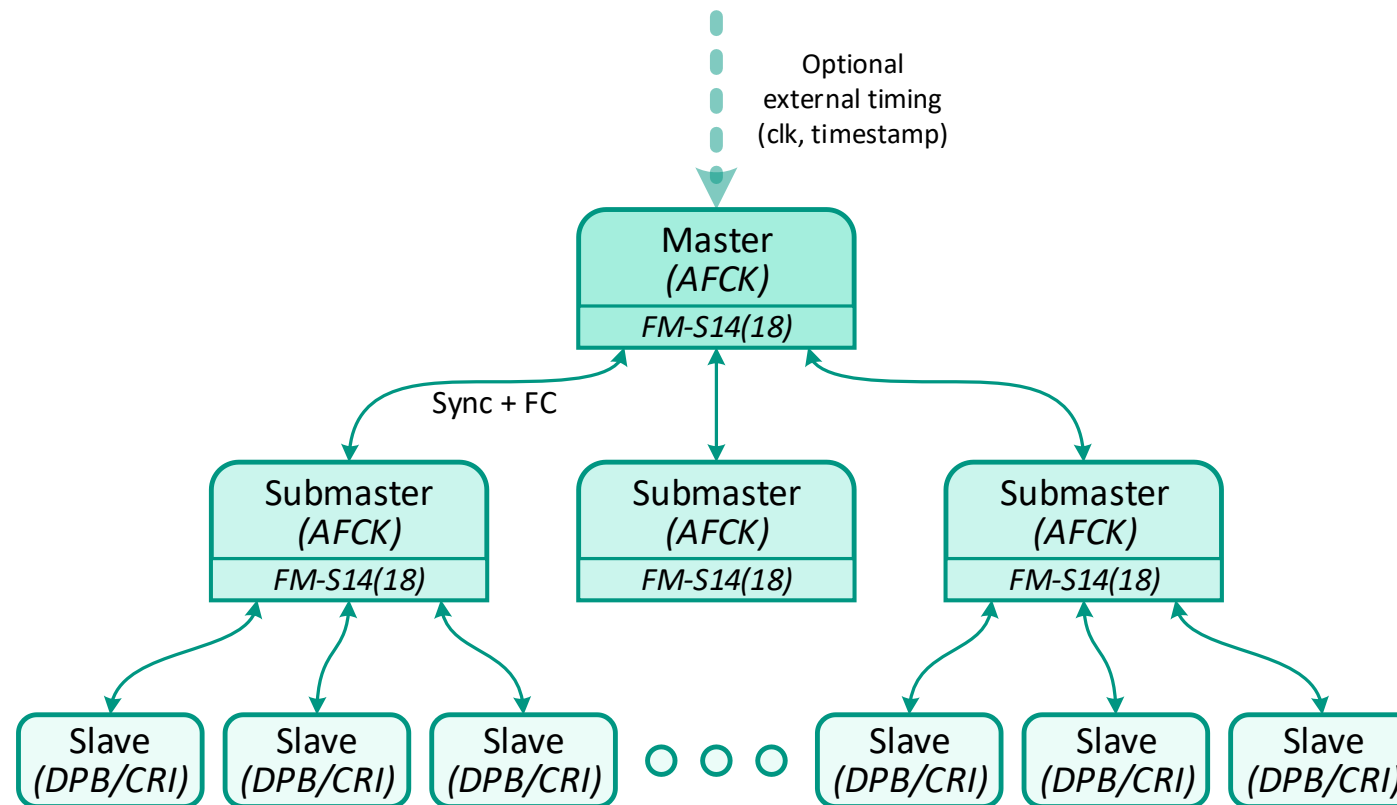
Timing mezzanine (COTS) – FM-S14



Picture source: FM-S14 User Manual

TFC topology

- Inspired by WR
- Communication over optical links
- Can be tailored for an external timing source



TFC core

- Number of TFC links scales up by replicating the “timing node” components
- Unified core for all nodes

