Design of the FEE for BM@N Si-subsystems

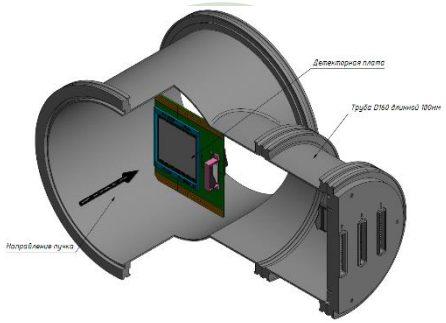
Status

Yu. Ivanova on behalf of
Forward Silicon Detector team

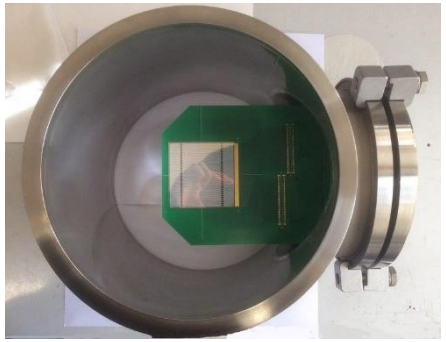
5th Collaboration meeting of the BM@N Experiment

20-21 April 2020

Si-subsystems

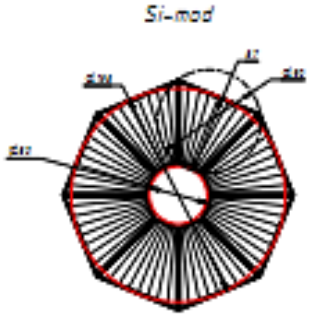


Beam profilometer
(32x32, 2 planes)

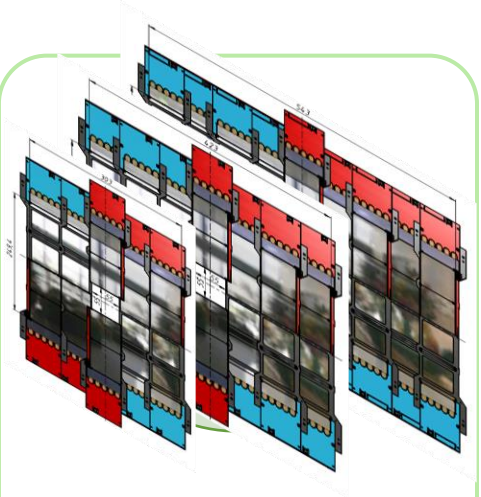


Beam tracker
(128x128,
3 planes)

Target



Multiplicity trigger

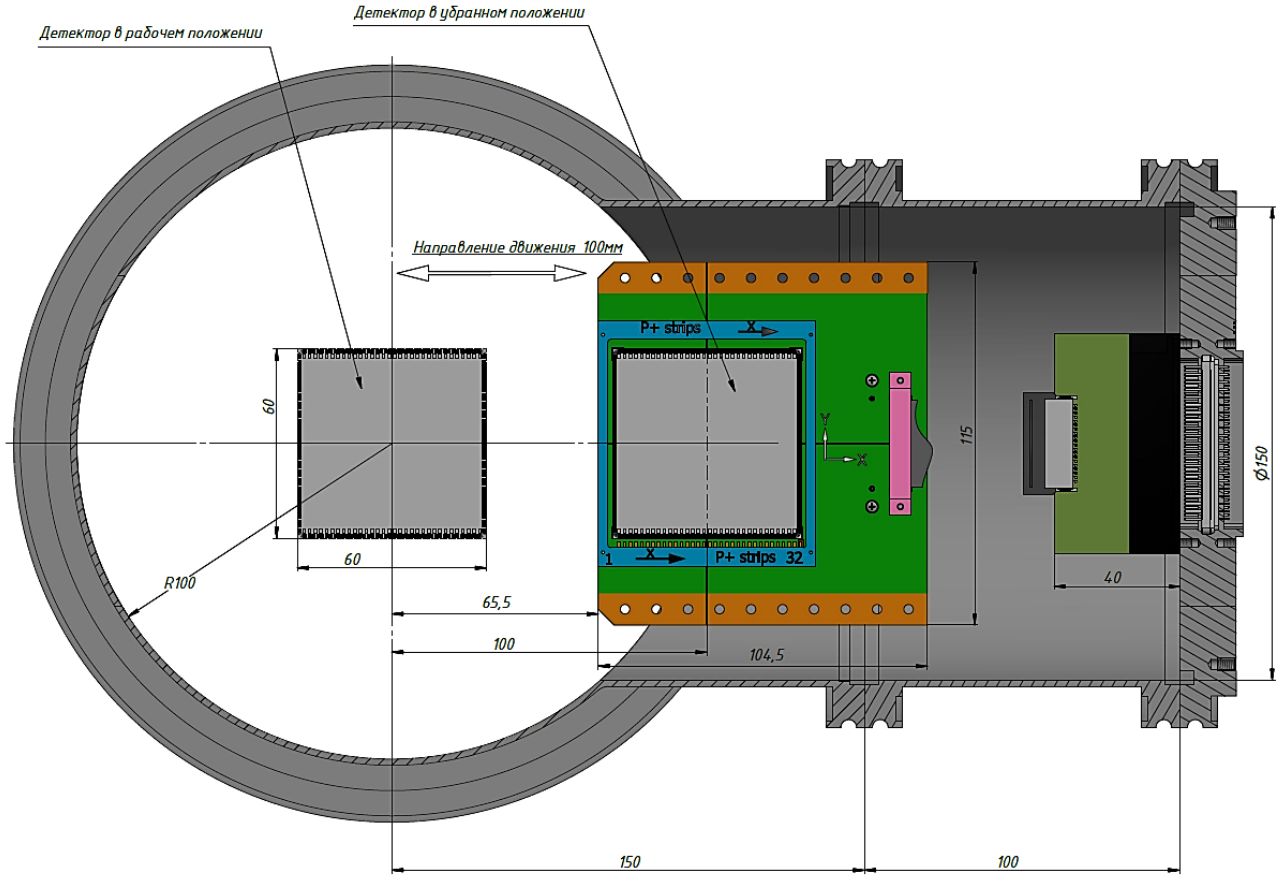


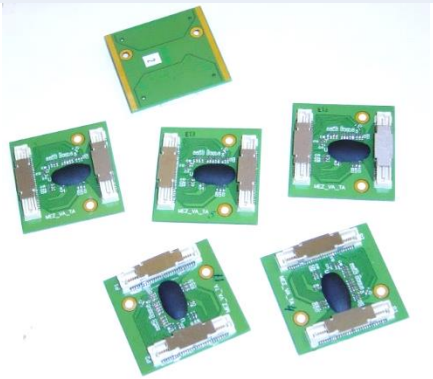
Forward Si Detectors
(3 planes)

beam direction

Beam profilometer DSSDs

Detector	DSSD (32x32 strips, thickness 175 μm)	
Ions	light ($_{6}C$ – $_{11}Ar$) Q = (96 - 866) fC	heavy ($_{36}Kr$ - $_{79}Au$) Q = (4 - 18) pC
FEE ASICs	VA163 + TA32cg2 (32 ch, dynamic range -750fC ÷ +750fC)	VA32HDR11+ TA32cg2 (32ch, dynamic range -35pC ÷ +25pC)
FEE PCBs	design in progress	
Mechanical support	design in progress	

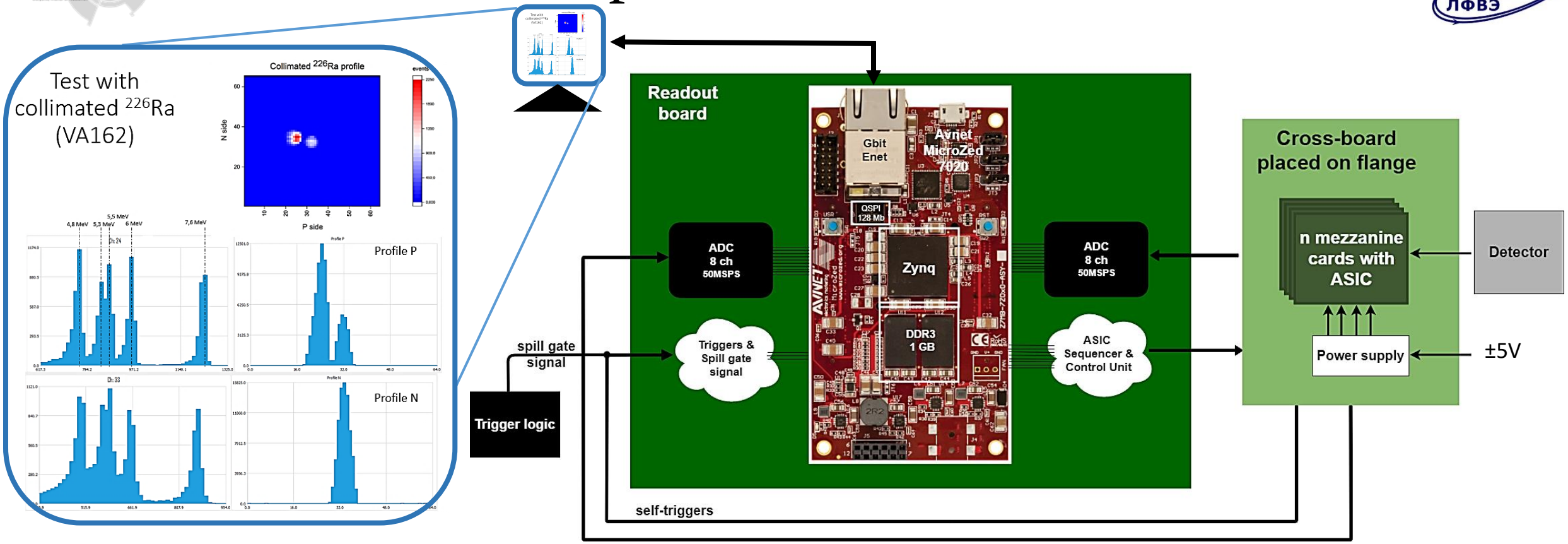




Two versions of mezzanine cards: VA32HDR11+TA32cg2 and VA163+TA32cg2 (IDEAS ASICs) might be plugged into FEE PCB.

The mechanical construction supports automatic removal of profilometer planes from beam zone to special branch pipe after beam tuning.

Beam profilometer DSSDs



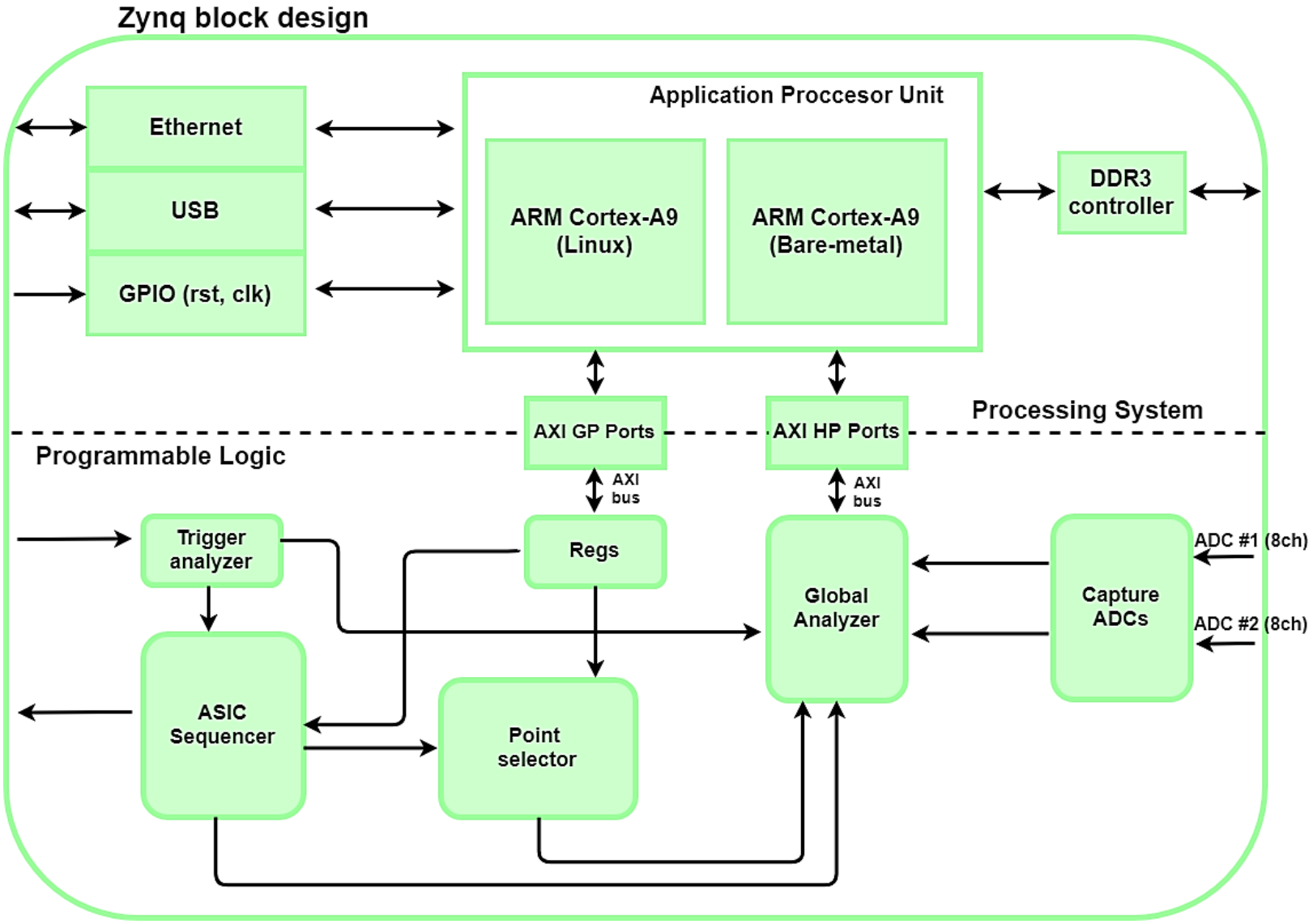
FEE for Beam profilometer DSSD:

- autonomous measurement system (without connection to BM@N DAQ);
- display information in the form of a 2D image and amplitude information;
- self-trigger counter = ion beam intensity;
- universal Readout board with changeable Mezzanine boards.

Beam profilometer DSSDs

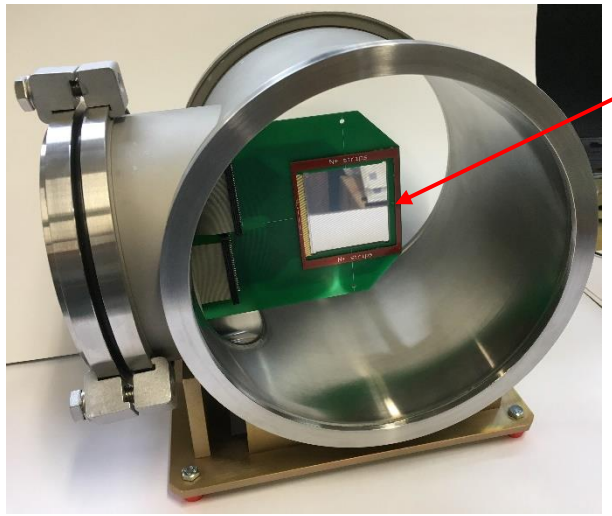
FEE for Beam profilometer DSSD:

- based on Xilinx Zynq SoC;
- configure ASICs by external trigger;
- capture ADC data and analyze;
- pedestal subtraction and zero suppression;
- send via Ethernet.

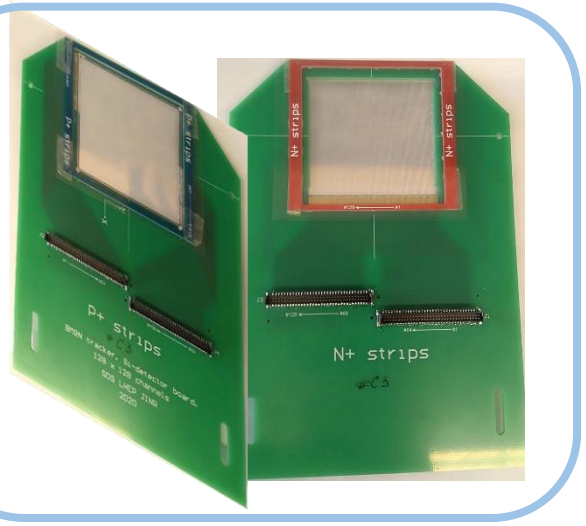


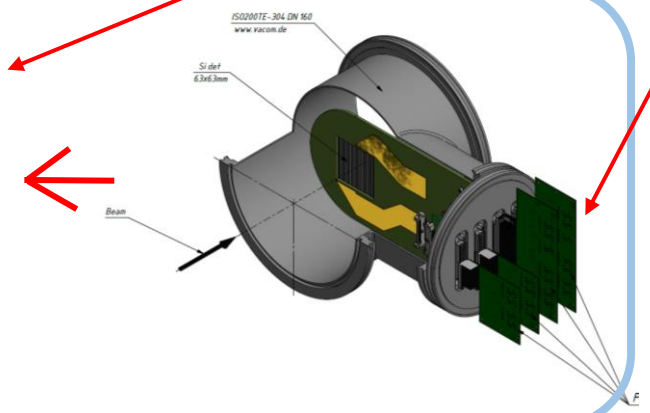
Beam tracker DSSDs

- Beam tracker is designed to determine the coordinates (X, Y) of incident “trigger ion”;
- self-trigger counter = ion beam flux/run;

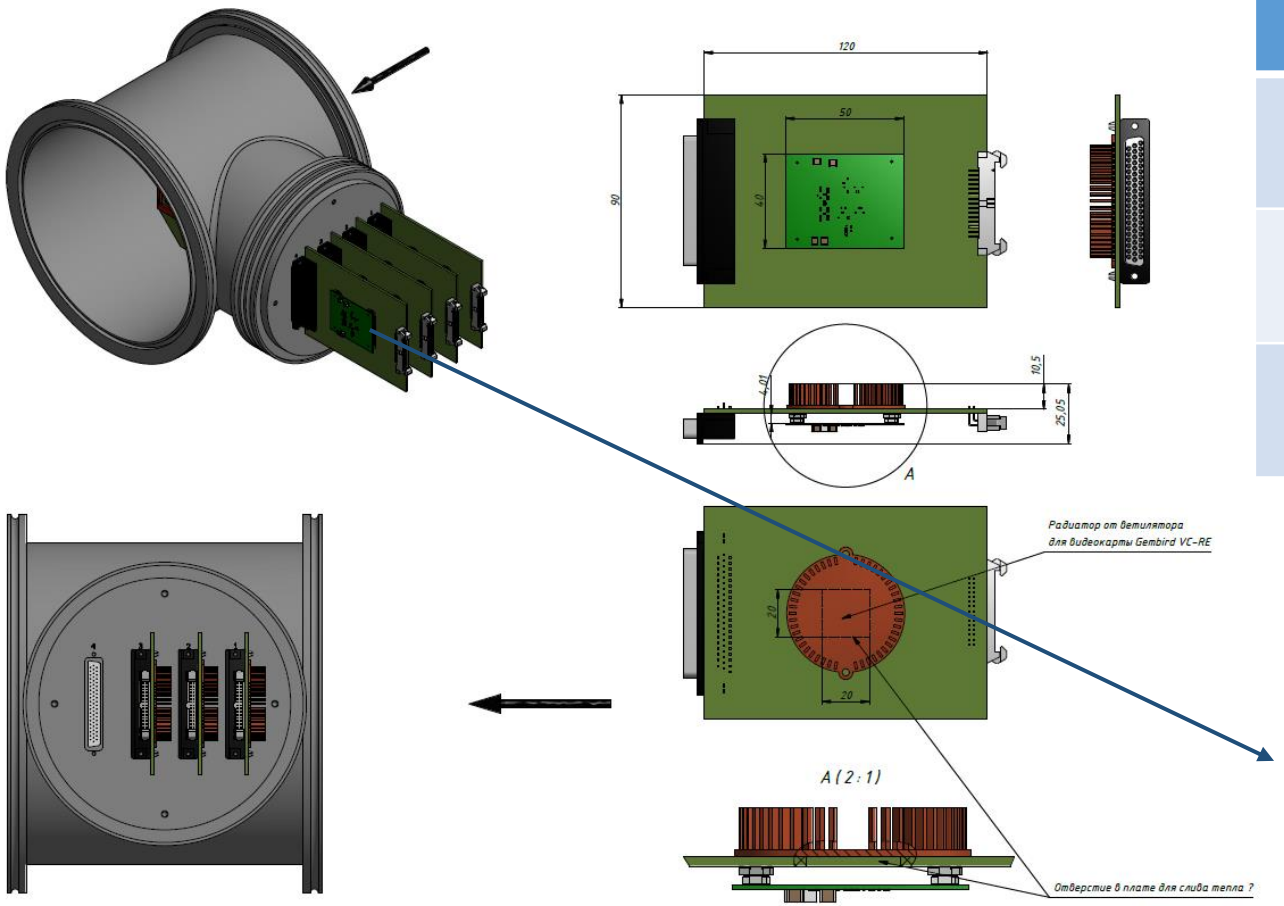


Detector	DSSD (128x128 strips, thickness 175 μm)	
Ions	light ($_{6}$C – $_{11}$Ar) Q = (96 - 866) fC	heavy ($_{36}$Kr - $_{79}$Au) Q = (4 - 18) pC
FEE ASICs	VA163 + TA32cg2 (32 ch, range -750fC ÷ +750fC)	VATA64HDR16.2 (64ch, range -20pC ÷ +55pC)
FEE PCBs	PCB board for two ASIC versions	
Mechanical support	flange is ready	

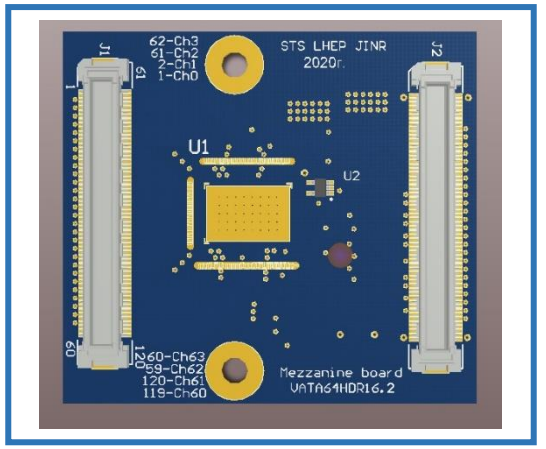




Beam tracker DSSDs



Ions	IDEAS ASIC	Shaping time
light ($_{6}C$ – $_{11}Ar$)	VA163	500ns
heavy ($_{36}Kr$ - $_{79}Au$)	VATA64HDR 16.2	50/100/150/300ns
Compatibility ASIC shaping time with Global Trigger is under discussion		

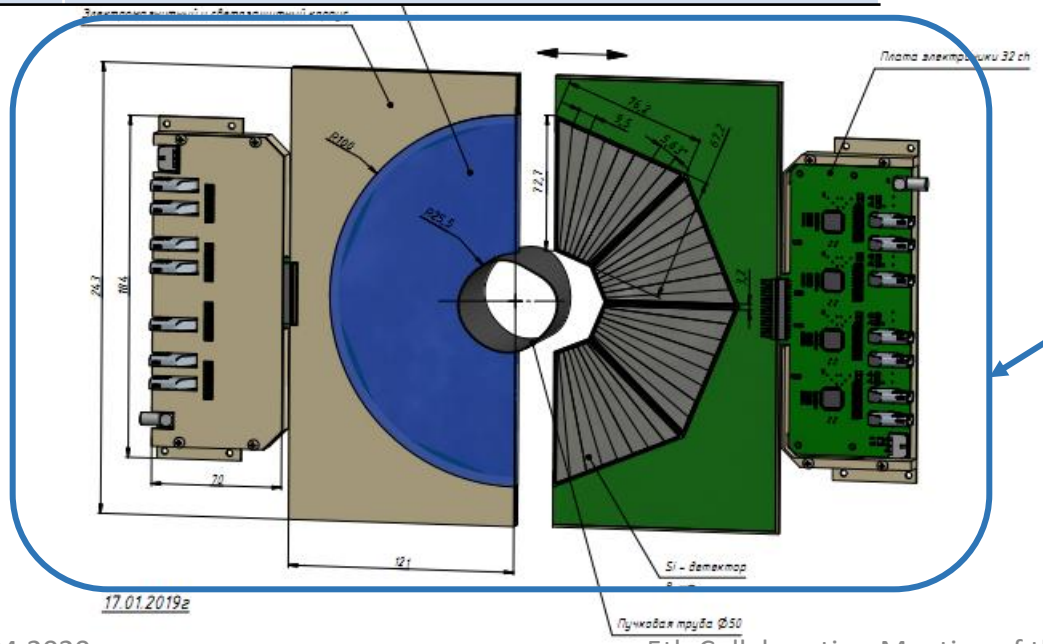


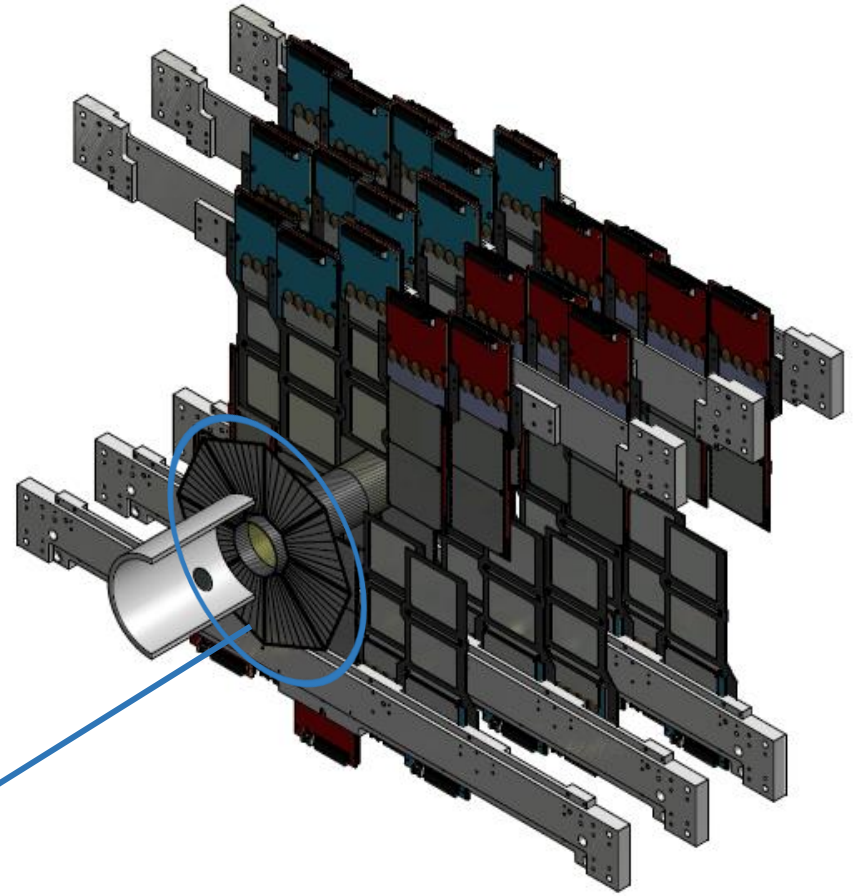
A PCB design of a mezzanine card with one VATA64HDR16.2

VA163 and VATA64HDR16.2 have different configuration sequencer and readout format.

Si-Forward Multiplicity trigger

Detector	SSSD (8 silicon strip trapezoid single side detectors, thickness 525 µm)
FEE ASICs	AST1.2 (8 ch, dynamic range ±50 fC)
FEE PCBs	upgrading
Mechanical support	design in progress

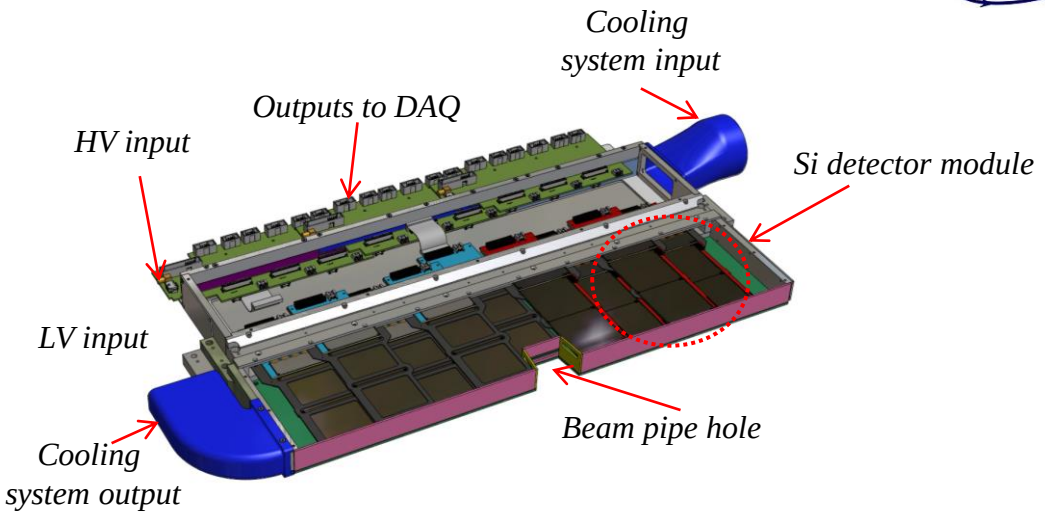


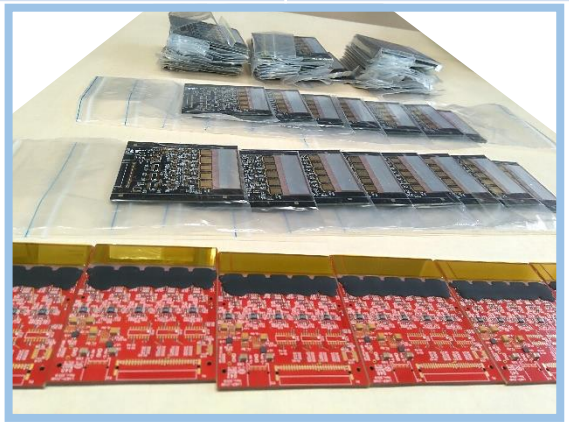


Multiplicity trigger in front of Forward Silicon Detectors

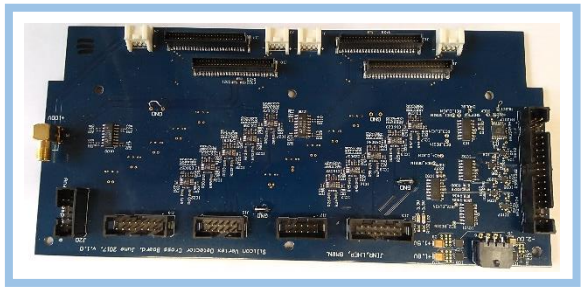
Forward Silicon Detectors

Detector	DSSD (640 (p^+) x 640 (n^+)) strips, thickness 300 μm)
FEE ASICs	VATAGP7.1 (128 ch, dynamic range ±30 fC)
FEE PCBs	1 PCB board = 5 x VATAGP7.1
Mechanical support	✓
Summary	Ready to test and assembly





FEE boards for p^+ and n^+ Si sides



Cross-board for two Detector modules

Previous configuration of Si plane

FEE Si-subsystem details

Si subsystem	Planes	$\frac{\text{Channels}}{\text{Si} - \text{plane}}$	Cross-boards	FEE boards	ASICs
Beam profilometer	2	32x2	2	4	4 (4xADC ch)
Beam tracker	3	128x2	3	12	12 (12xADC ch)
Multiplicity trigger	1	64	-	2	8
Forward Silicon Detectors	3	12800	10 for three modules	84	420 (420xADC ch)
		17920			
		23040	6 for two modules		
		Total = 53760			

Conclusion

- FEE for Beam profilometer:
  - Two versions of FEE design (for light ions and for heavy ions (high-priority)) based on IDEAS ASICs VA163+TA32cg2 and VA32HDR11 +TA32cg2, respectively in progress;
  - Design of Readout board (based on Xilinx Zynq SoC and ADCs) and Cross-board in progress;
  - Design of Silicon Sensor PCB in progress.
- FEE for Beam tracker:
  - Two versions of FEE design (for light ions and for heavy ions (high-priority)) based on IDEAS ASICs VA163 and VATA64HDR16.2, respectively in progress;
  - Silicon Sensor PCB designed and produced;
  - Design of Cross-board in progress.
- FEE for Multiplicity trigger:
  - FEE is based on existing design (ASIC AST1.2).
- FEE for Forward Silicon Detector:
  - FEE boards are based on existing design:
    - 100 FEE boards (50 for p+ side/ 50 for n+) produced and assembled with Pitch Adapters;
    - 15 FEE boards (n+) are full assembled and ready for testing.
  - Cross-boards for two and three modules are being designed.