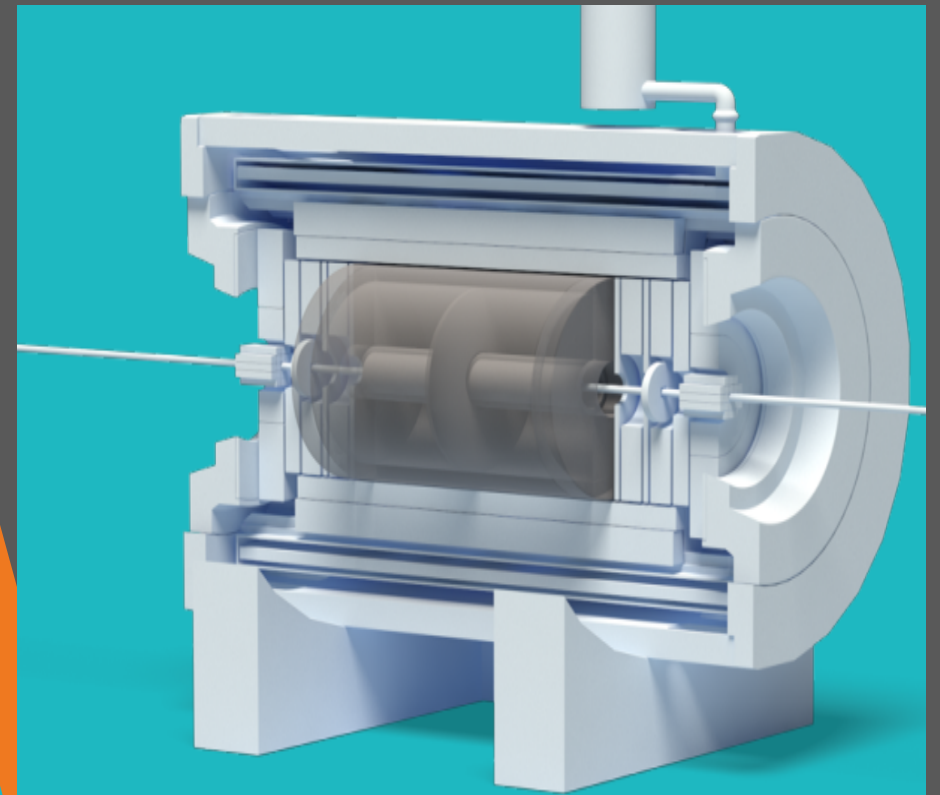
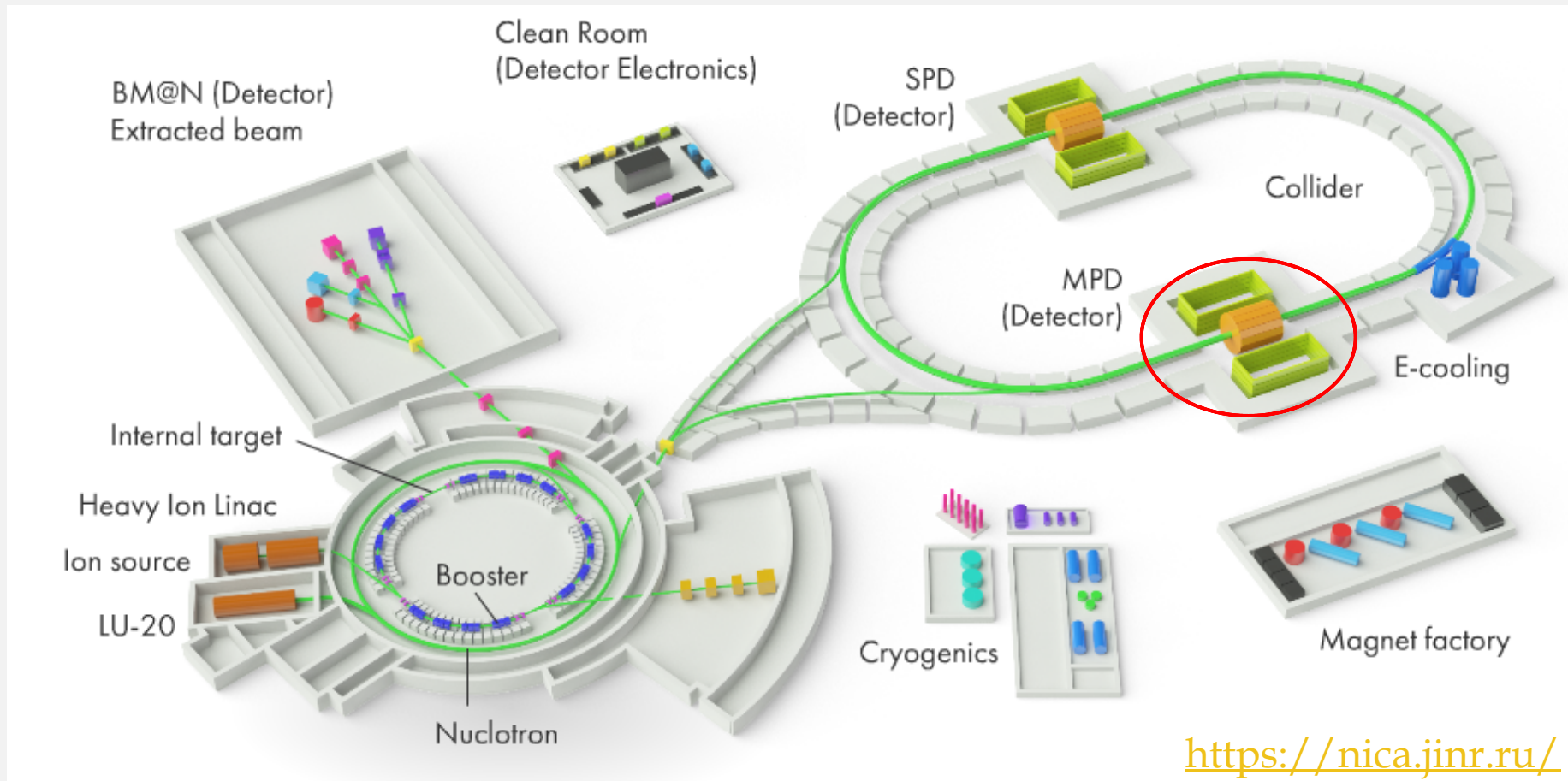


Front-End Electronics development for TPC/MPD detector of NICA project

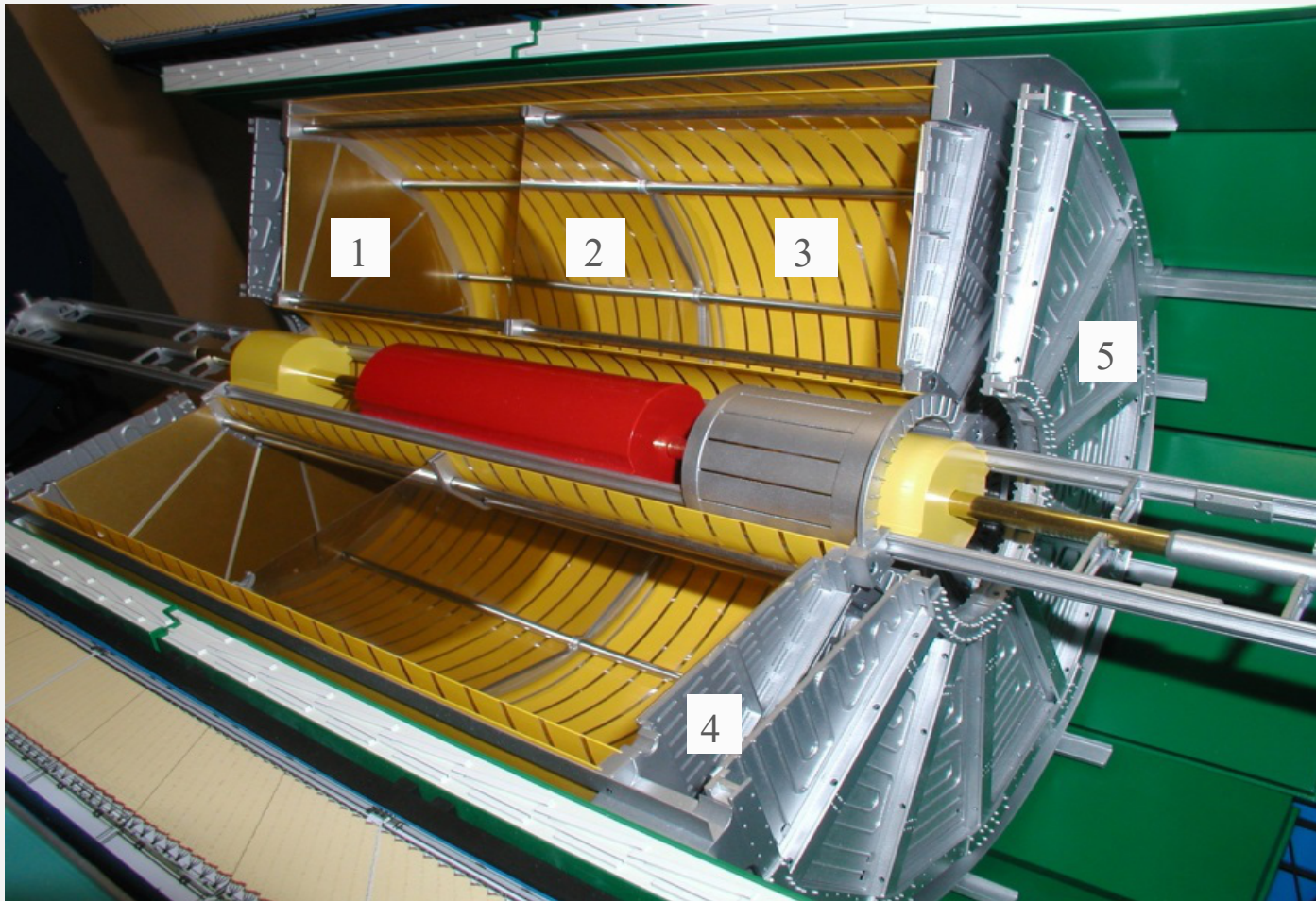
*Stepan Vereschagin, on behalf of the
TPC/MPD group, LHEP, JINR*



NICA Complex



Central part of the MPD mock up with TPC cut



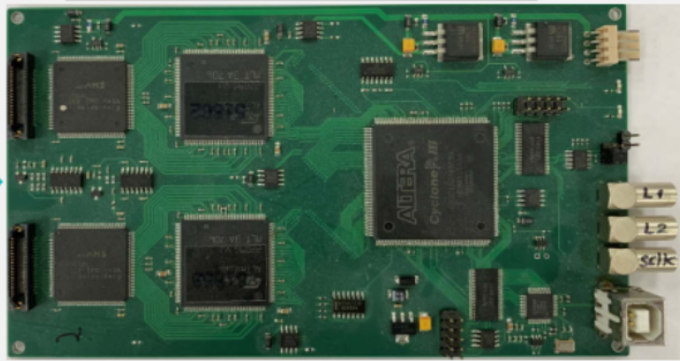
The TPC/MPD design requirements:

- The overall acceptance: $\eta < 1.2$
- The momentum resolution for charged particles is under 3% in the transverse momentum range $0.1 < p_t < 1 \text{ GeV}/c$
- Two-track resolution is of about 1 cm
- Hadron and lepton identification by dE/dx measurements - with a resolution better than 8%
- Data flow rate up to 100 GBps at trigger rate 7 KHz

- 1- MWPC;
- 2 - HV electrode;
- 3 - Field cage;
- 4 - FEE position;
- 5 - End cap thermal screen.

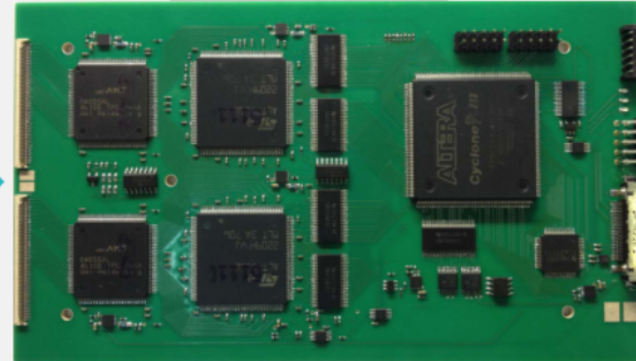
TPC/MPD FEC evolution

ALTRO FEC prototype



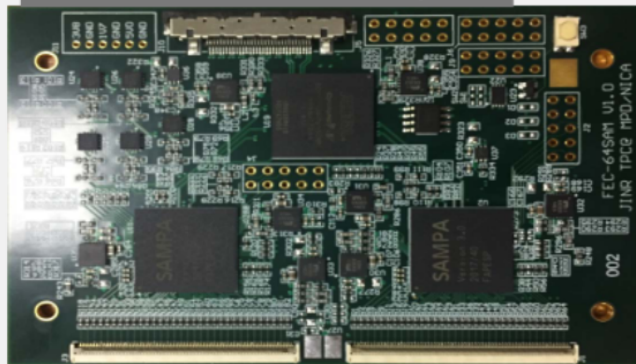
100x170
mm²

ALTRO FEC



95x167
mm²

SAMPA FEC prototype



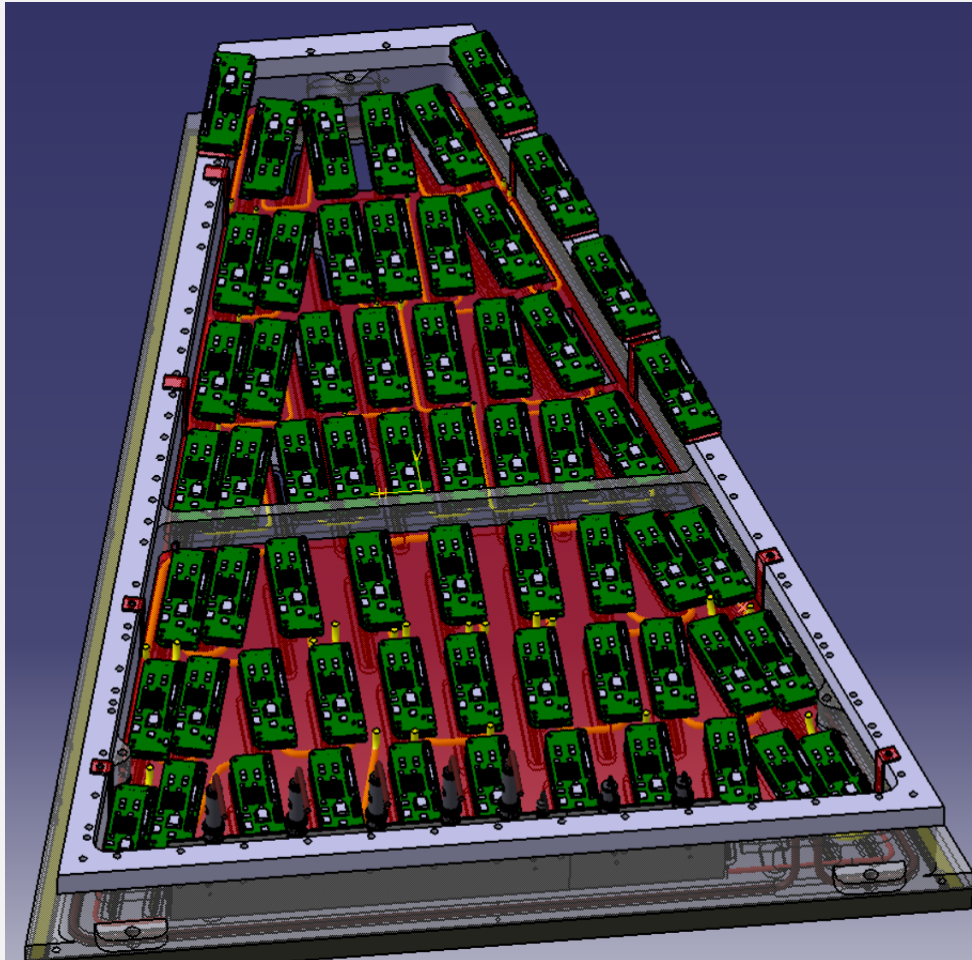
One
PCB
form factor
65x95
mm²

SAMPA FEC



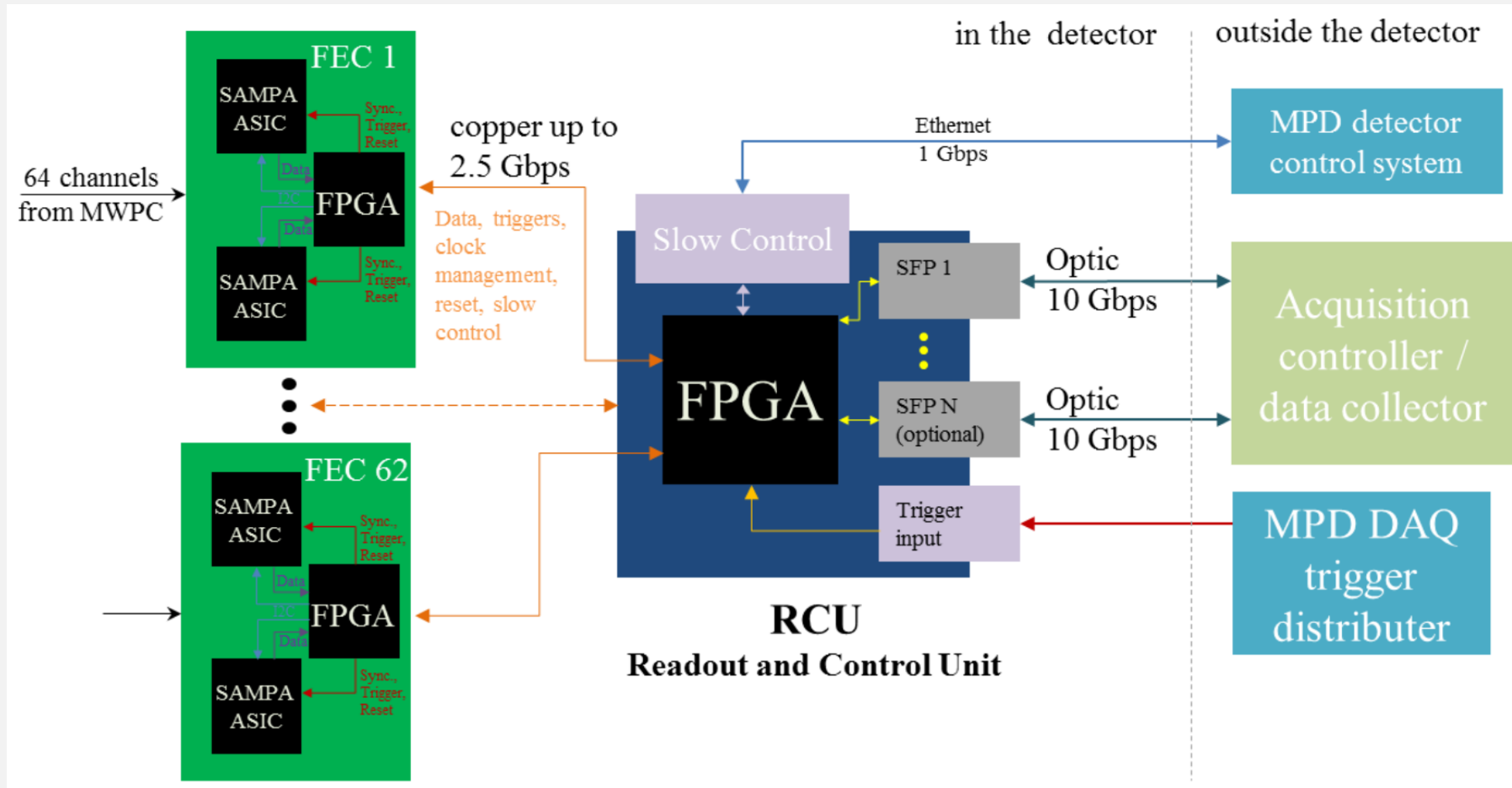
Two
PCB
form factor
28x91
mm²

Concept of electronics integration on ROC



Design goal is to reduce the amount of material at the TPC endcaps and to distribute it evenly. That was achieved with double PCB card form factor.

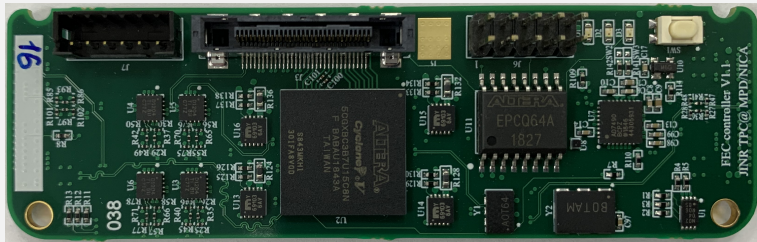
Block diagram of one chamber readout (1/24 TPC)



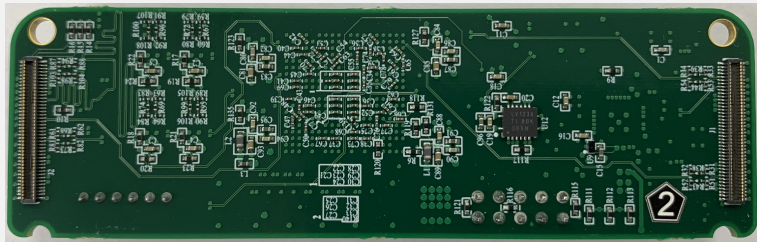
FEE status

- Concept of the TPC data readout system has been determined.
- Actual size FEC (28x91 mm²) satisfying integration demands has been designed, 68 FECs produced and tested. Another 35 FECs where ordered.
- RCU prototype based on Arria 10 development board has been prepared (firmware and transition cards for connection with FECs).
- Cable assemblies for multichannel gigabit communication have been designed, produced and tested.
- Half-ROC testing system (2048 ch.) has been prepared. Testing is going.
- The design of the first version of the RCU finished. PCB will be ordered soon.

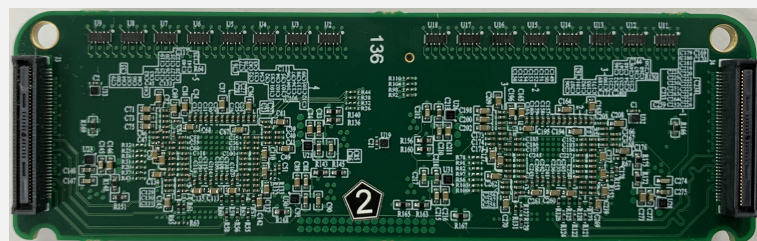
The view of 64-channel FEC



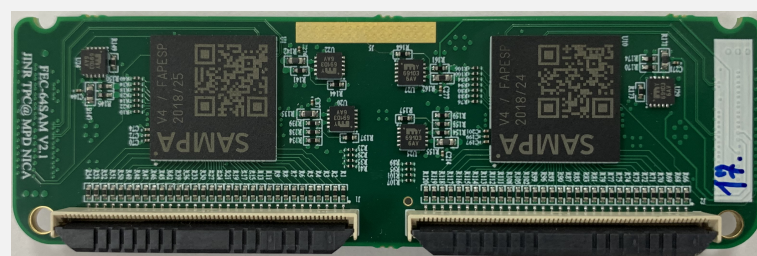
FEC controller
Top view



FEC controller
Bottom view

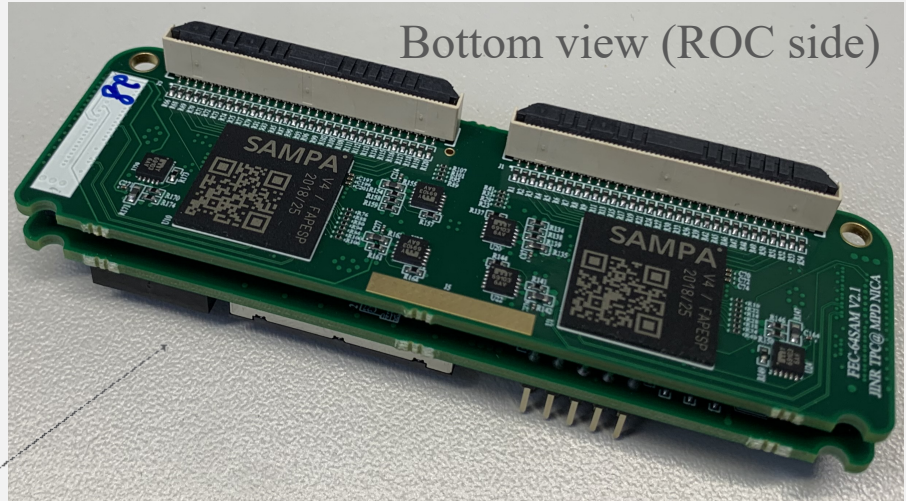


FEC assembly
view

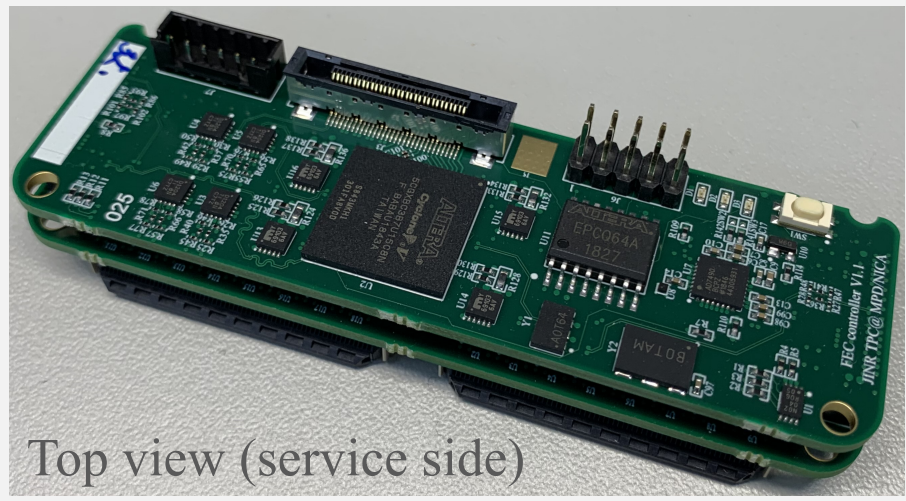


SAMPAs
FEC
Top view

SAMPAs
FEC
Bottom view

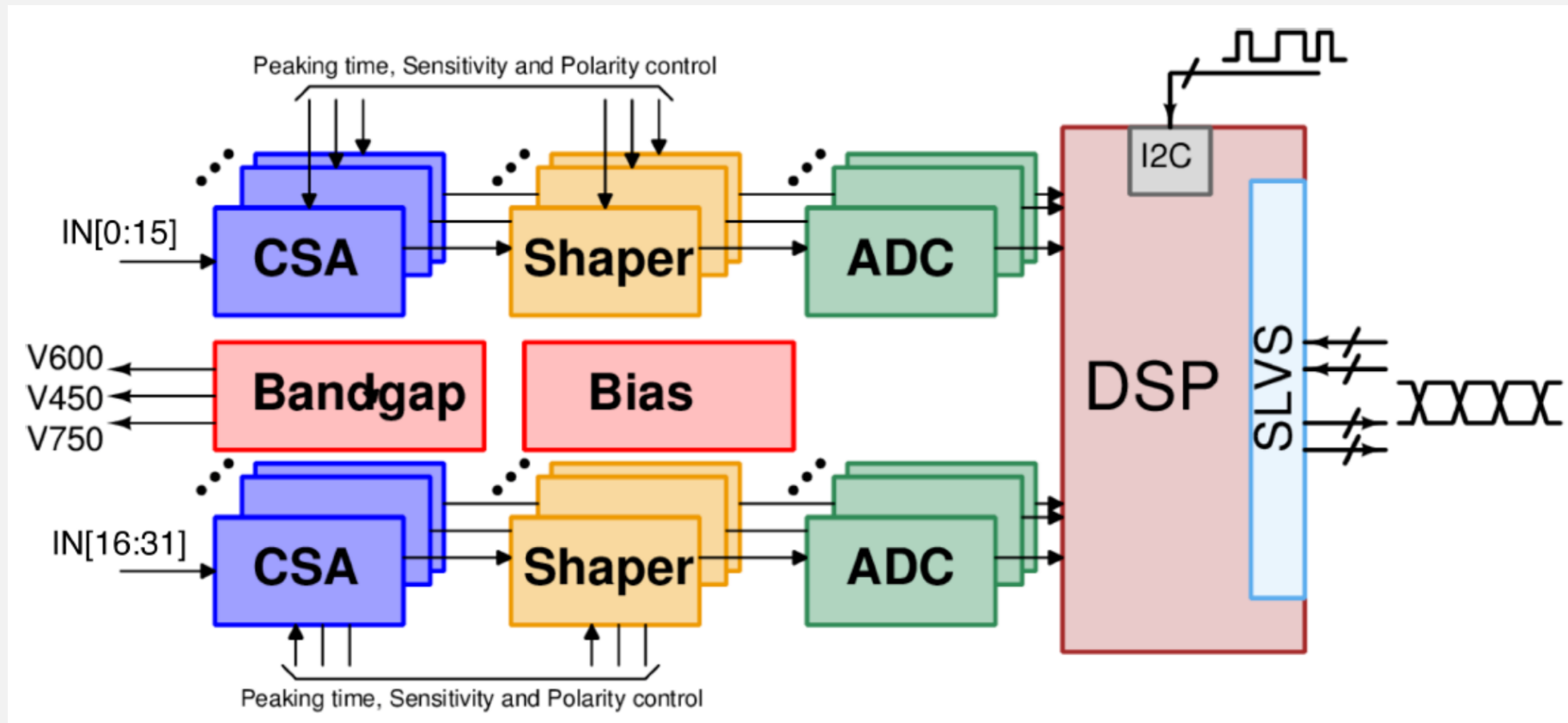


Bottom view (ROC side)



Top view (service side)

SAMPA ASIC: the core of FEE

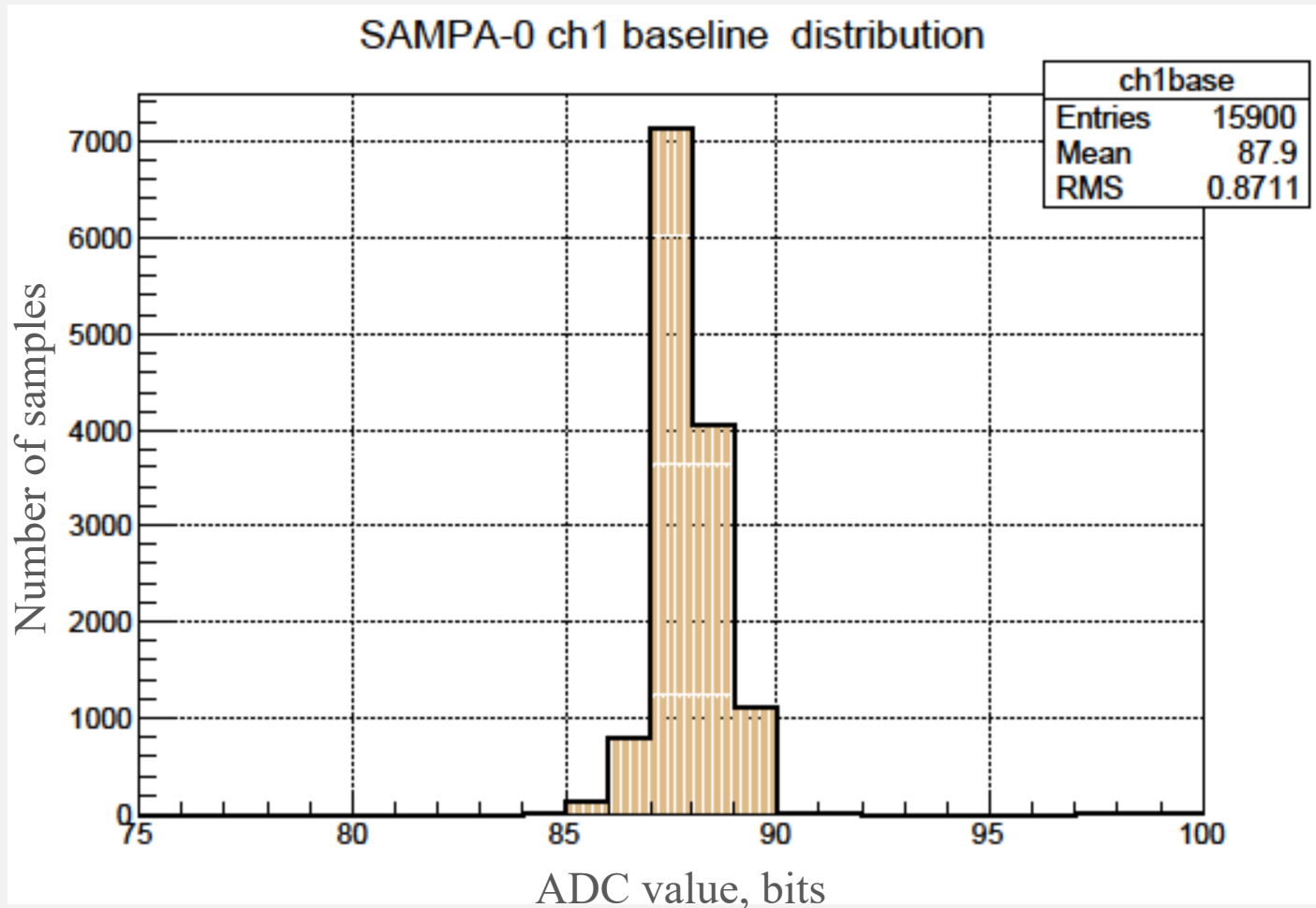


[1] J. Adolfsson, et al., SAMPA chip: the new 32 channels ASIC for the ALICE TPC and MCH upgrades, JINST 12 (04) (2017) C04008.

FEC main parameters and functionality:

- The total number of registration channels: 64
- Input signal dynamic range: 100 fC
- ADC resolution: 10 bit
- ENC: less than $1000e^-$
- SAMPA chips configured and controlled via FPGA
- Readout serial interface: up to 2.5 Gbps
- *Double-PCB FEC provides opportunities for possible upgrade of the card readout.*
- *Transfer of data and trigger signals was realized with the same high-speed serial interface.*
- *16 values of currents, voltages and board temperatures are controlled with ADC.*
- *Onboard circuit and embedded protection functionality against SEU are provided.*
- *Remote system update for FEC firmware was provided.*

Typical noise distribution of a SAMPA channel

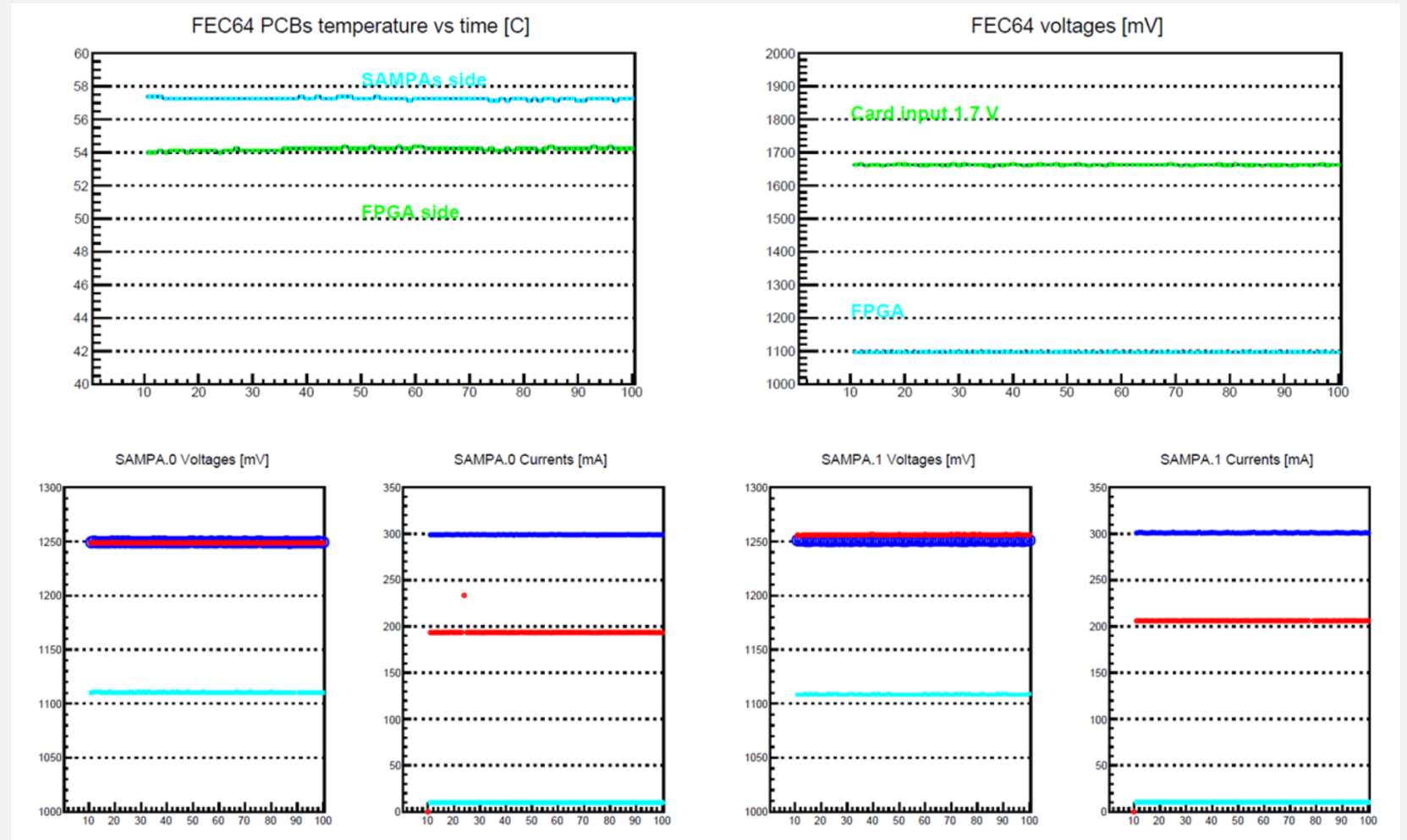


1 ADC LSB = $670 e^-$

Measurement was done
without connection with
ROC

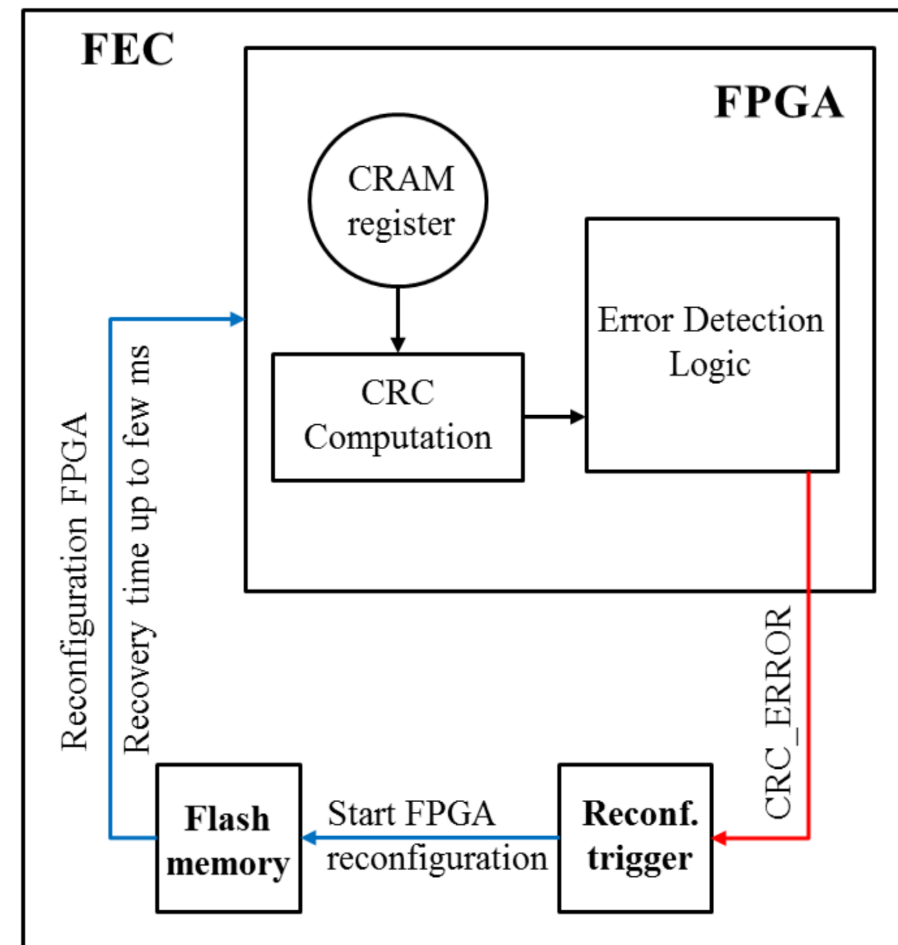
FEC slow control data

16 values of voltages, currents and temperatures are continuously measured on each FEC. The FPGA control state machine processes the data of the ADC and can form an interrupt vector.

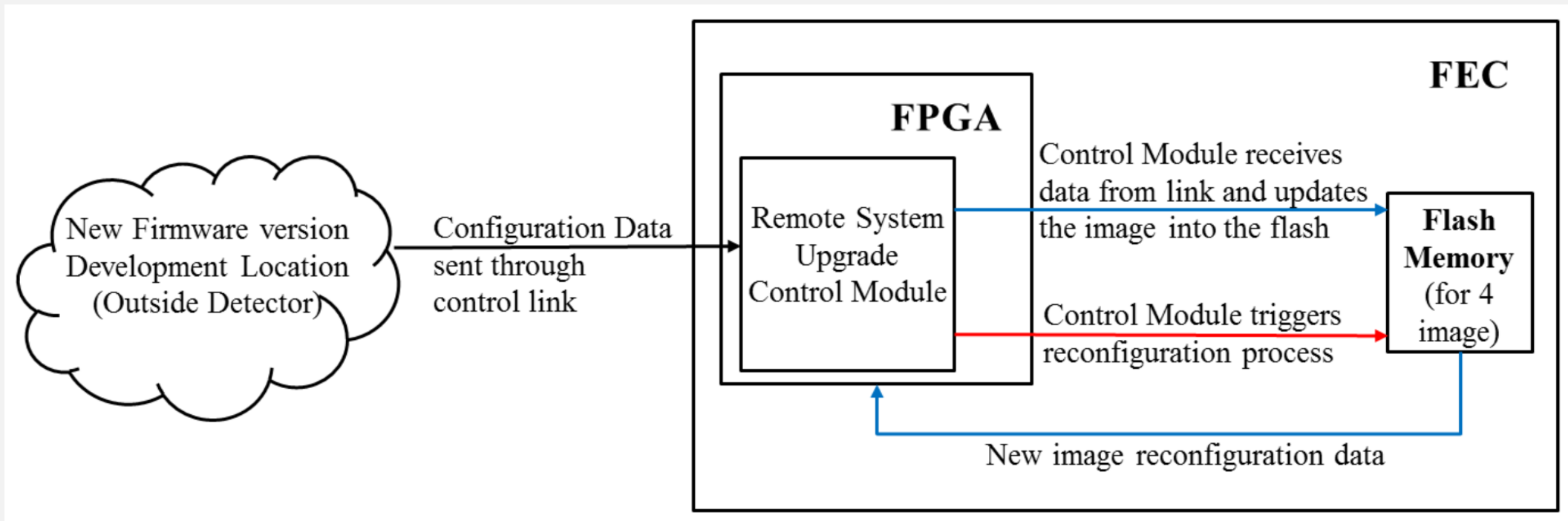


SEU recovery circuitry

- Due to the FECs operation in a radiation environment, it is reasonable to have mechanisms to protect the FPGA firmware from SEU.
- The CRC circuit can detect all single-bit and multi-bit errors within the FPGA configuration memory.
- In the case of detecting a firmware error, the onboard trigger initiates the reconfiguration process from the external flash memory.

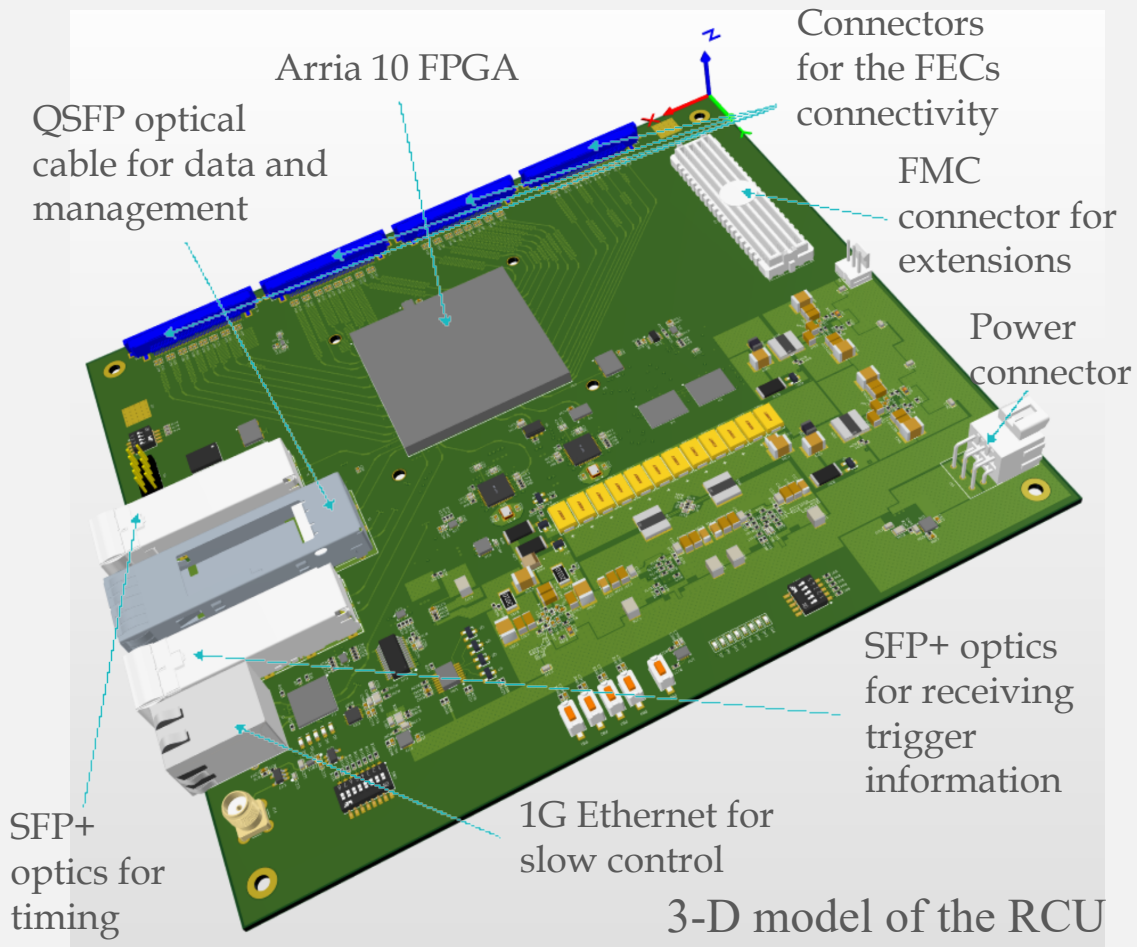


Remote firmware update



Anticipating limited access to the electronics installed on the detector, it is desirable to provide a remote update of the firmware. Remote firmware upgrade feature was implemented into the FPGA design of the FEC controller.

Key features of the RCU:



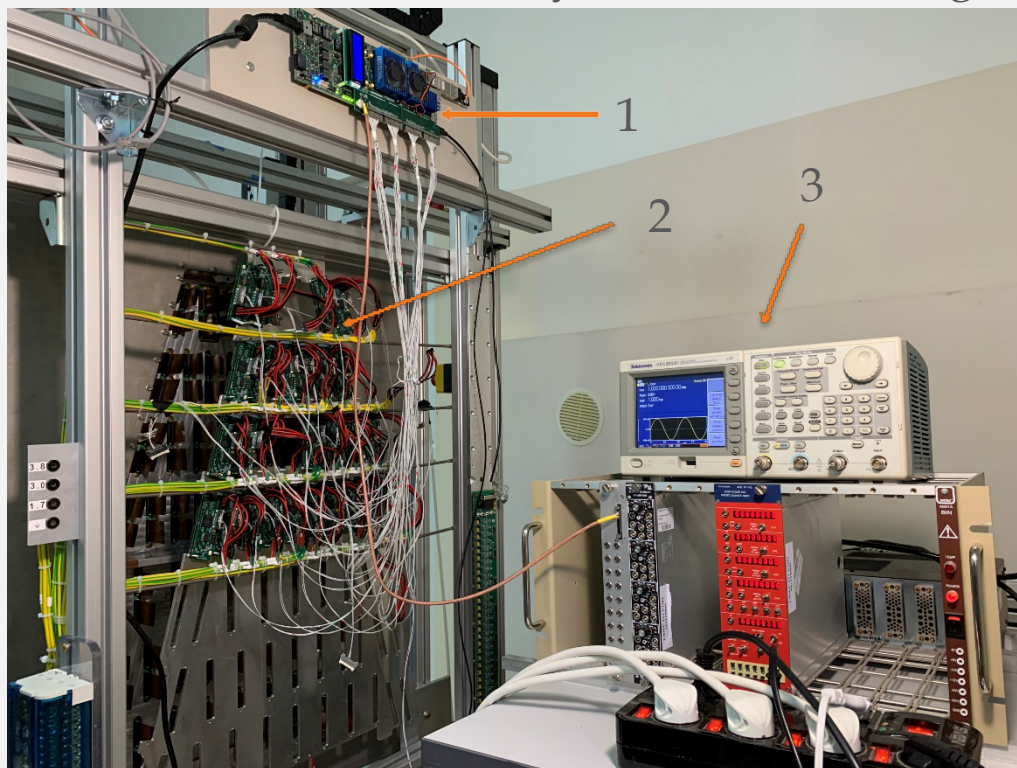
Flow Summary	
Flow Status	Successful - Fri Sep 25 14:47:14 2020
Quartus Prime Version	19.4.0 Build 64 12/04/2019 SC Pro Edition
Revision Name	RCU_A10
Top-level Entity Name	top
Family	Arria 10
Device	10AX115S2F45I2SG
Timing Models	Final
Logic utilization (in ALMs)	30,152 / 427,200 (7 %)
Total registers	64031
Total pins	453 / 960 (47 %)
Total virtual pins	0
Total block memory bits	30,369,964 / 55,562,240 (55 %)
Total RAM Blocks	1,894 / 2,713 (70 %)
Total DSP Blocks	2 / 1,518 (< 1 %)
Total HSSI RX channels	70 / 72 (97 %)
Total HSSI TX channels	70 / 72 (97 %)
Total PLLs	81 / 144 (56 %)

The RCU firmware design compilation flow summary.

- Intel 20nm FPGA Arria 10 was selected as a base of data readout.
- Embedded 72 transceivers are sufficient to implement the RCU on a single FPGA.
- ALMs and memory resources allow implementing all the necessary data transfer system algorithms
- Excess FPGA resources allow further system improvement

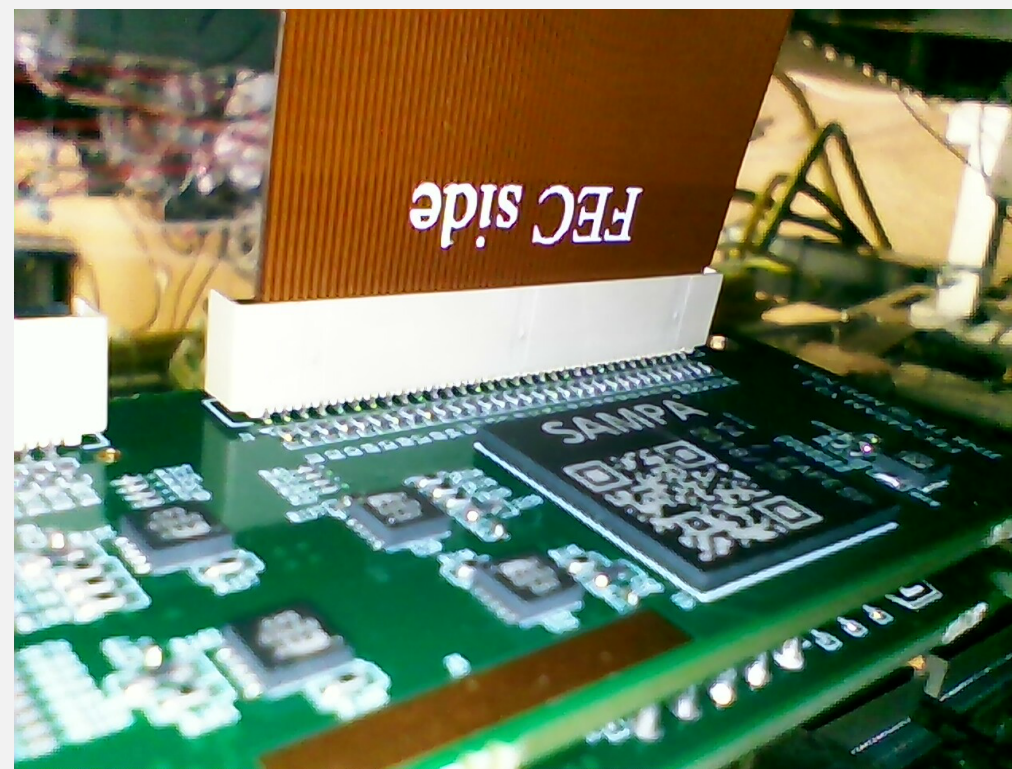
Half-ROC (2048 ch. \sim 2% of full TPC) readout system

Half-ROC readout system under testing



- 1) RCU prototype;
- 2) FECs installed on the ROC;
- 3) Trigger signal generation system;

FEC flat cable connection with ROC



Visual inspection of the FEC connection

Conclusion

- ◆ The FEE for the TPC has been designed on the base of the ASIC SAMPA and Intel FPGAs with high-speed serial links.
- ◆ The FECs form factor of 28x91mm² conforms to the detector design constraints.
- ◆ 68 actual size FECs have been produced and tested. Another 35 ones where ordered.
- ◆ RCU design including PCB layout and FPGA firmware was finished. Production of the first sample is scheduled for the end of this year.
- ◆ TPC readout system prototype testing is going. The system is considered as a starting point for full-featured TPC readout system design.

Thank you!