Fast data-driven readout system for the BM@N STS

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"RFBR grants for NICA",
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VB LHEP, JINR, Dubna

RUSSIAN FOUNDATION FOR BASIC RESEARCH

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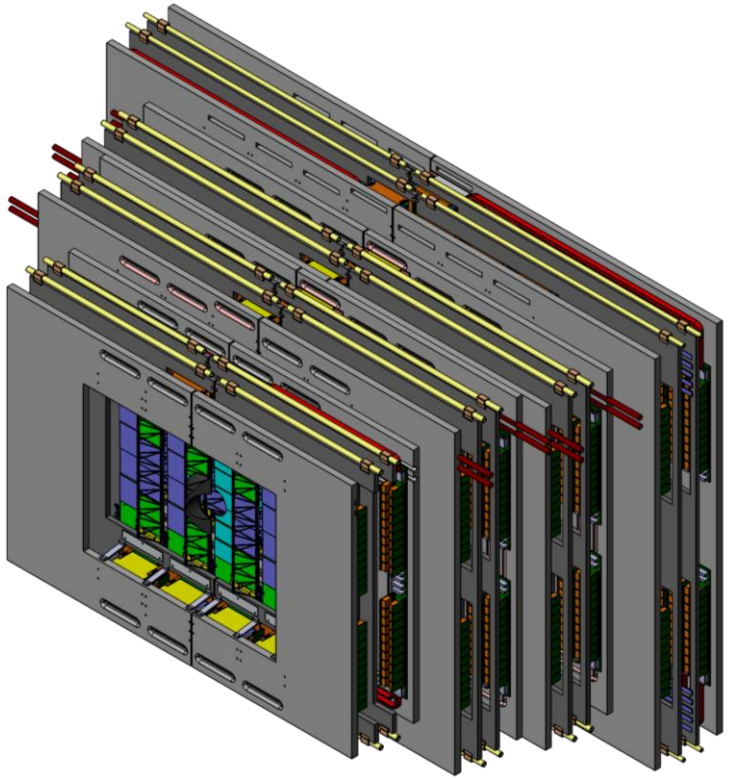
Work supported by RFBR 18-02-40047 grant

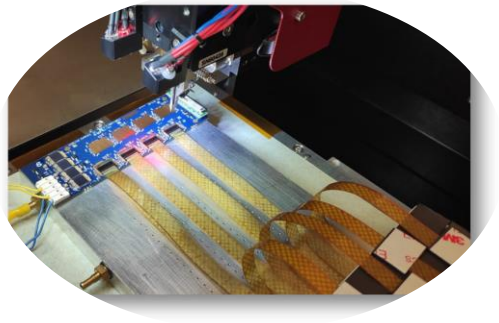
Silicon Tracking System of BM@N



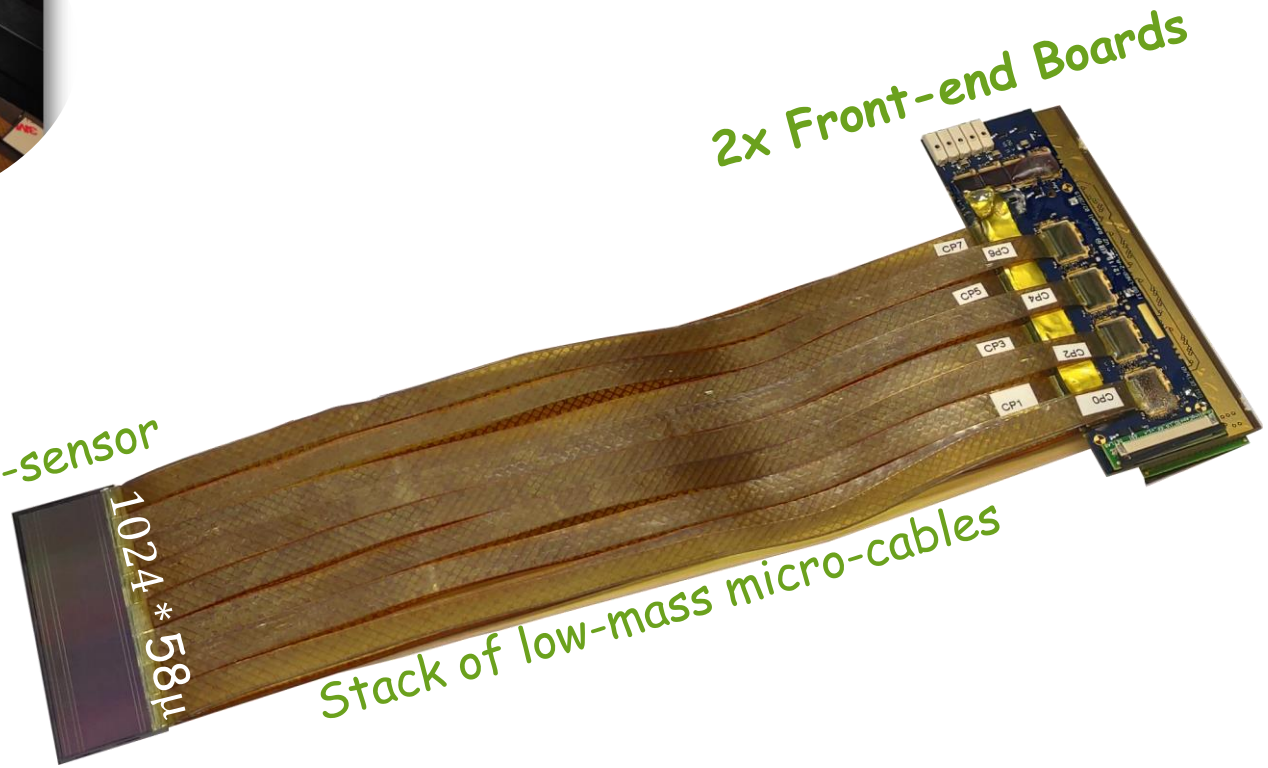
BM@N STS

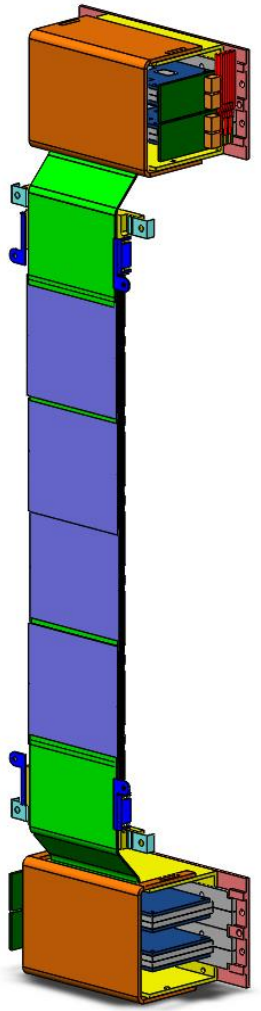
- 4x Stations with 292 STS modules with double-sided microstrip silicon sensors
- Hit spatial resolution ~25 µm
- ~600 k. self-triggered channels with a free-streaming readout
- ~15 kW Power consumption

STS module

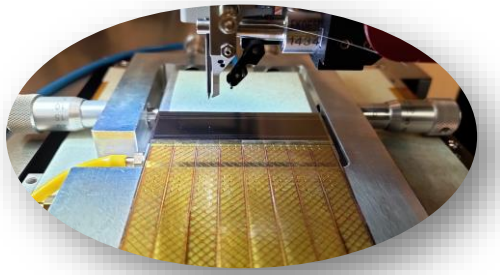


Photos of the module assembly



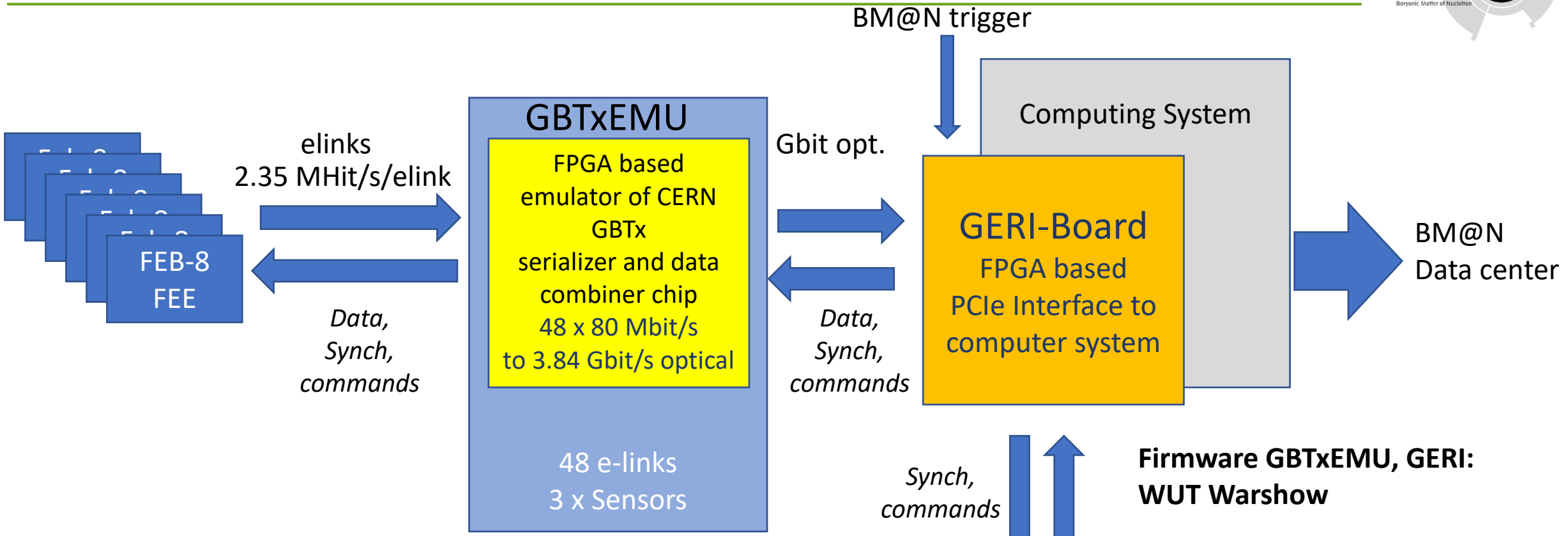


STS ladder



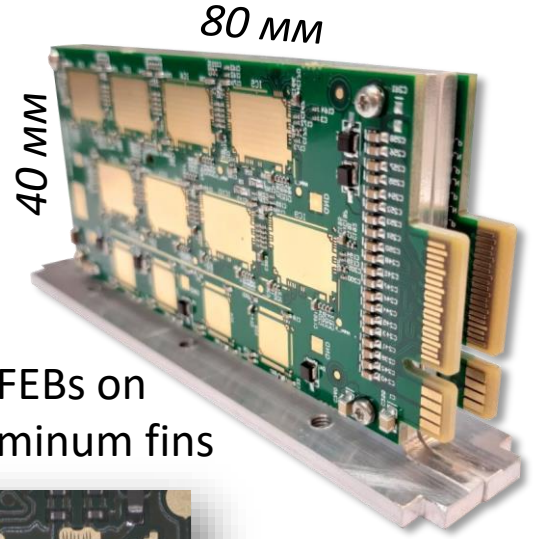
More details about the module assembly are presented in the talk by N.Sukhov

Readout electronics of BM@N STS



Hardware developments: GSI Detector Lab, JINR, MSU
Software: JINR, MSU

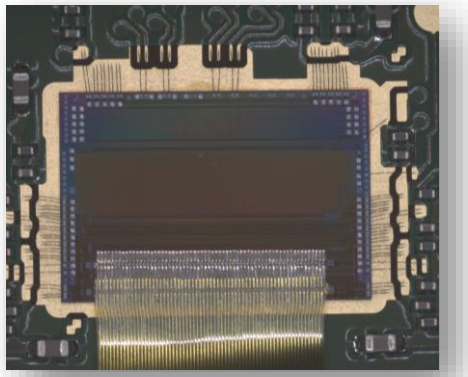
Front-end boards



2* FEBs on aluminum fins

One FEB provides the following interfaces:

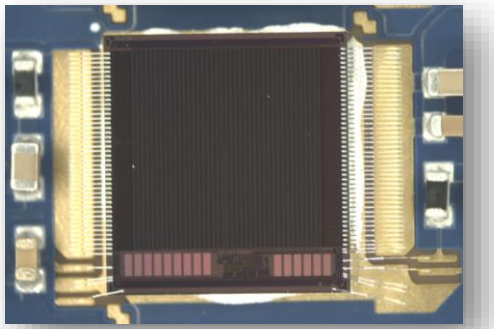
- **1x Down link – 40 Mb/s**
- **1x Clock - 40 MHz**
- **8x Up links – 80 Mb/s**



8x STS-XYTER ASICs

Self-triggered readout provides digitized hits:

- 5bit pulse height
- 14bit timestamp
- Hit frame: 30 bits



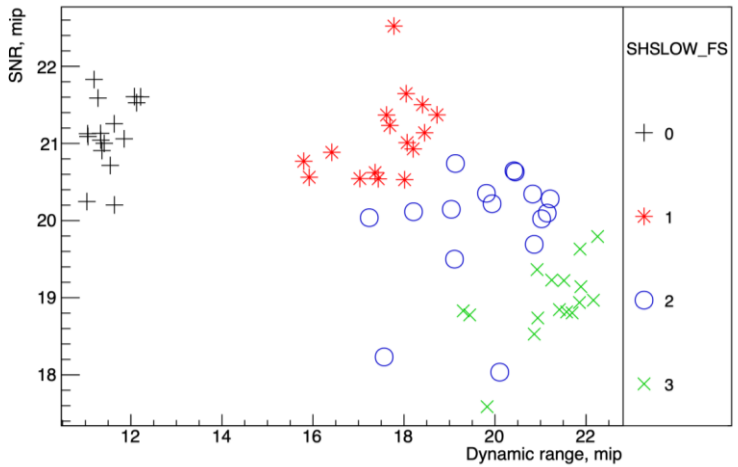
4x skimming LDOs

- up to 2.5 A at 1.2 V for the analog part
- up to 2.3 A at 1.8 V for the digital part

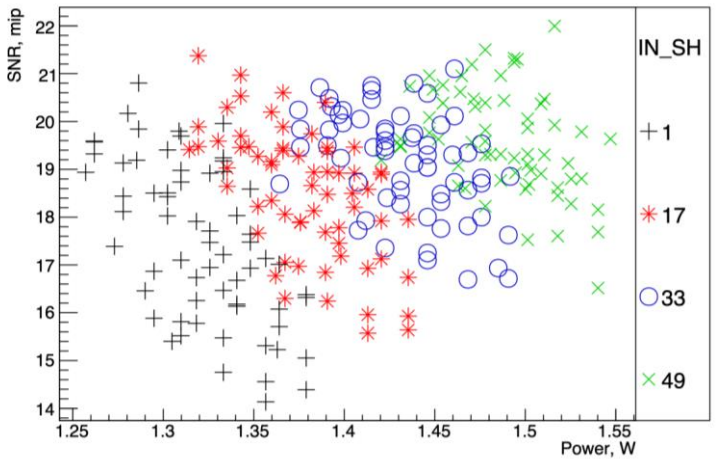
Signal is transmitted via AC –coupled LVDS links
~ 10 m electrical connection to GBTxEMU

FEB design: JINR and MSU

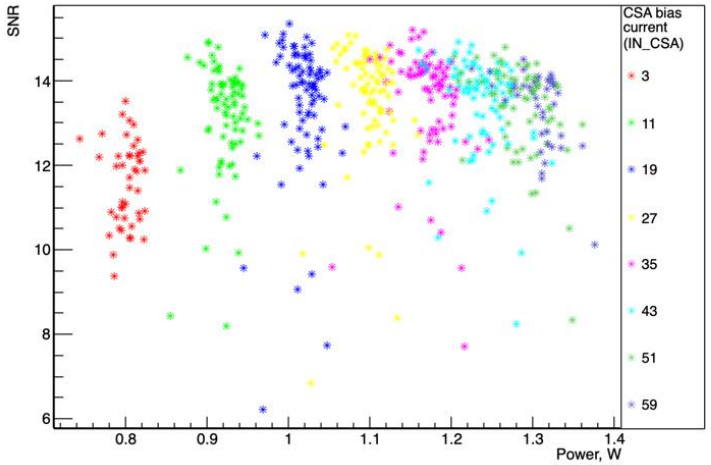
Certification of the STS-XYTER ASICs



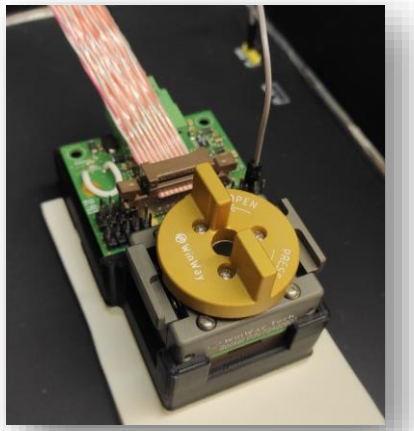
Signal to noise ratio and dynamic range dependence on the slow shaper shaping time



Signal to noise ratio and power consumption dependence on the fast shaper bias current register value



Signal to noise ratio and power consumption dependence on the CSA bias current register value

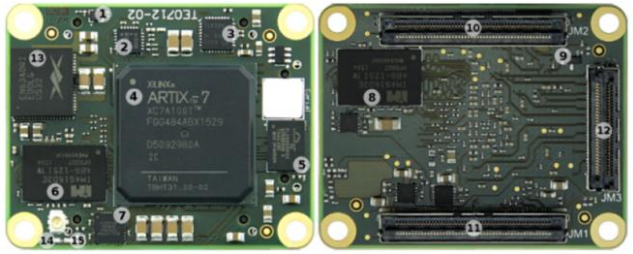


Pogo-pin test circuit

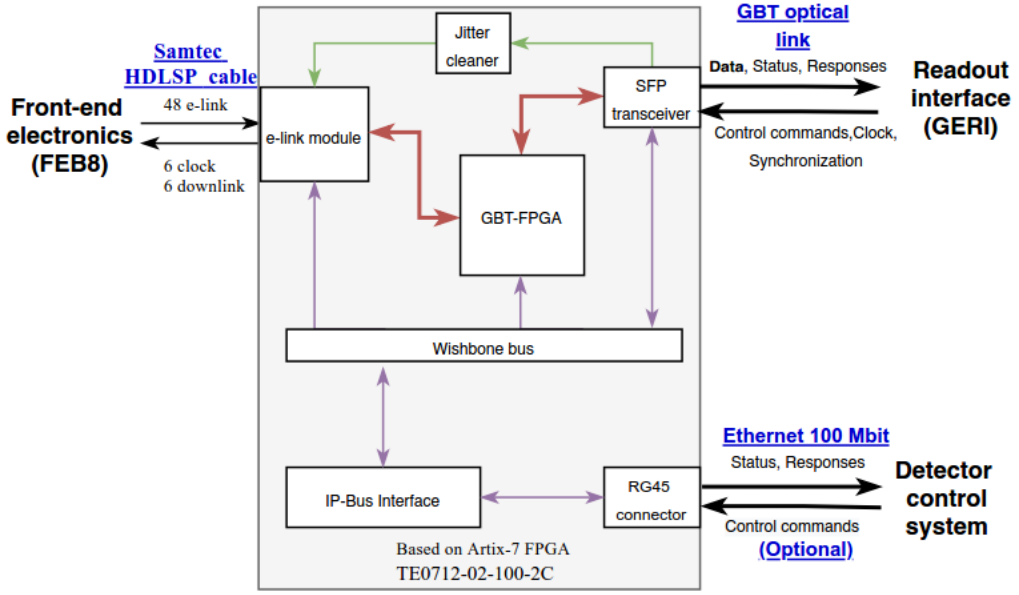
STS-XYTER has a number of variable settings for both analogue and digital parts. To optimize these settings, one needs to measure key characteristics of the ASIC in every point of multidimensional phase space of its parameters and to choose an optimal operation point

Tests of analogue part: MSU

GBTxEMU



Trenz TE0712-02-100-2C platform with Xilinx Artix-7



- Emulates functionality of GBTx ASIC on FPGA
- Platform: Trenz TE0712-02-100-2C
- Xilinx Artix-7 FPGA
- 48 up links with 80 Mb/s data rate
- 6 down links and 6 clock links
- 6 Gbps optical link with a payload bandwidth of 4.375 Gbps
- Control interface (optional): IPbus via 100 Mb/s Ethernet
- Clock recovery with Si5344A chip

Hardware developments: C.J. Schmidt et al at GSI Det. Lab.,
M. Shitenkow at JINR
Firmware developments: Wojtek Zabolotny et al at Warsaw University of Technology (WUT)
Software developments: WUT and JINR

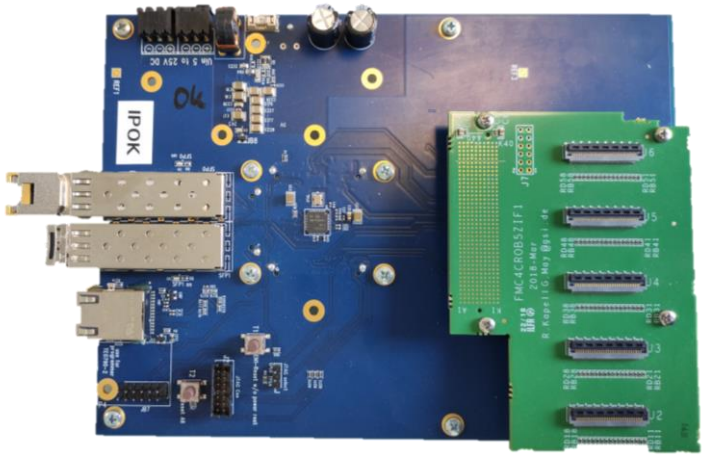
GBTxEMU H/W platform

Features:

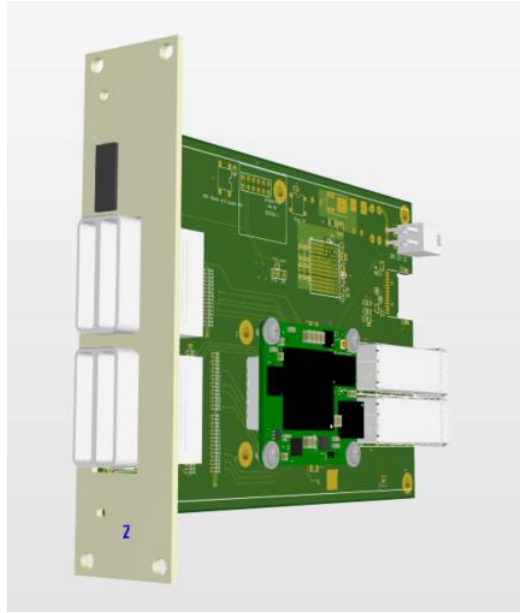
- 3U crate format;
- 12 layers PCB design;
- HDI6 connectors instead of mezzanine card;
- Minimal of s/w modifications are needed according to the prev. h/w platform
- The platform has the ability to upgrade and increase the clock to 80 MHz

Status:

- PCB Design is ready;
- All components are available;
- First operational boards on the table – Dec 2020.



Prototype of the GBTxEMU board



A new GBTxEMU board

New H/w design: JINR

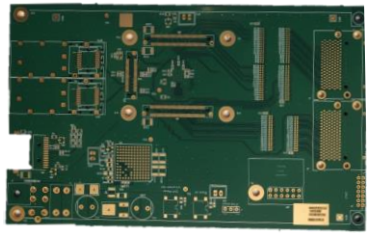
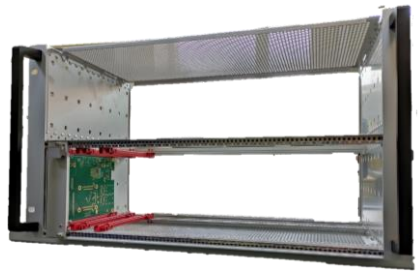
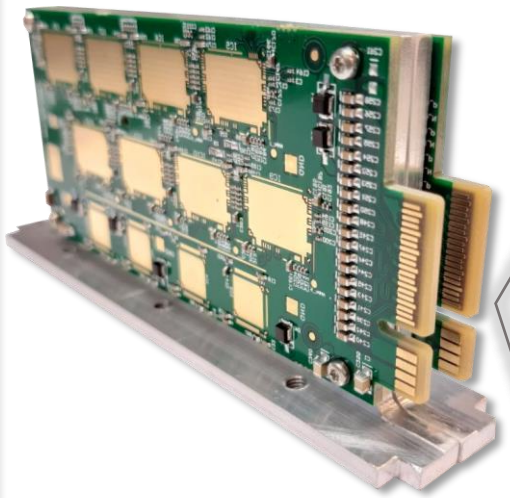


Photo of the PCB



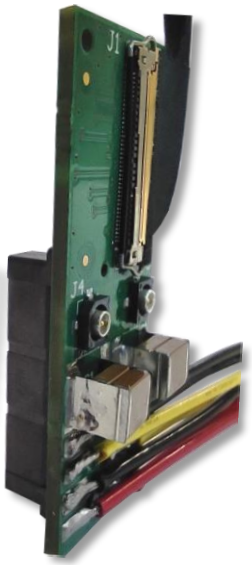
GBTxEMU crate

Connectivity between FEBs and GBTxEMU



Front-end boards

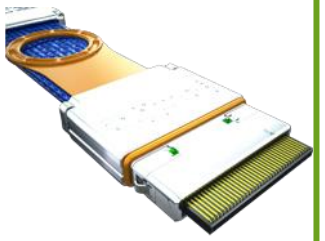
STS-box



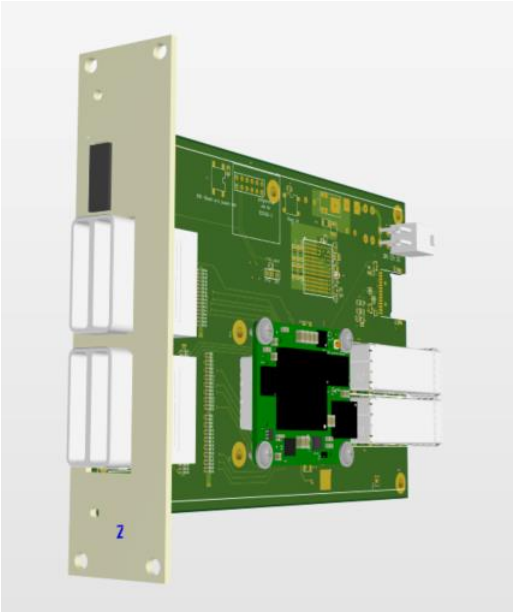
FEB-panel

Microcoax. cable
~0.7 m long

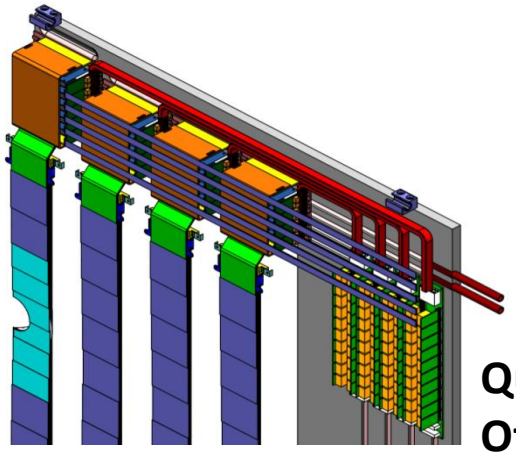
Cross-Pannel



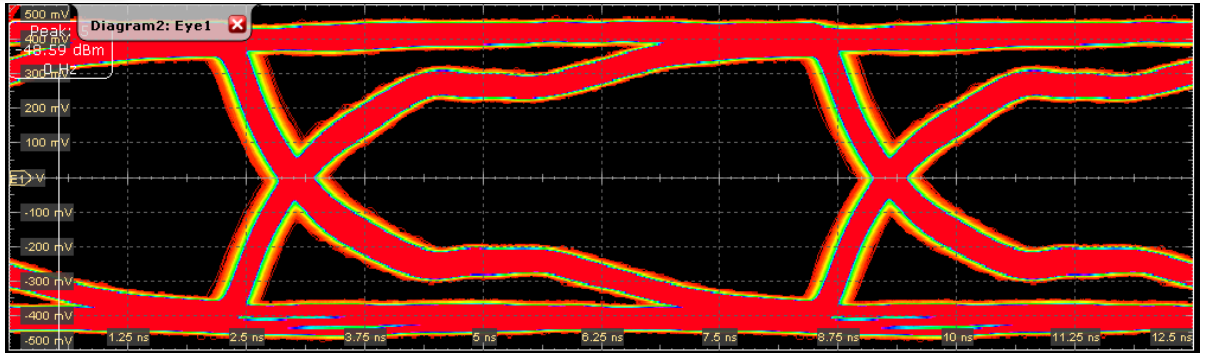
Twinax cable
~10 m long



GBTxEMU



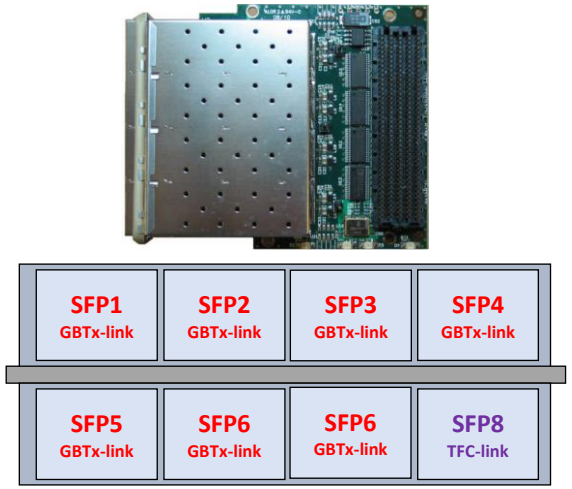
Quarter-station Of BM@N STS



Eye diagram of the Down link signal at 160 MHz Clck

GERI

TRENZ TEC0330-4 PCIe Gen2 Interface Board



FMC board with 8x SFP cages

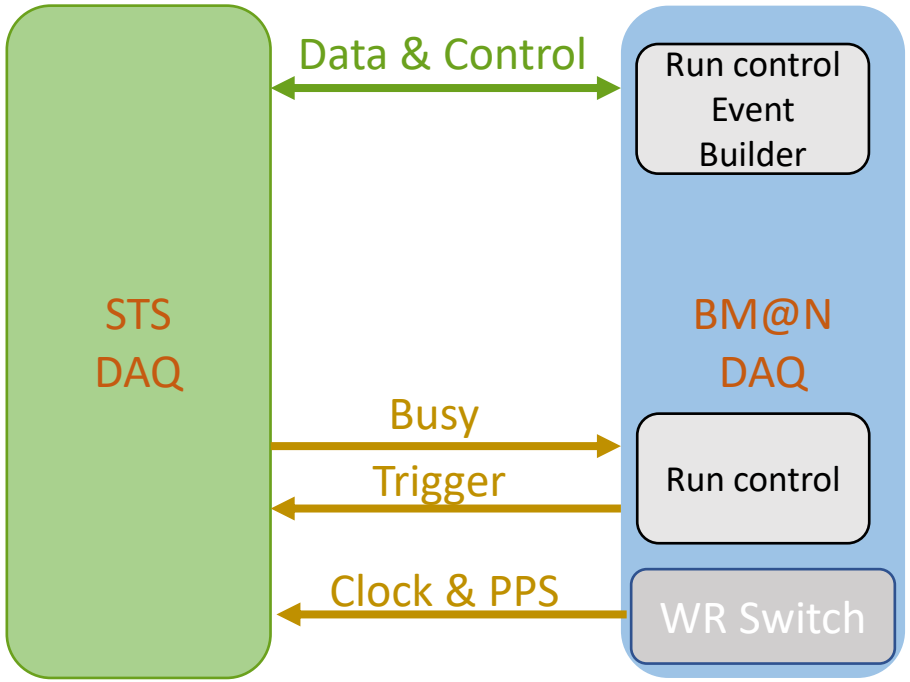
Compute node with data processing boards

GBTxEMU Readout Interface (GERI)

Is based on the commercial platform: TRENZ TEC0330-4

- Comprises Xilinx Virtex-7 FPGA
- 8 lane PCIe Gen2 interface
- Preprocessing of the data
- Timing and control interfaces
- Trigger interfaces
- Up to 7 GBTxEMU boards could be connected
- Refactoring of the DPB FW is ongoing

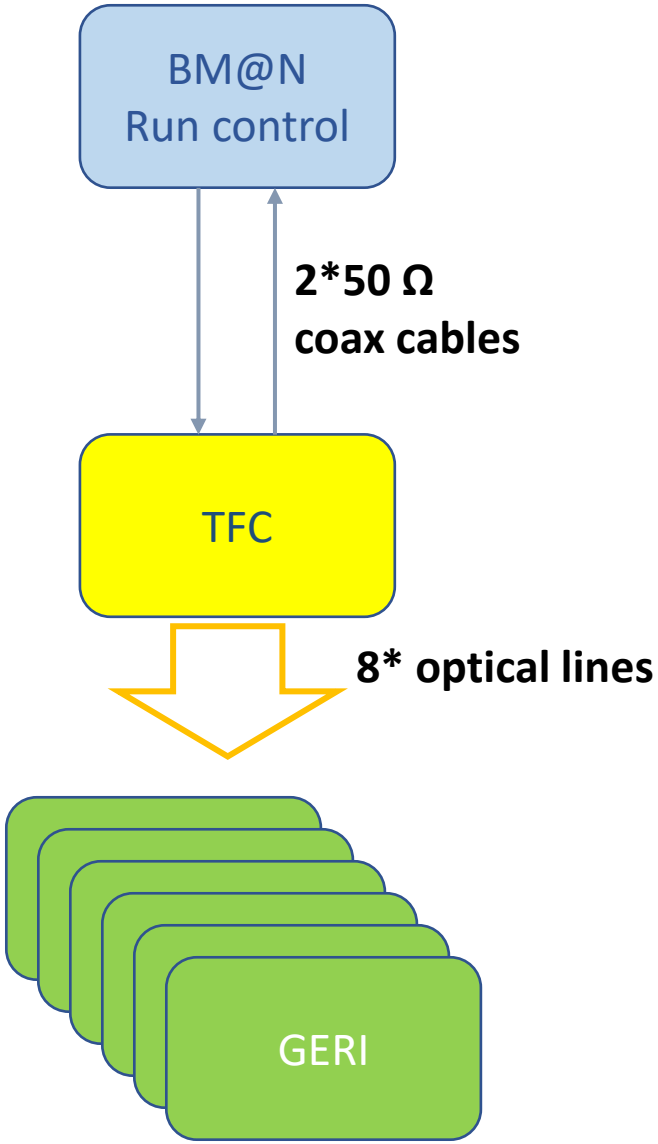
Integration into global BM@N DAQ



STS integration requirements:

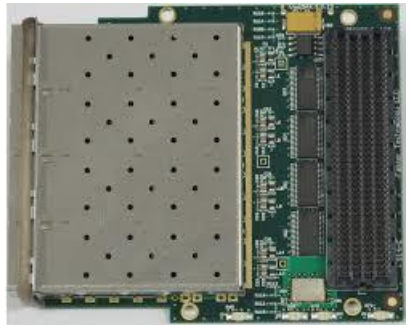
- Data & Control link from BM@N Run Control and Event Builder software
- Two 50 Ω coaxial connectors for trigger distribution and busy collection;
- Data packed in MPDRawData format
- Time synch between BM@N DAQ and STS DAQ within ~1 ns

Trigger distribution



- Trigger will be collected by the Timing and Fast Control (TFC) module
- Two SMA connectors for trigger and busy signals will be used
- Trigger signal will be distributed through the GERI boards via optical lines
- Expected trigger latency is ~5 μs

Timing mezzanine (COTS) – FM-S14

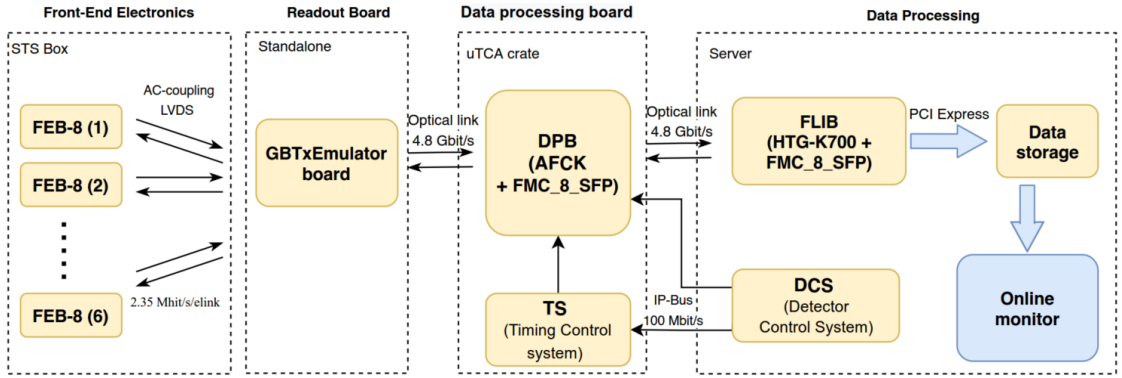


Timing and Fast Control (TFC) hardware

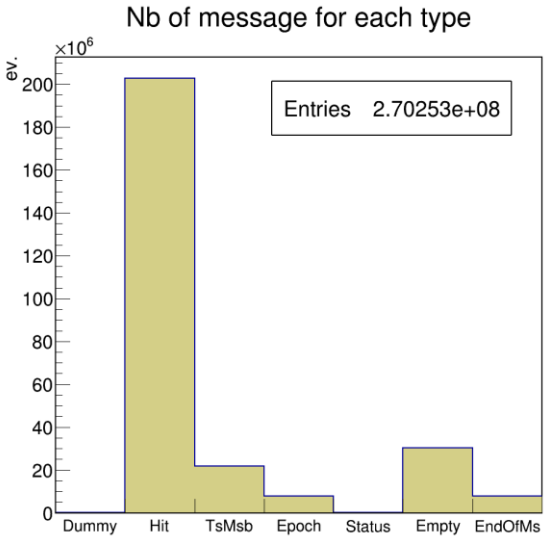
Processing of the trigger signals

- Data filtering according to the trigger decision will be performed at GERI
- A new F/W architecture proposed by the team from WUT uses the bin sorter (bucket sorter), where data are simply split into „bins” covering consecutive time periods
- The new readout architecture is currently tested in CBM
- The bin length is set to 3,2 µs and the number of bins is 16, that makes possible to implement the trigger with latency of 5µs

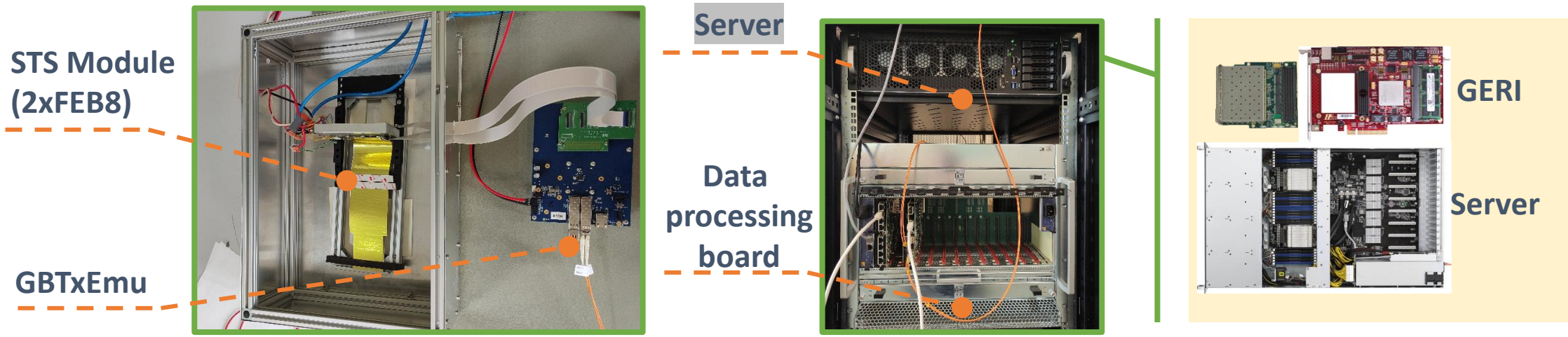
Prototype of the readout chain



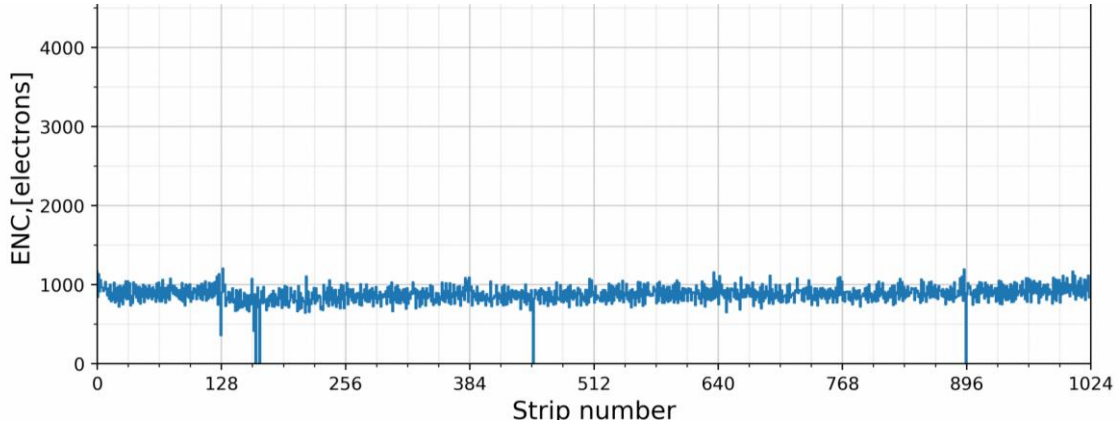
Prototype of the readout chain used for the certification of the modules



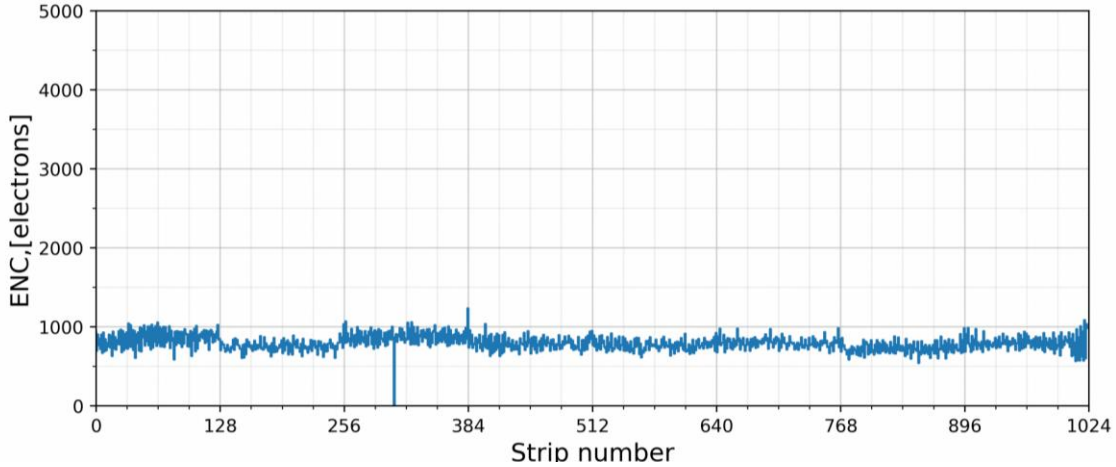
Types of messages per one connected FEB



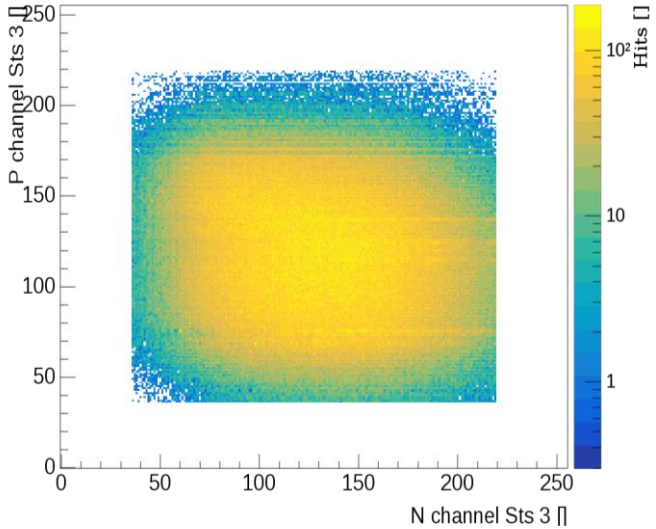
Prototype of the readout chain



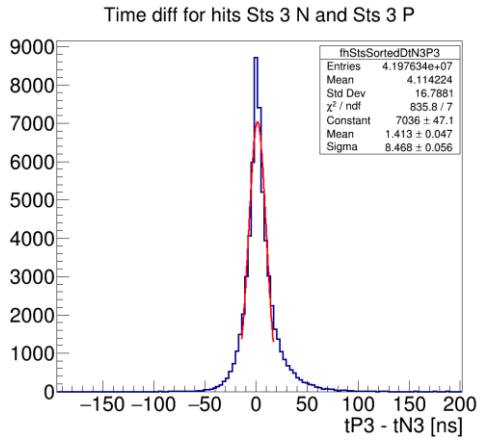
Noise/strip for the P-side of the module



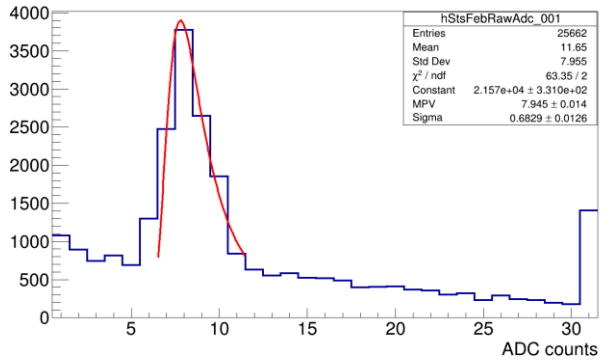
Noise/strip for the N-side of the module



Beam profile



Time synch



Energy distribution

Noise per strip measurements for the P- and N-sides of the sensor

Testing of the modules with electron beam at Linac-200

Summary

- STS readout system provides a completely free-streaming readout based on the concept of CBM DAQ
- GBTx functional is emulated with a help of FPGA
- Triggered mode of operation will be implemented on the level of GERI boards
- Prototypes of the H/W and F/W readout are already developed and are used in the test-benches
- Connectivity between the Front-end electronics and GBTxEMU interface was proposed

Thank you for your attention!