Development of data concentration method and its implementation in radiation-tolerant CMOS ASIC

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(headed by V. Samsonov)

Outline

- Motivation
- Expected applications (MPD TPC or/and BM@N STS)
- Common tasks and selected approbation
- ASIC designation & environment
- Design route
- Specifications
- Features & building blocks
- ASIC block diagram
- External interfaces
- Pinout & Bonding
- Further plans & conclusions

Motivation

- **General project** for MPD и BM&N
- The experimental set-ups contain up to 10**5 detector channels, ended by up to 10 bit ADCs and thus generate a large **amount of** digital **data**
- Needs to use a very limited number of **higher-speed** output **links** both for data transfer and control
- Necessity to process data on-detector in a non-friendly **radiation environment**
- Absence of COTs ready to use

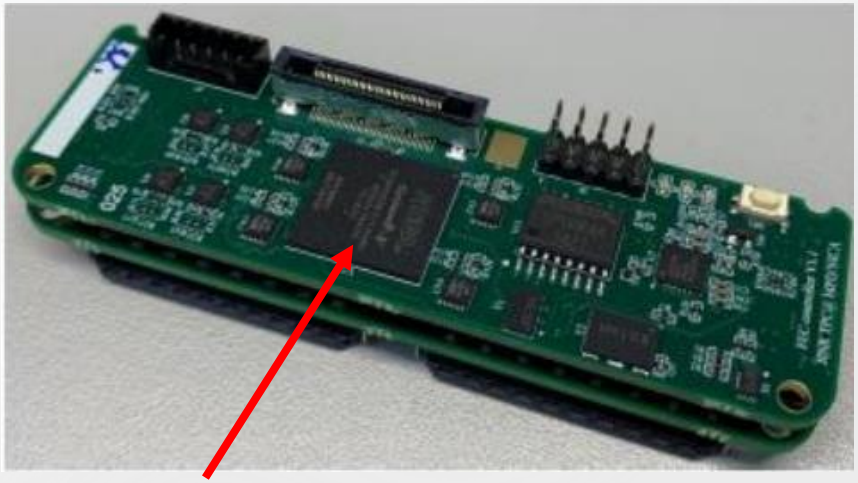
Common tasks

- High granularity and accuracy of the detecting equipment require a high integration, thus impose use of ASIC technology
- Development of a method for processing a large amount of data, generated at multichannel (up to 10**5 chs) detector FEE, ended by high-speed (10-20 Mbit/s) high-resolution (up to 10 bit) ADCs
- Data, coming from the FEE, should proceed through a synchronized deserialization, sequencing, noise-free and fault-free encoding, output serialization and then be transmitted via high-speed interface links at a gigabit rates
- Approbation method of data concentration based on own ASICs since no available COTs
- Development of approaches to be used to provide radiation tolerance of the designed ASICs

Approbation

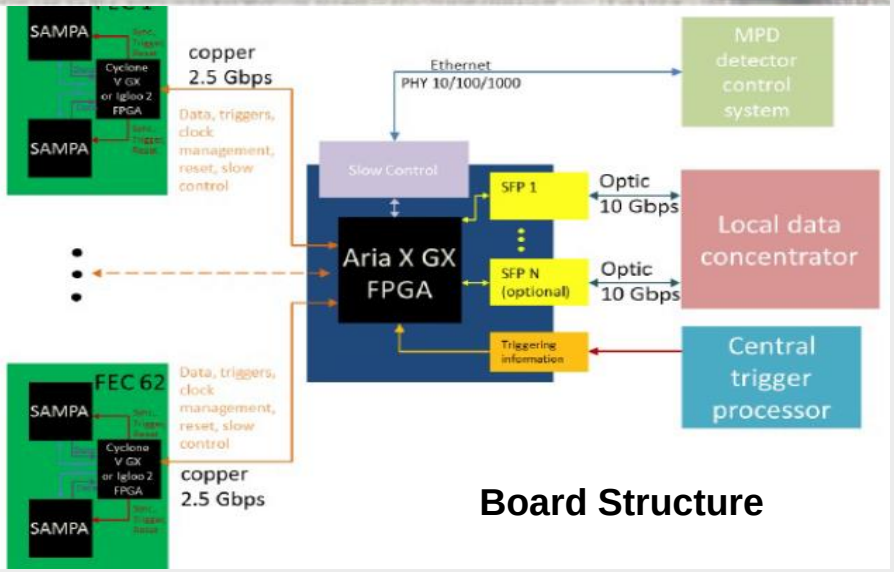
(replacement of non rad-hard FPGA in MPD TPC FEE cards)

SAMPA FEC Top view (service)



Non-radiation tolerant FPGA

SAMPA FEC Bottom view (ROC)



Board Structure

S.Movchan et al. MPD/NICA TPC status, INSTR-2020, Novosibirsk, Russia, Feb 24-28 2020

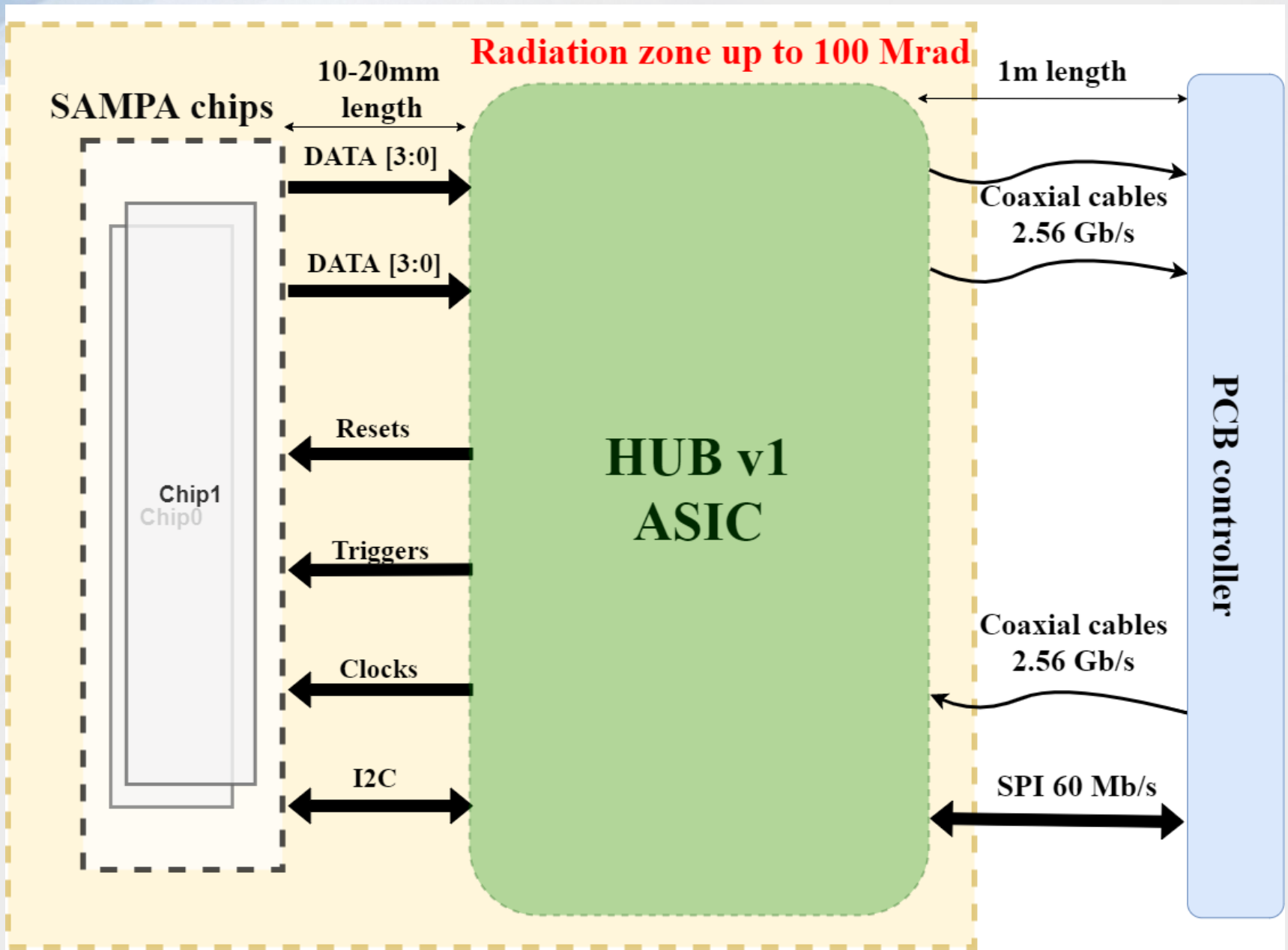
ASIC designation

- HUB v1 is a radiation tolerant prototype ASIC that can be used to implement multi purpose high speed bidirectional links for MPD TPC FEE .
- ASIC supports two 1m 2.56 Gb/s links in the direction from detectors to the counting room (Uplink) and one 1m 2.56 Gb/s link in the direction from counting room to the detectors (Downlink).

Interfaces:

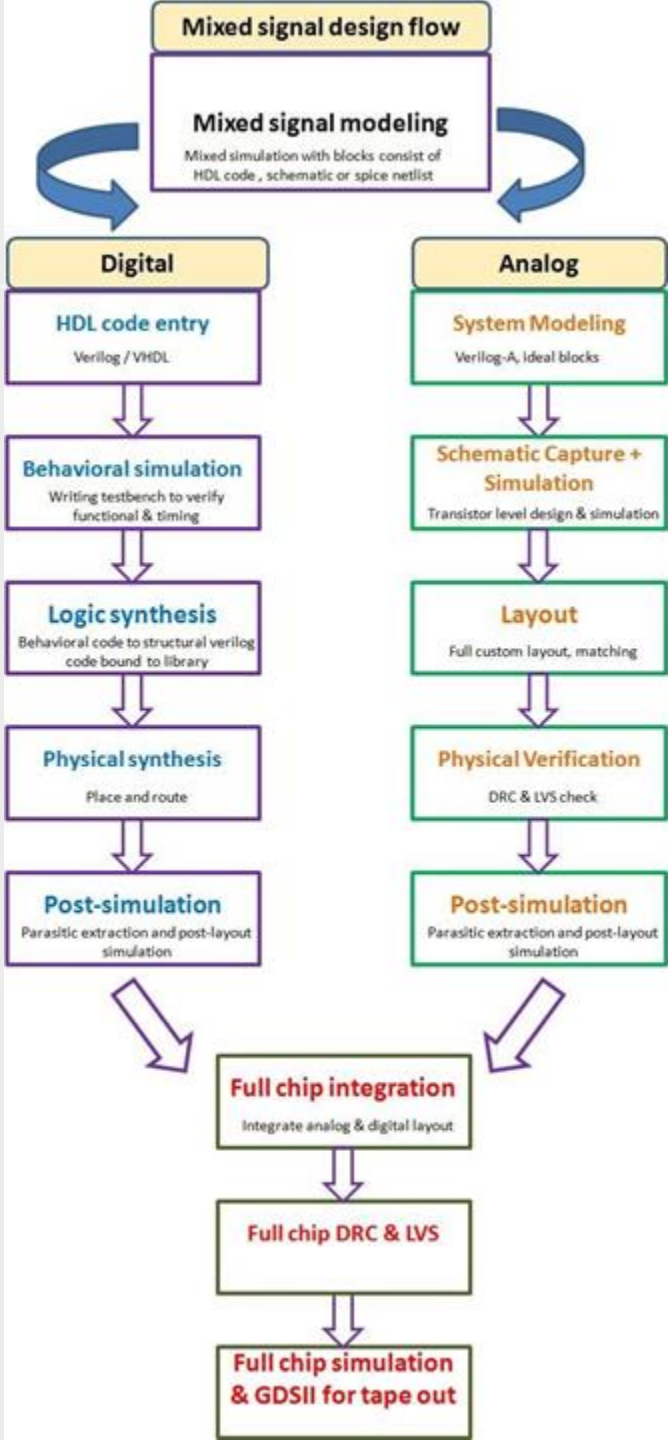
- 2x4 ports SAMPA data
- 2x ports SAMPA Reset
- 2x3 ports SAMPA Trigger
- 2x3 ports SAMPA Clock
- 2x CML Tx
- CML Rx
- SPI (slow control)
- I2C

Environment



Standard mixed-mode design route

- Cadence CAD tools for start-to-finish design flow
- Top-to-bottom design
- TSMC DKs for the 65 nm process
- Powerful computer servers + client workstations
- Digital on top and mostly digital flow

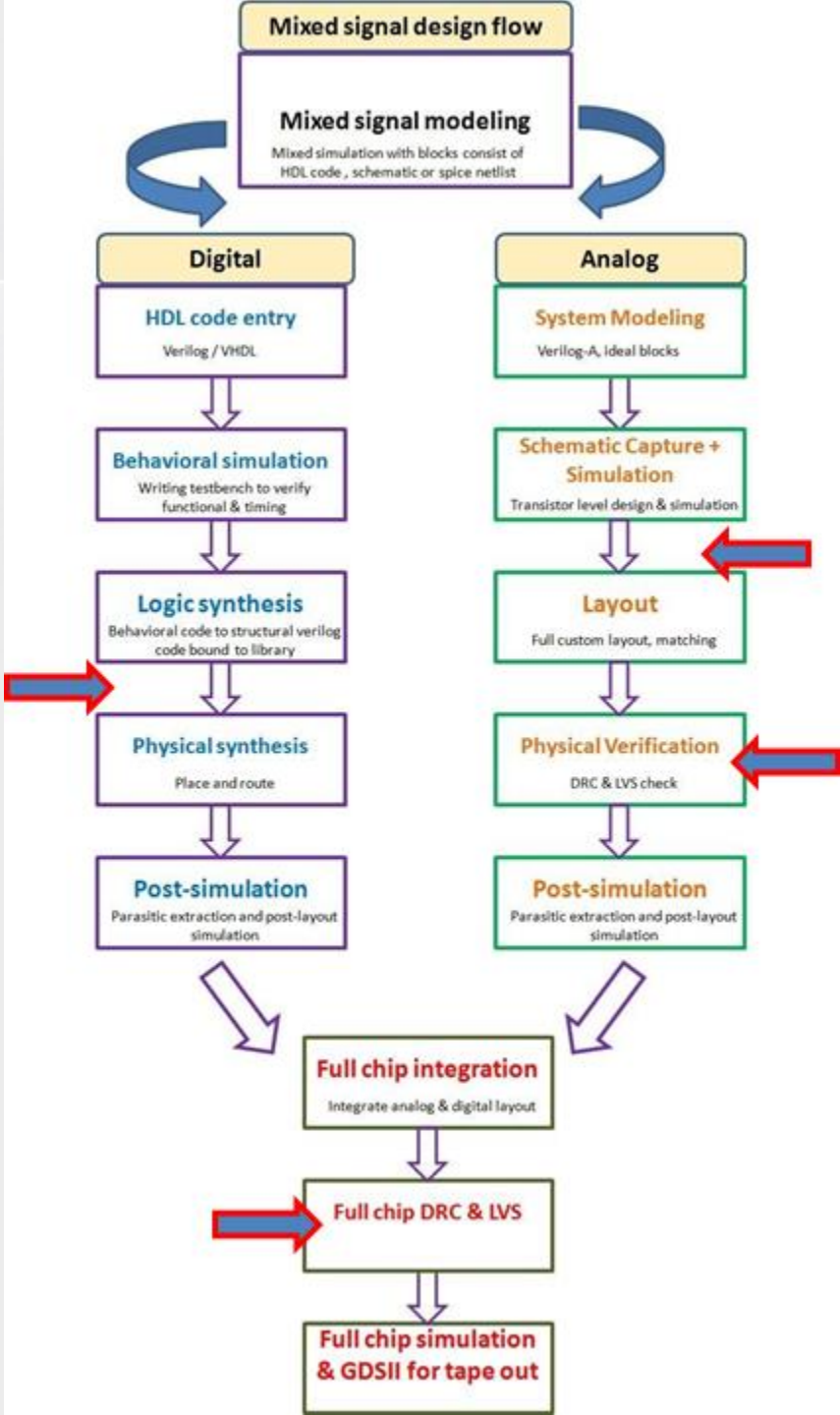


Radiation tolerance aspects in design

Legend 

- Digital part uses: 12T standard cell library of TSMC 65 nm process and triplication logic
- Analog part uses different known tips and tricks to provide radiation hardness by:
  - process
  - design
  - schematics implementation

(see proc. paper for details)



Specifications (1)

Specifications	Value
Technology node	65 nm
I/O voltage	2,5 V
CORE voltage	1,2 V
Temperature	0 - 85 ºC
Power consumption	< 1 W
Radiation tolerance	< 100 Mrad
Serial interface with SAMPA	
Number of input channels	8 channel (16 pins)
Maximum input frequency	320 MHz
Physical level	SLVS

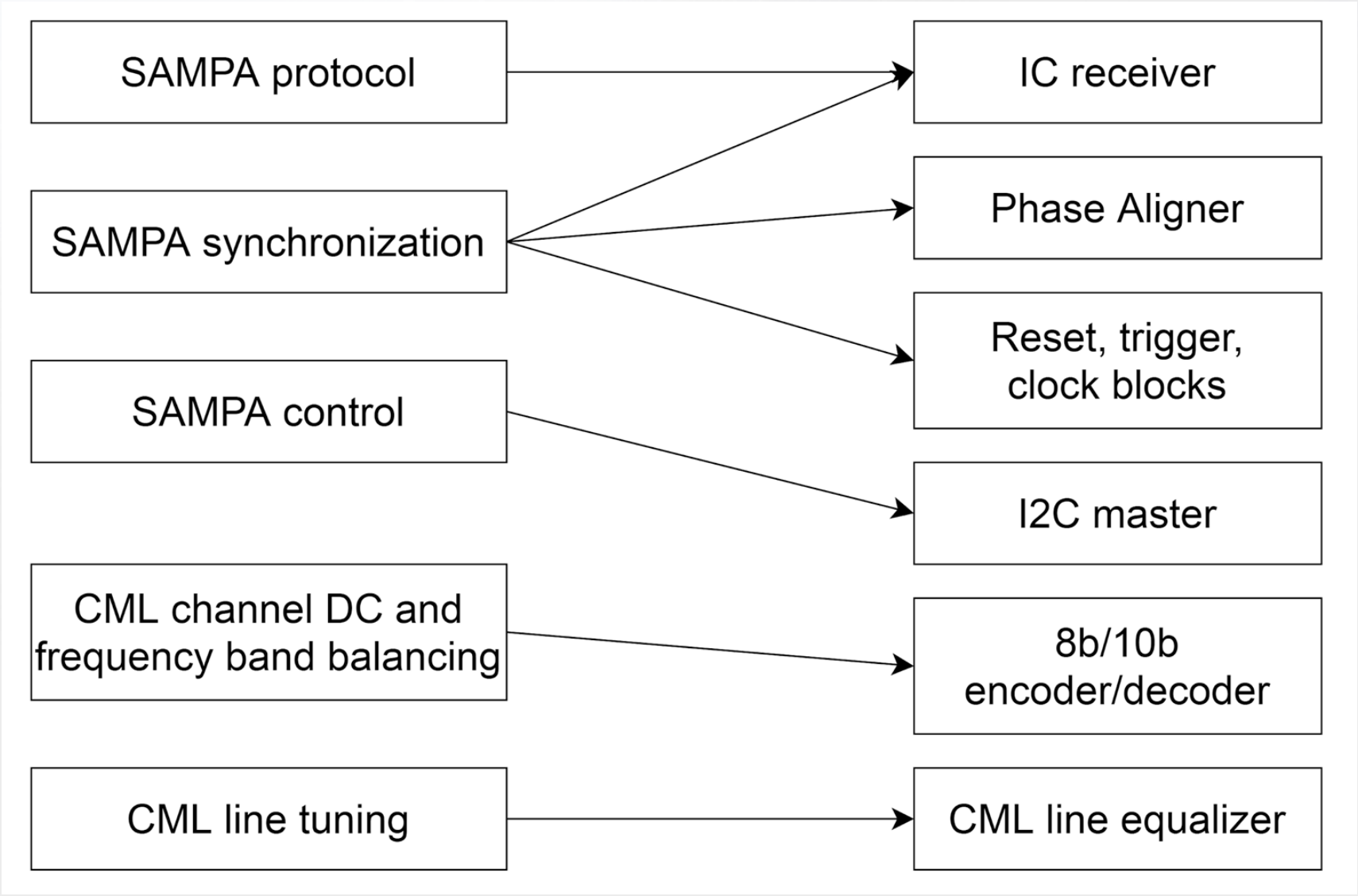
Specifications (2)

High speed Interface to counting room		
Number of channels	Input	1
	Outputs	2
Frequency	2.56 GHz	
Physical level	CML	
Transmission distance	< 1 meter	
I2C Interface		
Operating mode	10 bit addressing	
Frequency	100 kHz - 5 MHz	
Physical level	LVCMOS 1.2 V	
Synchronization Interface		
Number of channels	6 channel	
Frequencies	20/40/80/160/320 MHz	
Physical level	SLVS	

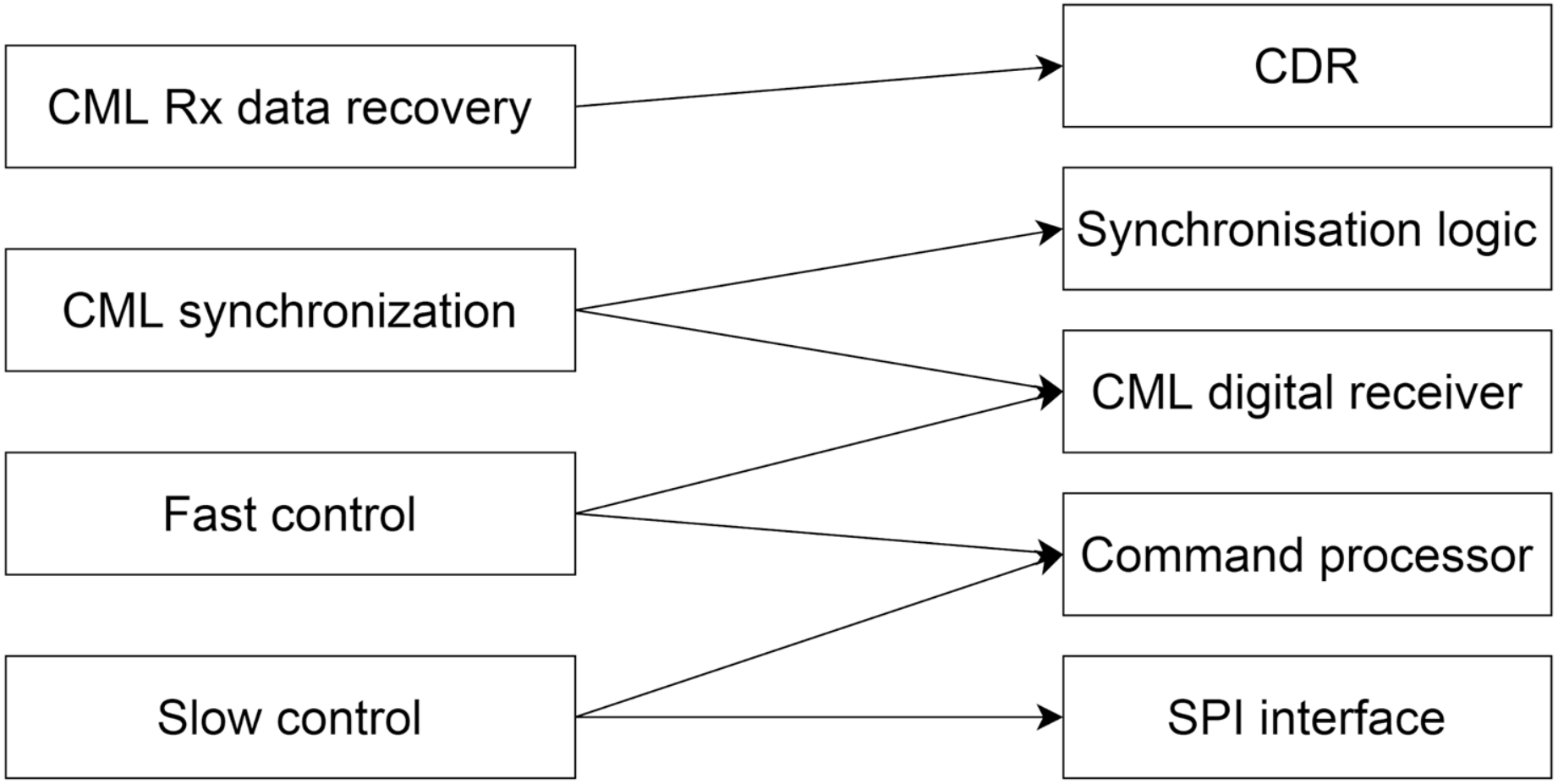
Specifications (3)

Output trigger links	
Number of links	6
Physical level	SLVS
Output reset links	
Number of links	2
Physical level	SLVS
Hardware address	
Number of links	4
Physical level	LVCMOS 1.2 V
External LDO control	
Number of links	2
Physical level	LVCMOS 1.2 V

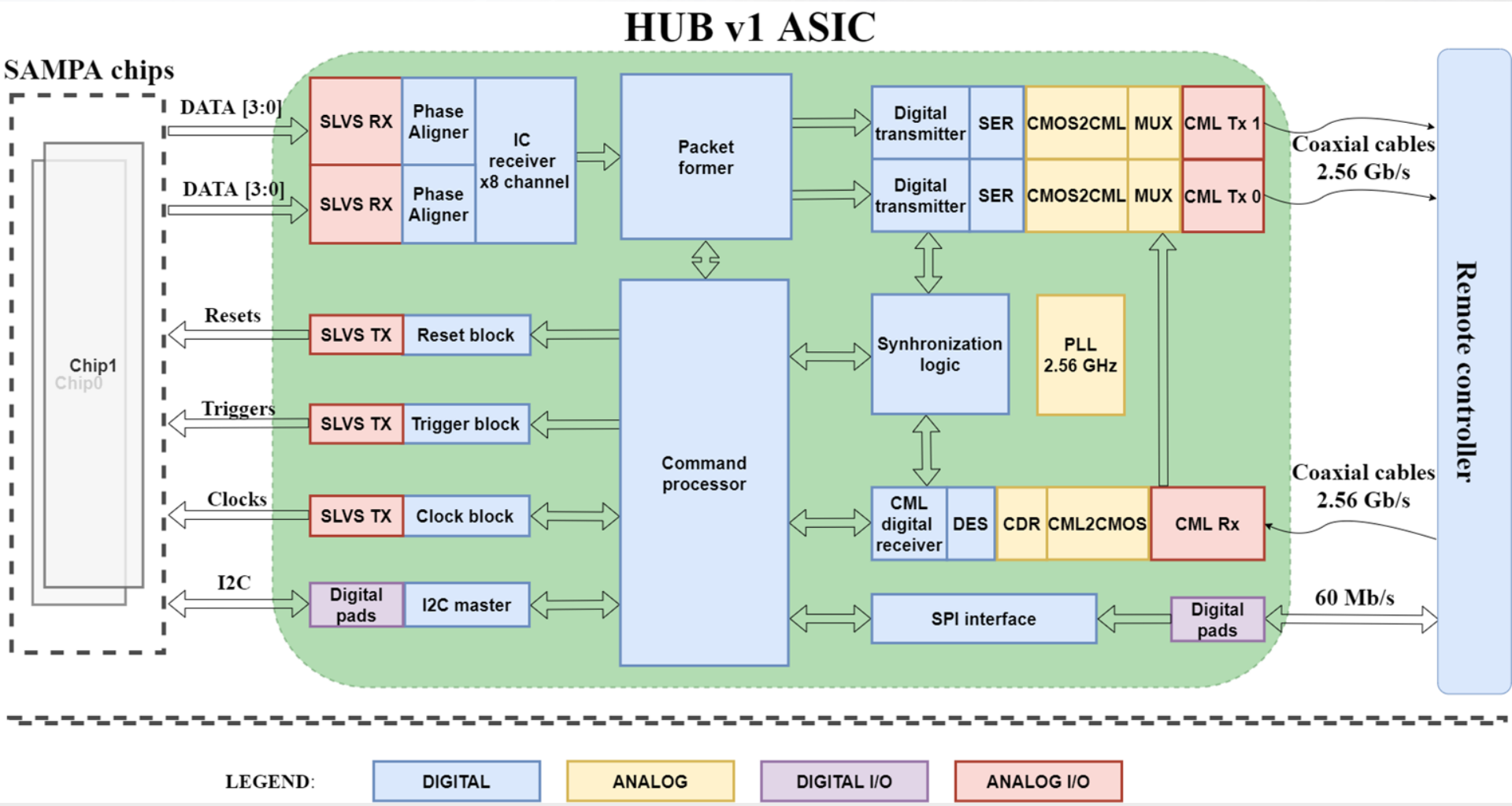
Features & blocks



Features & blocks (2)



Prototype ASIC block diagram

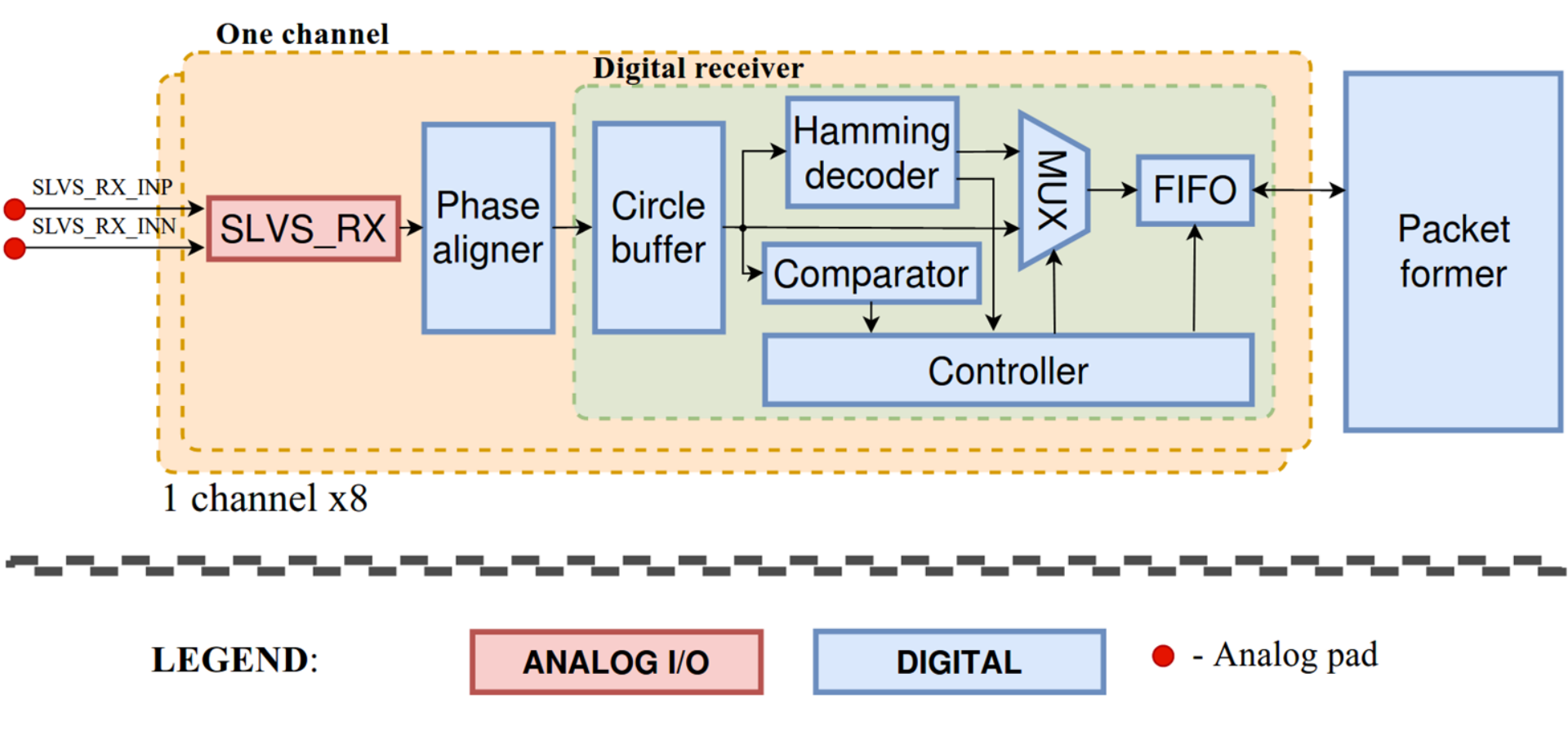


Mixed-mode (mostly digital (~70%)) design

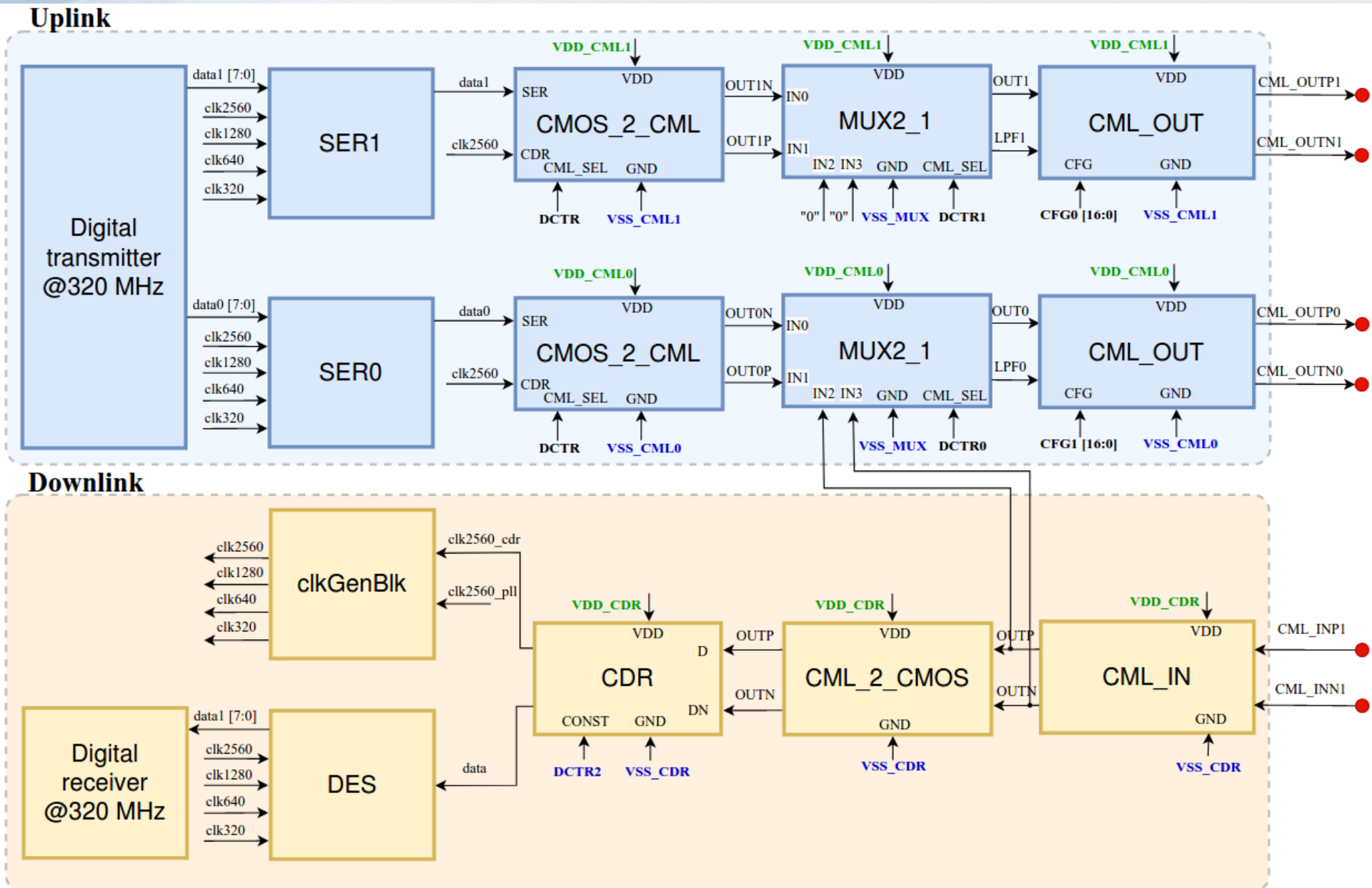
Building blocks

Analog blocks	***Digital blocks***	
SLVS Rx	IC receiver channel	I2C master
SLVS Tx	Phase Aligner	DES
CML_RX	Packet former	Reset
CML_TX	Digital Transmitter	Trigger
PLL	SER	Clock
CDR	Synhronization Logic	
POR	SPI Interface	
CMOS2CML	Command processor	

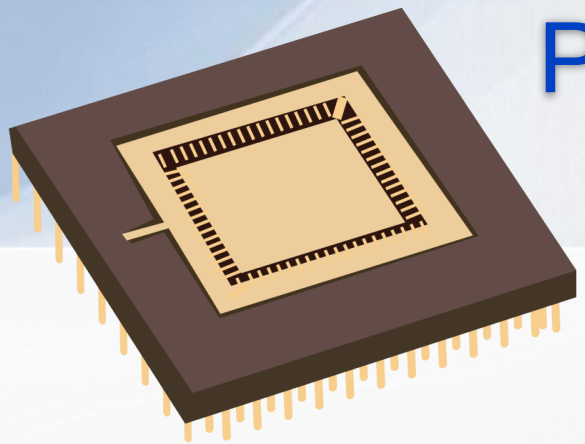
Getting data from SAMPA



High speed interface to counting room



Process & Pinout & Bonding



CPGA 120

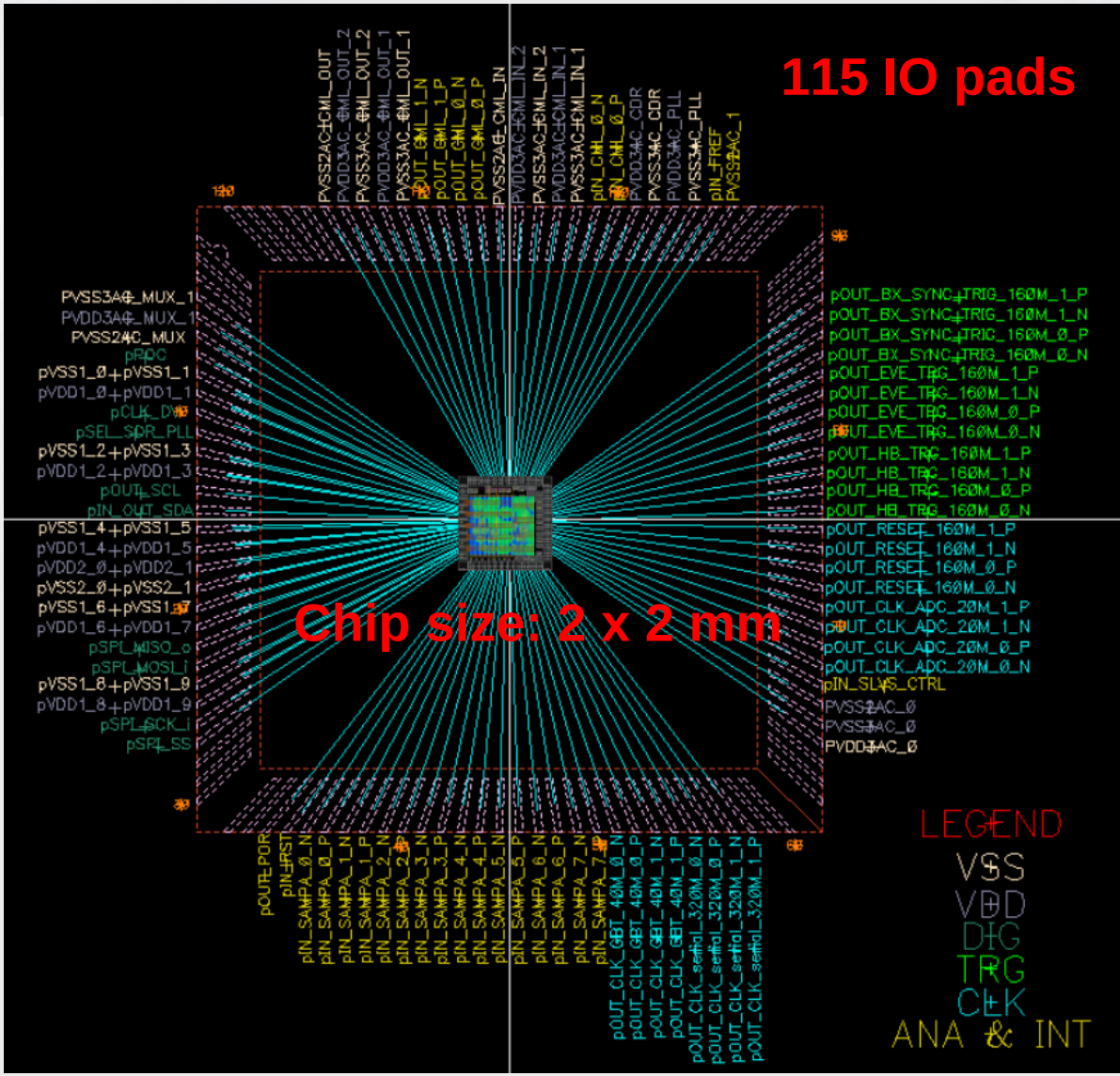
TSMC 65nm CMOS

Mixed-Signal/RF, Low Power

Core : 1.2 V, IO : 2.5 V

Metal scheme:

1P9M_6X1Z1U



a well radiation qualified commercial process

Nearest plans

EUROPRACTICE ASIC SERVICE

TSMC

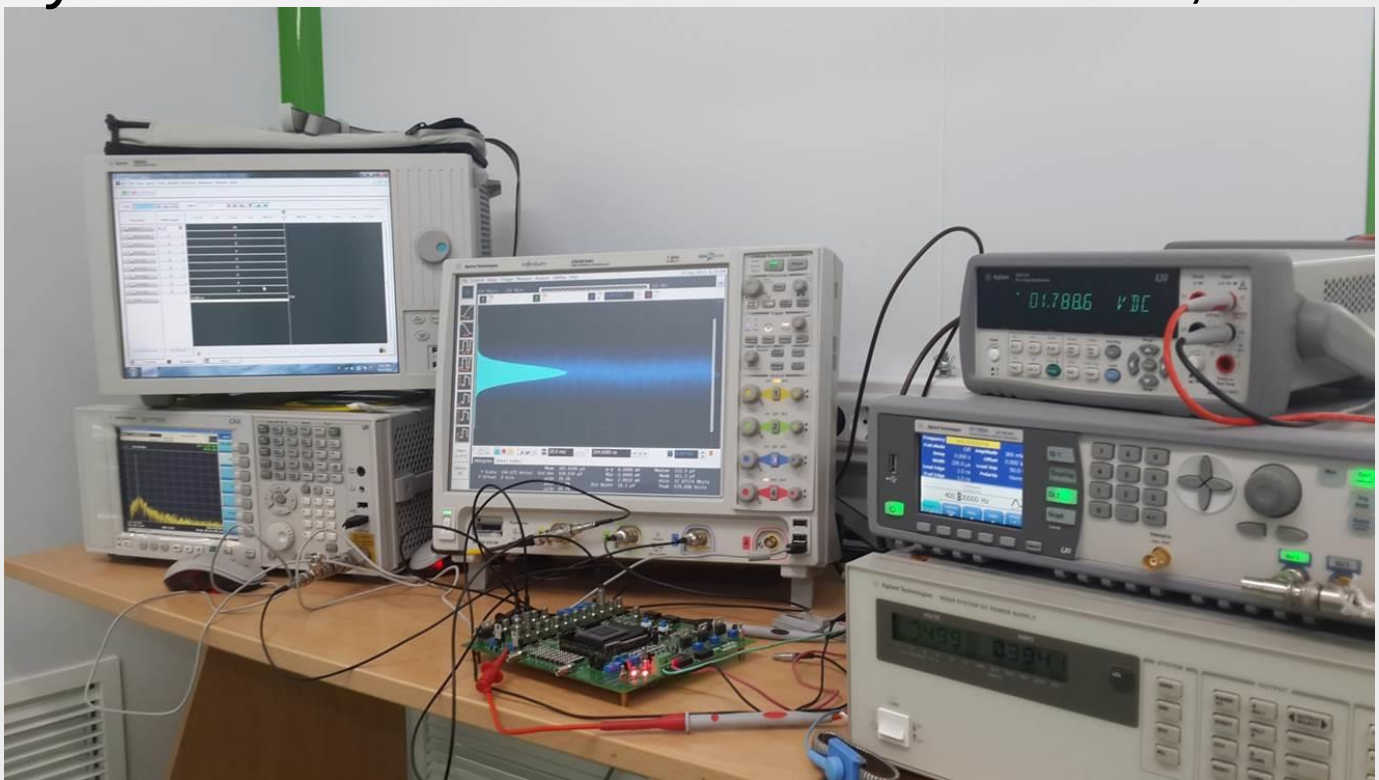
Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
TSMC 65nm CMOS Logic or Mixed-Signal/RF, Low Power*		19			13			19			18	

Nov. 18, 2020 -- deadline for ASIC GDSII submission for prototyping via Europractice miniasic program

Sponsorship for fabrication is a responsibility of MPD team from JINR

Further plans (2021)

- Design of breadboard (PCB) & measurement technique
- Lab functional tests of prototyped ASICs
- Study of ASIC radiation tolerance at PNPI, Gatchina



Conclusions

- Method for front-end (on-detector) data concentration has been developed
- Its implementation in radiation-tolerant CMOS ASIC, intended for the FEE cards of MPD TPC, is foreseen
- Prototype ASIC will be submitted for fabrication via Europractice soon (on Nov. 18)
- Lab functional tests of ASICs as well as their radiation tolerance tests are expected as next steps in 2021

Thank you
for attention

The presented results have become possible due to RFBR support under Grant 18-02-40093

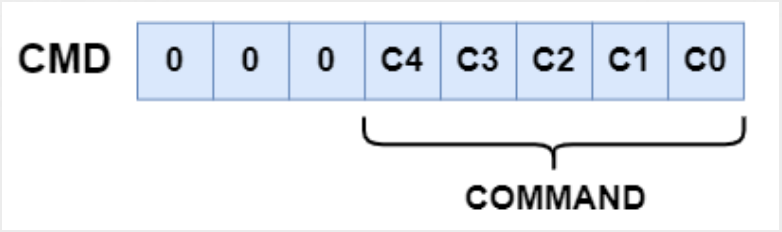
Back up slides

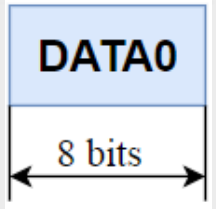
Format of commands for remote controller

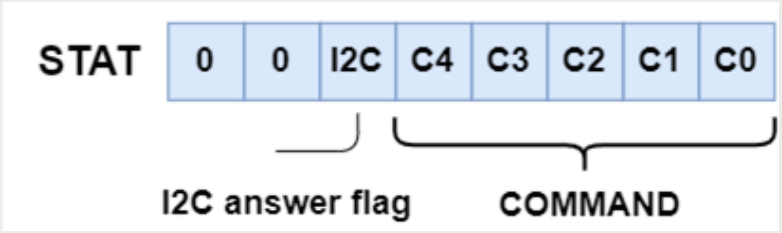
Request	CMD	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
Answer	STAT	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Commands:

- Config load
- Config read
- Soft Reset
- Trigger out
- SAMPA reset
- I2C read
- I2C write





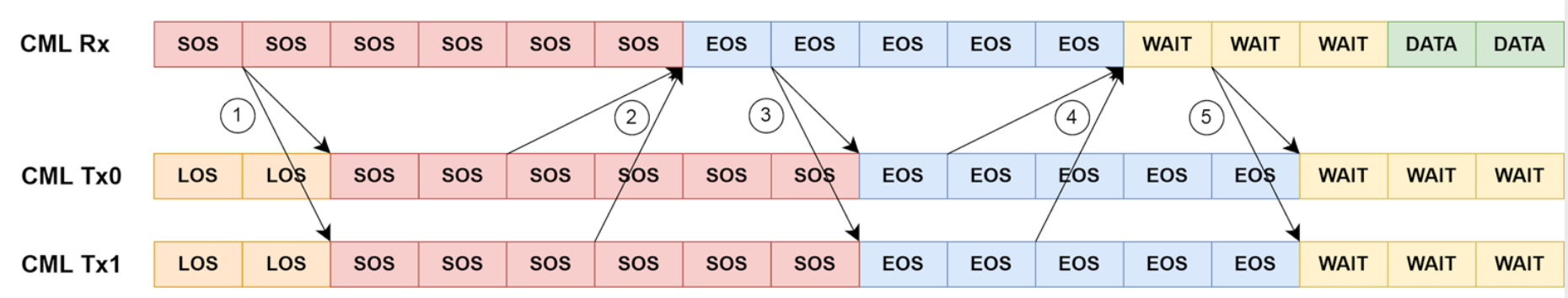


CML protocol (1)

Main CML interface features:

- CML Rx receives command request
- CML Tx 0 translates command response and SAMPA data (if CML Tx 0 is free)
- CML Tx 1 translates SAMPA data if CML Tx 0 is busy
- CML data are encoded by 8b/10b

CML protocol (2)
Synchronization procedure



CML modes:

- LOS (lost of sunc) - K28.4
- SOS (start of sync) - K28.1
- EOS (end of sync) - K28.3
- WAIT - K28.5
- Data packet
- Cmd packet

Steps:

1) ASIC starts of synchronization
2) Controller synchronize both channels
3) ASIC sends EOS
4) Controller finalize synchronization
5) ASIC finalize synchronization