## **Readout electronics for TPC detector in the MPD/NICA project**

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## Outline

- Multi-Purpose Detector of NICA project
- TPC design overview and main parameters
- Requirements for the data readout system, design concept and status
- PASA + ALTRO chipset design
- SAMPA design
- Conclusion

## General view of the TPC in the MultiPurpose Detector (MPD) of NICA project



# MPD tasks for TPC

The scientific program of the MPD includes the following topics:

- > Particle yields and spectra (  $\pi$ ,
- K, p, clusters,  $\Lambda$ ,  $\Omega$ )
- > Event-by event fluctuation
- > Femtoscopy with  $\pi$ , K, p,  $\Lambda$
- > Collective flow of identified hadron species
- > In-medium modification of vector mesons



Observables	Detectors in use
Yields & spectra	TPC, ZDC, barrel TOF & ECAL
	end-cap tracker + end-cap TOF & ECAL
Di-leptons	TPC, barrel TOF & ECAL
	end-cap tracker + end-cap TOF & ECAL
Event-by-event fluctuations	ZDC, barrel TOF & ECAL
	end-cap tracker + end-cap TOF & ECAL
Flow	TPC,TOF, event plane detector (extended ZDC)
	end-cap tracker + end-cap TOF & ECAL
Hyperons, hyper-nuclei, charm	TPC, IT

## TPC parameters



Item	Dimension
Length of the TPC	340cm
Outer radius of vessel	140cm
Inner radius of vessel	27 cm
Outer radius of the drift	133cm
volume	
Inner radius of the drift	34cm
volume	
Length of the drift	170cm (of each half)
volume	
HV electrode	Membrane at the center of the TPC
Electric field strength	~140V/cm;
Magnetic field strength	0.5 Tesla
Drift gas	90% Ar+10% Methane, Atmospheric pres.
	+ 2 mbar
Gas amplification factor	$\sim 10^4$
Drift velocity	5.45 cm/µs;
Drift time	< 30µs;
Temperature stability	< 0.5°C
Number of readout	24 (12 per each end-plate)
chambers	
Segmentation in $\phi$	30°
Pad size	5x12mm <sup>2</sup> and 5x18mm <sup>2</sup>
Number of pads	95232
Pad raw numbers	53
Pad numbers after zero	<10%
suppression	
Maximal event rate	< 7 kHz ( Lum. 10 <sup>27</sup> )
Electronics shaping time	~180 ns (FWHM)
Signal-to-noise ratio	30:1
Signal dynamical range	10 bits
Sampling rate	10 MHz
Sampling depth	310 time buckets

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## TPC design



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Requirements for the data readout system

- Total number of channels is: 95 232
- Trigger rate 7 kHz, max tracks per event 1000
- Mean data stream with zero suppression 7 GB/s
- Mean data stream without zero suppression 23 GB/s
- Requirement for TPC end-caps transparency (because of FEE is shading CPC Tracker, ECT, TOF)

# Read out electronics design status

- Main components of FEE FECs, RCUs and gigabit data links
- Design based on the ASICs (PASA +ALTRO or SAMPA) and FPGAs
- ALTRO+PASA option (FEC64S) design was completed
- Pilot system (512 ch) is under testing
- SAMPA option design is in progress
- Controller RCU design was completed
- Controller manufacture December 2017

## FEC-64S (top side) with cable



## FEC64S linearity



Top graph shows the difference between the measured value and the linear fit. The bottom graph demonstrates FEC response to the input signal

## Eight cards at the test setup



1) FECs array (512 ch. in total); 2) clocks and control signal distribution card; 3) RCU emulator

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## New ASIC for TPC electronics (SAMPA)

- New ASIC SAMPA [1,2] is under development. V2, V3 and V4 preproduction versions are exist.
- Few amount of pilot chips version V2 was tested and measurement results has showed us feasibility of design SAMPA-based FEC for the TPC MPD/NICA.
- Concept of usage SAMPA chip in the FEE was defined and design of the new FEC in progress.

[1] S.H.I. Barboza et al. SAMPA Chip: a New ASIC for the ALICE TPC and MCH Upgrades. // J. Instrum. 2016. V. 11. C02088.
[2] J. Adolfsson et al. SAMPA Chip: the New 32 Channels ASIC for the ALICE TPC and MCH Upgrades. // J. Instrum. 2017. V. 12. C04008.

# SAMPA testing in Dubna

### Using SAMPA test board in Dudna



Shielding box

### SAMPA test board

# FPGA development board

#### General view of test setup



#### **SAMPA chip parameters:**

- Cross-talks < 0.5%
- Noise ~ 500e<sup>-</sup>
- ADC ENOB = 9.2 bit
- e-links (350 MHz each)

## SAMPA block diagram



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## Main advantages of the SAMPA chip:

- SAMPA chip is more integrated then PASA and ALTRO chip set. Its square is only 225 mm<sup>2</sup> per 32 channels while squares of PASA and ALTRO are 484 mm<sup>2</sup> and 708 mm<sup>2</sup> respectively per 16 channels. Estimates show that the size of the FEC PCB can be reduced by a factor of 3.
- SAMPA chip can operating with multi-wire proportional chambers as well as with GEM chambers that is necessary for a future TPC upgrade.

## SAMPA-based FEC block diagram



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## Firmware operation monitoring

### Synchronization packets from 4 SAMPA links

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## SAMPA data monitoring in test setup

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## SAMPA-based pilot system status

- The same concept as for ALTRO pilot system was proposed
- Target 8 card system (512 ch.) for beam test (17/18 year).
- Firmware was developed and tested with SAMPA test board as model of FEC. Firmware works without any faults.
- FEC schematic was finished.
- PCB layout is in progress.

## Conclusion

## FEE TPC for MPD/NICA project is designing.

- FEC testing including analog and digital parts was performed. RCU firmware was developed and verified.
- ALTRO-based FEC design was completed and trial lot of FECs was fabricated.
- RCU prototype is under verification.
- Schematics and firmware for SAMPA based FEC was designed. PCB layout is in progress.
- Preparation of beam test in progress.

On behalf TPC/MPD electronics group allow me to express gratitude for the help to:

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# Thank you for your attention!