THE PHASE-II UPGRADE OF THE ATLAS CALORIMETER

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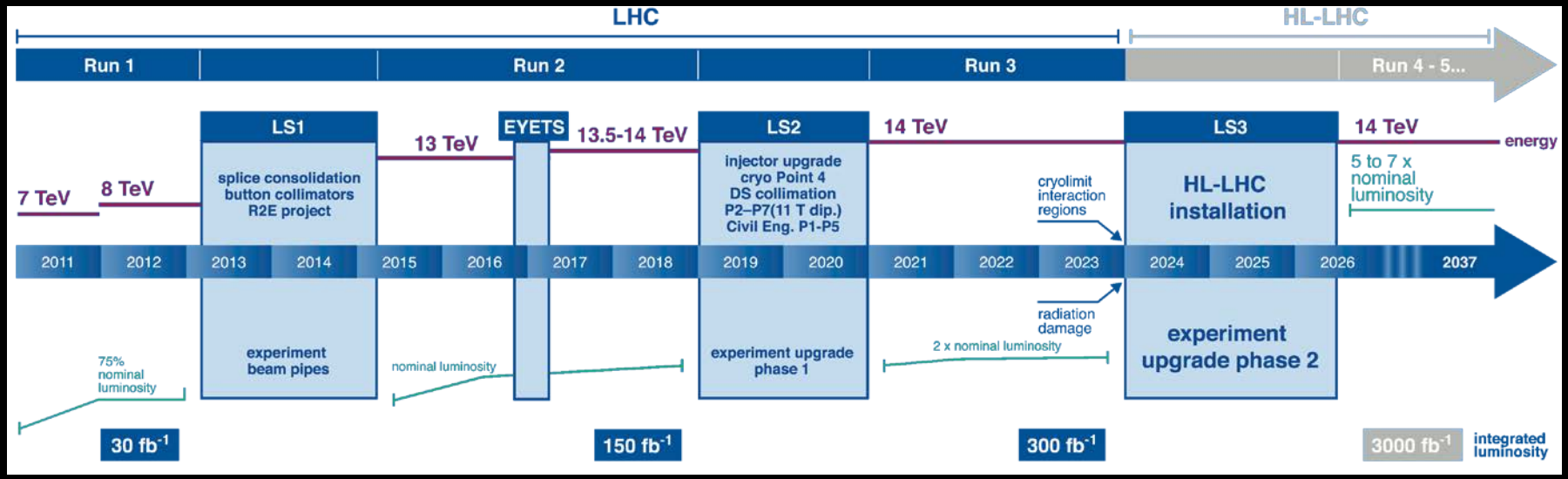
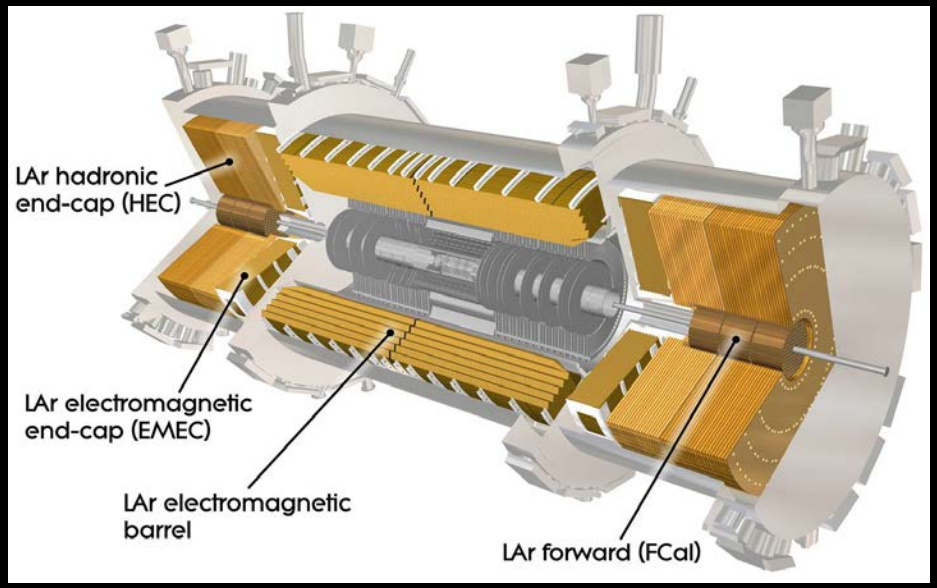
High Luminosity LHC

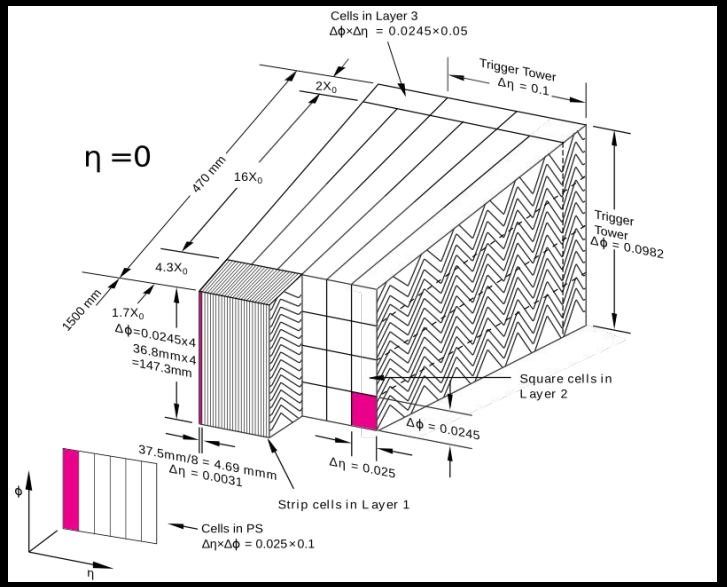


- Instantaneous luminosities up to 7.5×10^{34} cm^{-2} s^{-1}
- "Ultimate" integrated luminosity up to 4000 fb^{-1} after a period of about 12 years
- Up to $\langle\mu\rangle$ = 200 interactions per bunch crossing
- Challenging run conditions will require a substantial upgrade of the LHC detectors
- Two upgrades of the ATLAS detector discussed here:
  - Upgrade of Liquid Argon calorimeter front-end and back-end electronics
  - New detector: High Granularity Timing Detector (HGTD)

Upgrade of Liquid Argon calorimeter electronics

Liquid Argon calorimeter system





- EM barrel and end-cap:
  - accordion geometry lead/LAr sampling calorimeters
- Hadronic end-caps:
  - copper/LAr calorimeter
- Forward calorimeter:
  - Three cylindrical modules arranged sequentially
  - FCal1: uses copper as absorber
  - FCal2 and FCal3: uses tungsten
- Total of 182468 channels

Upgrade of LAr electronics

- The LAr calorimeters themselves are expected to operate reliably during the HL-LHC data-taking period
- But the current electronics is not compatible with operations at HL-LHC
  - Radiation resistance: replace components with versions more rad-tol
  - Ageing: some components would have ~20 yrs operation. Difficult to maintain and repair
  - Trigger: the ATLAS trigger system will be upgraded to cope with the expected pile-up, making the present LAr readout electronics incompatible.

$\Rightarrow$ All front-end and back-end electronics will be replaced

Requirements

- Trigger and DAQ upgrade
  - Baseline: one hardware trigger with 1 MHz Level-0 accept rate and 10 μs buffering interval
  - Evolution: two hardware trigger levels operating at 2-4 MHz Level-0 accept rate (10 μs buffering) and 0.6-0.8 MHz Level-1 accept rate (35 μs buffering)
- Radiation tolerance

	TID [kGy]		NIEL [n_{eq}/cm^2]		SEE [h/cm^2]	
ASIC	1.24	(2.25)	3.4×10^{13}	(2)	4.6×10^{12}	(2)
COTS (multiple lots)	16.5	(30)	13.6×10^{13}	(8)	1.8×10^{13}	(8)
COTS (single-lot)	4.1	(7.5)	3.4×10^{13}	(2)	4.6×10^{12}	(2)
LVPS (barrel and endcap)	3.0	(30)	3.4×10^{13}	(8)	4.3×10^{12}	(8)
HEC LVPS	0.02	(2.25)	6.0×10^{11}	(2)	1.2×10^{11}	(2)

- Dynamic range
  - large dynamic range needed: eg in the barrel from about 35 MeV (muon MIP deposit in one “strip”cell) to about 3 TeV (from searches of high mass resonances)

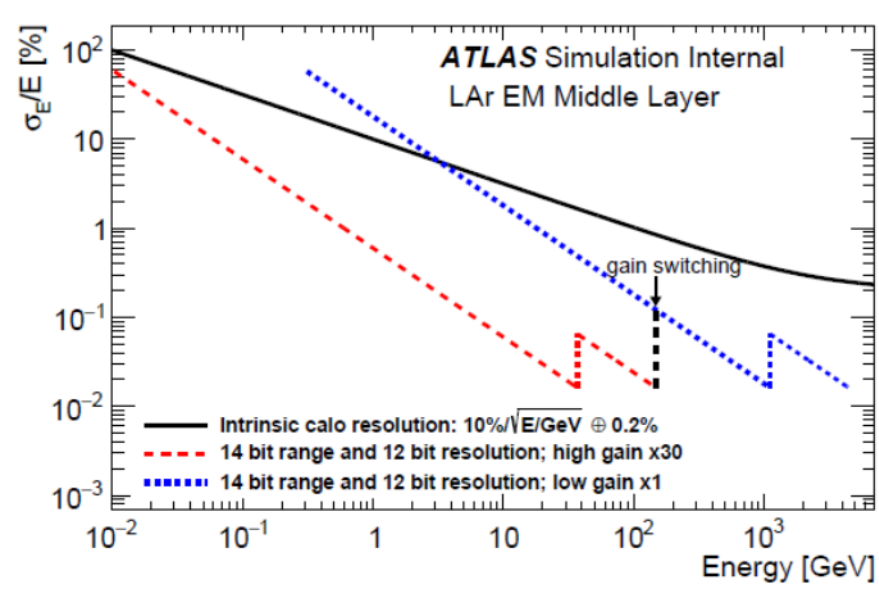
Requirements

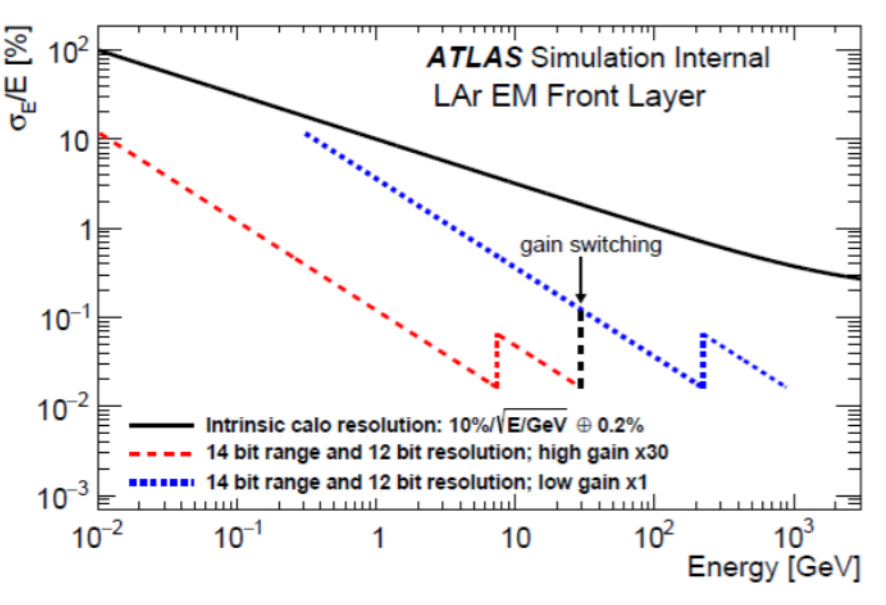
- Linearity
  - Energy scale set using Z or J/ψ. Need linearity at ‰ level up to ~10% (300 GeV) of the dynamic range; somewhat looser (few percents) at higher energies
- Noise
  - sum of electronic and pile-up noise: dominated by pile-up noise at high energies; can be reduced with optimal filtering techniques
  - however, especially for calibration, aim to keep electronic noise lower than MIP signal (order of 50 MeV in the “middle” cells) before filtering
- Shaping
  - today: bipolar CR-$(RC)^2$ shaping of analog LAr triangular signal with peaking time of 13 ns
  - plan to do something as today or similar (CR-$(RC)^3$ also under study) with programmable peaking time

Requirements

- Digitization
  - full dynamic range of the preamp to be digitized typically 16 bits
  - Baseline is to develop a 14-bit, rad-hard, ADC
  - two-gain system where each ADC digitizes only part of the range and both outputs are sent to the back-end electronics
- The quantization noise must be lower than the electronics noise (typically around half a LSB)
- At the lowest energy at which the low gain is used (gain-switching energy), the quantization noise must be lower than the intrinsic LAr resolution (typically $10\%/\sqrt{(E/GeV)} + 0.2\%$ in the EM calorimeters, in order not to degrade the total resolution by more than 5%.
- requirement from physics: arrange gain switching so that most photons from H->$\gamma\gamma$ have their cells in high gain, as for Z decays that are used to set the energy scale

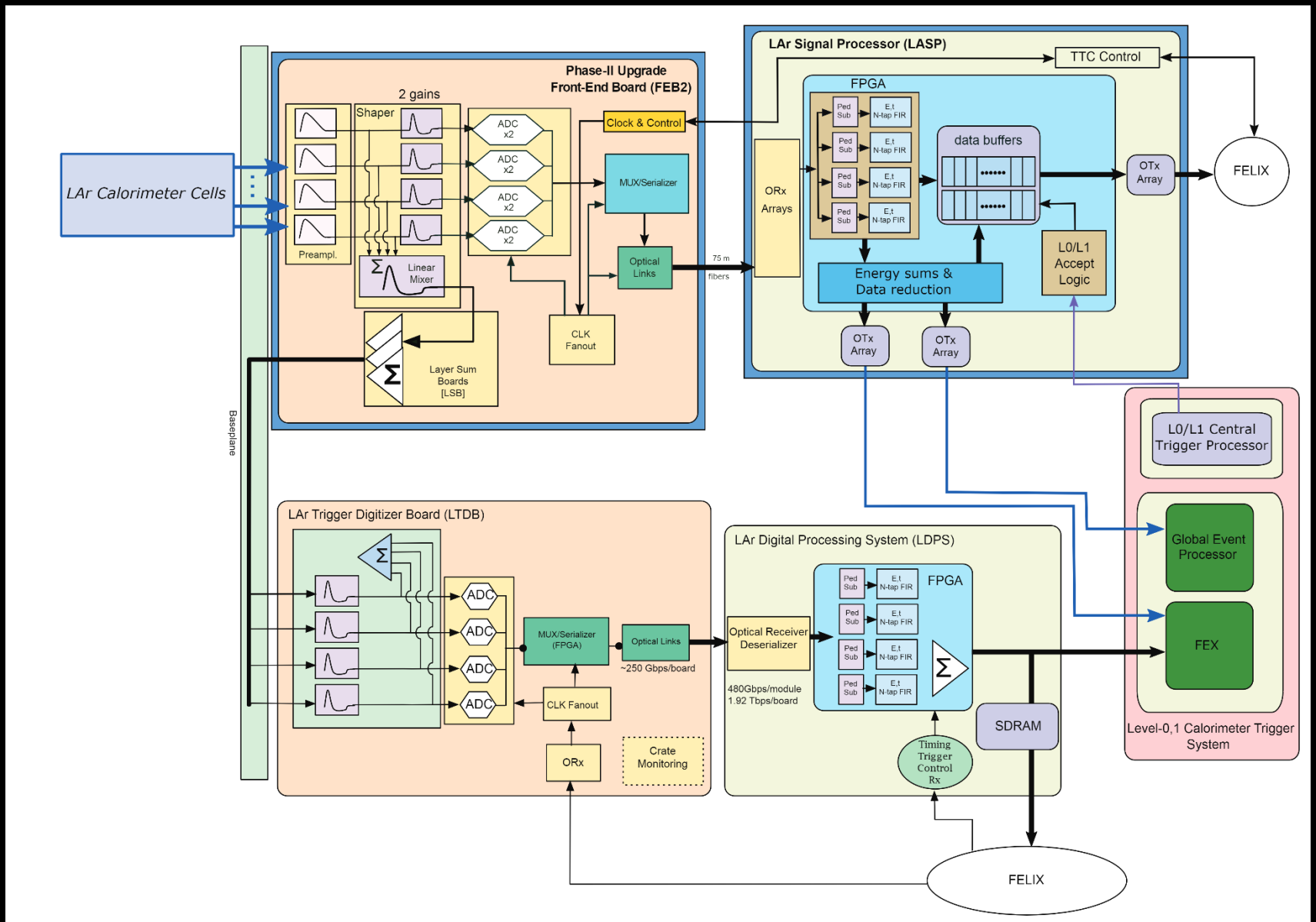
Requirements





- a system with two 14-bit ADCs, with gain ratio 30, can fulfil these requirements
  - electronics noise being typically 4 times larger than the LSB
  - quantization noise being a factor 5 to 10 lower than the LAr resolution at the gain-switching energy

New read-out architecture

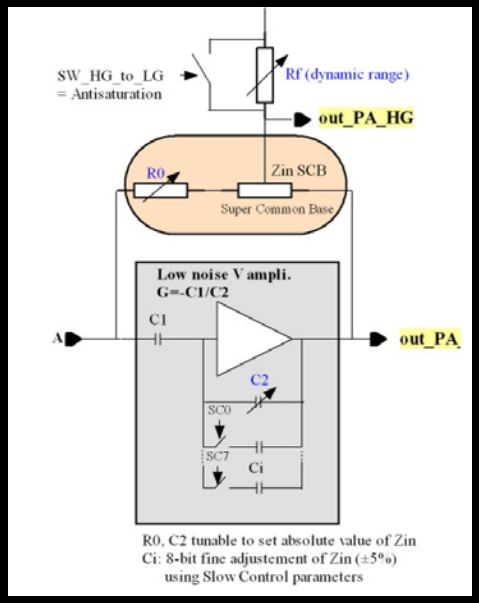


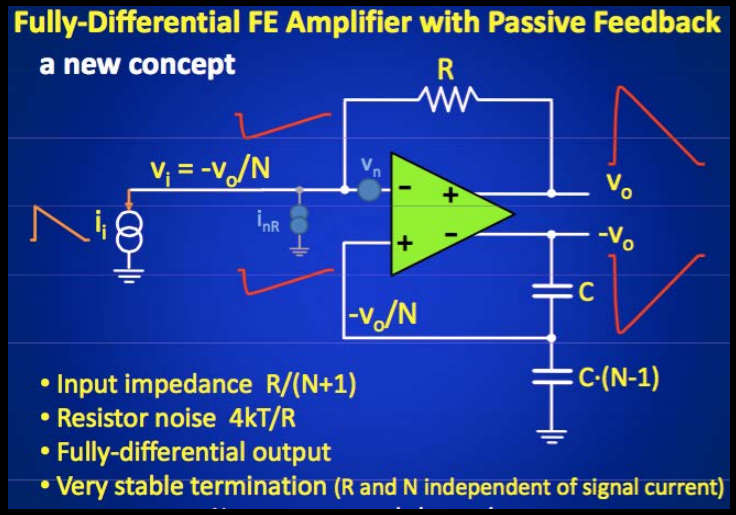
New readout electronics

- Two main boards: FEB2 and LASP boards
- FEB2:
  - located on crates attached to the calorimeter cryostats
  - 1524 boards, each board handles 128 calorimeter channels
  - provide input line termination, amplification, shaping, digitization and data shipping off detector for further processing
  - Main ASICs needed in new front-end board:
    - Preamplifier + shaper
    - ADC
    - Serializer
- LASP:
  - located off detector in counting room
  - receive digitized waveforms, apply digital filtering and buffer the data until a trigger decision is received
  - based on FPGA
  - baseline configuration: 186 boards are needed

Analog processing

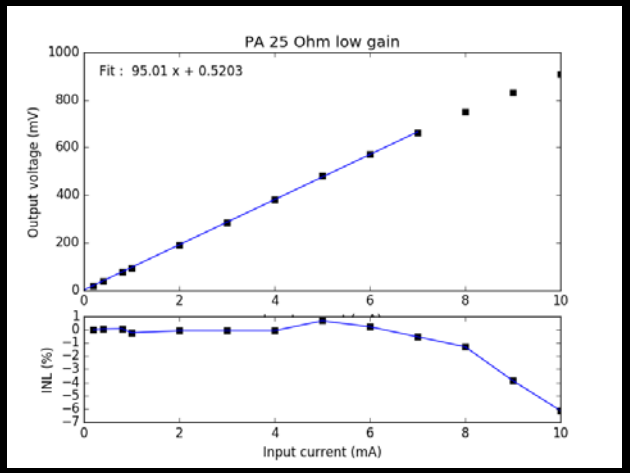
- Amplification of calorimeter signal + shaping
  - integrated in one single ASIC
- Two R&D's on-going with different technology and architecture
- 130 nm CMOS (TSMC)
  - Line terminating preamp with dual range output, electronically cooled resistor, Super Common Base amplifier
  - Test chip (preamp only) being measured, then irradiation and new submission which includes also shaper
- 65 nm CMOS (TSMC)
  - Fully differential amplifier with passive feedback
  - Pre-prototype received in July: includes preamp and shaper, programmable termination, 2 gains, programmable peaking time
  - Built-in ADC driver to interface to COTS or ASICS ADC for evaluation tests
- Common test stand developed
  - Will test both solutions against technical specifications and make a choice by end 2017

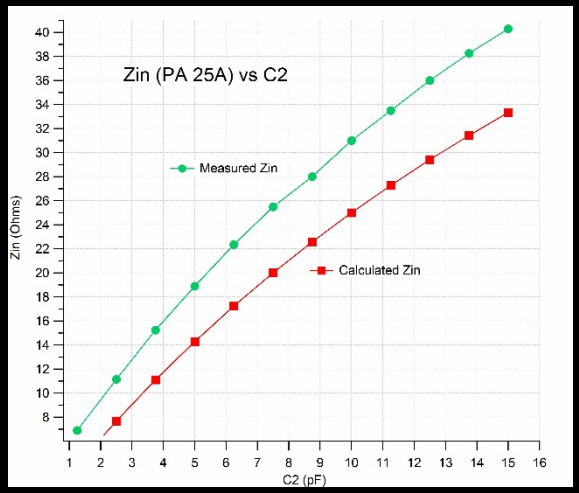




Tests of front end

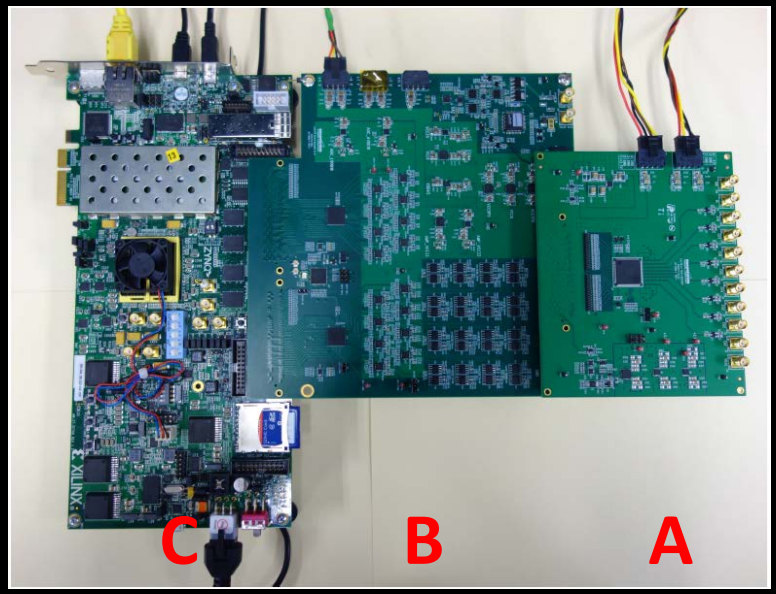
- 130 nm prototype test results
- Linearity ~0.1%,
  - within 1% up to 7 mA
- Measured about a factor of 2 more ENI than what is expected by simulation
  - Additional noise due to additional resistance in input transistor
  - new transistors designed (tests in November)





- 65 nm prototype being tested now

- Test stand in common for evaluate both front-end options:
- A: analog mezzanine
- B: digital test board
- C: control and DAQ board:
  - Xilinx ZC706 evaluation board

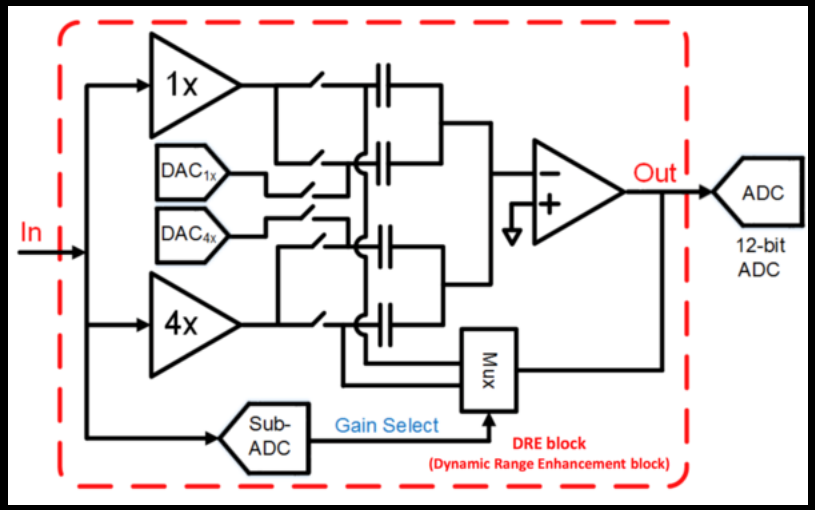


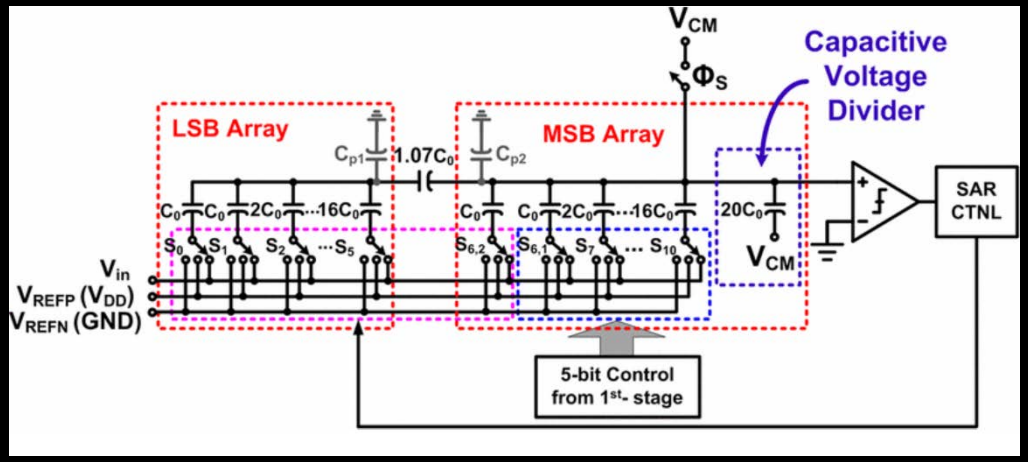
Digitization

- Digitize analog signal from each calorimeter cell at 40 Mega-Samples per Second, synchronized to the LHC bunch-crossing rate
- Cover full 16-bit dynamic range digitizing each channel with two gains, using an ADC with a 14-bit dynamic range
- Other requirements:
  - Radiation tolerance
  - integral and differential non-linearities below one least significant bit
  - less than 100 mW of power consumption per detector channel.
- Exploring both commercial and custom solutions
  - COTS: choice limited by cost and radiation tolerance
  - Custom: challenging design; design could be customized to ATLAS need

Digitization

- Custom design: 14-bit ADC in 65 nm process made from two parts:
  - Dynamic Range Enhancer block that determines the most significant 2 bits
  - 12-bit SAR (Successive Approximation Register) block
  - Test chip received in August, being tested now
  - Will be tested for functionality and then irradiated (total dose and SEU)





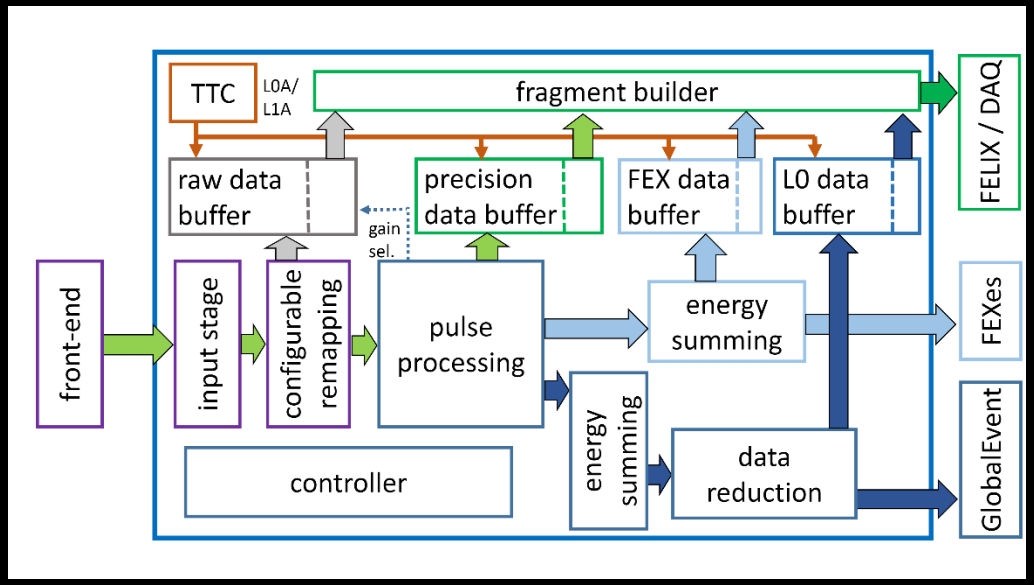
Digitization

- Commercial option: several commercial ADC tested for radiation
- Promising candidate: Texas Instruments ADS5294
  - octal 14-bit ADC, 60 mW (at 40 MSPS) consumption per channel
  - rad hard for HL-LHC expected doses
  - however SEE and SEFI (Single Event Functional Interrupt) were observed
- Estimate 10 SEE/min and 1 SEFI/min for the entire LAr system (about 50k ADC in total)
  - need to understand if maneageble

- IP block option: third, “intermediate”, option under consideration
  - purchase and use critical ADC IP blocks with proven analog performance, while still having the possibility to customize the digital interface as needed for integration with the FEB2.
  - Can also tailor IPs to meet needed radiation resistance, such as minimizing the quantity of ancillary logic and introducing triple-redundancy to minimize sensitivity to SEE
  - IPs that seem to fit our requirements in terms of digitazion speed, low power, effective number of bits will be evaluated in the coming months

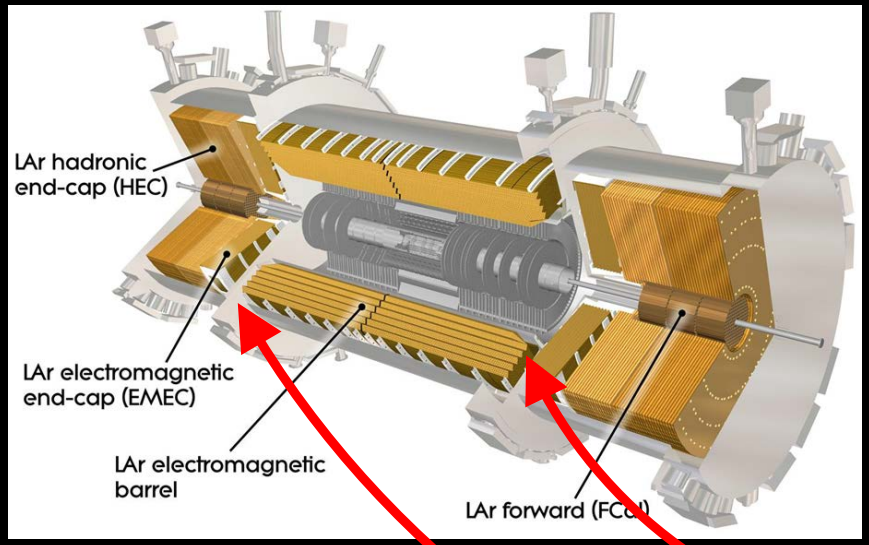
LAr Signal Processor system

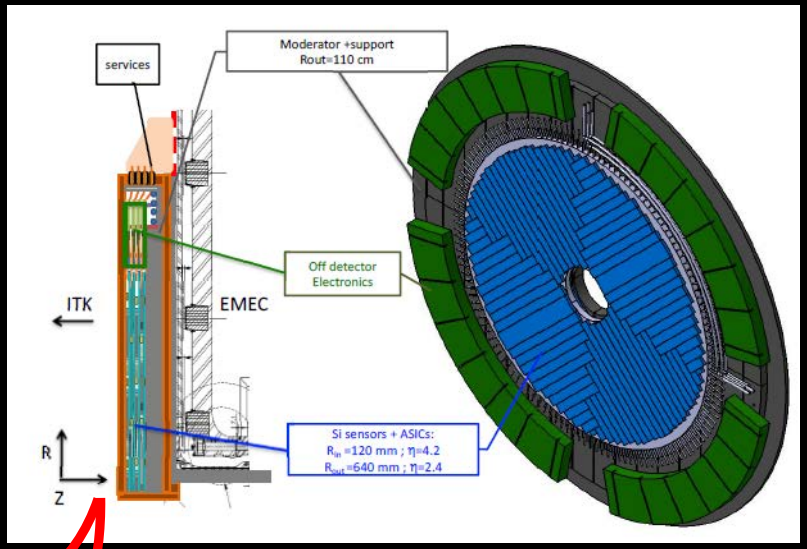
- The LASP system will receive the digitized waveforms off detector. The full data stream of detector signals digitized at 40MHz will be available in the LASP modules
- Main functionalities:
  - select between the two gains
  - apply digital filtering algorithms to reduce the effects of electronics noise and pileup noise
  - energy and time measurement of LAr signal pulses
  - buffer the data until a trigger decision is received
  - transmit the relevant data to the trigger and data acquisition (DAQ) systems



High Granularity Timing Detector

High granularity timing detector





- Timing detector to be placed at z = ±3.5 m from the interaction point, in front of the forward and EM endcap (inner wheel) calorimeters
- Provides time information for tracks/physics objects, complementing the spatial and p_T information provided by tracking and calorimeters
- At LHC vertices are distributed (Gaussian) with: σ_z = 5 cm (σ_t = 180 ps); with pile-up there are on average 1.6 vertices/mm
  - Tracking detectors provide resolution of primary vertices in forward region typically >1 mm, which leads to merging of up to 7 collision vertices
  - time detector with a resolution of 30 ps per MIP should be able to assign a vertex to each particle

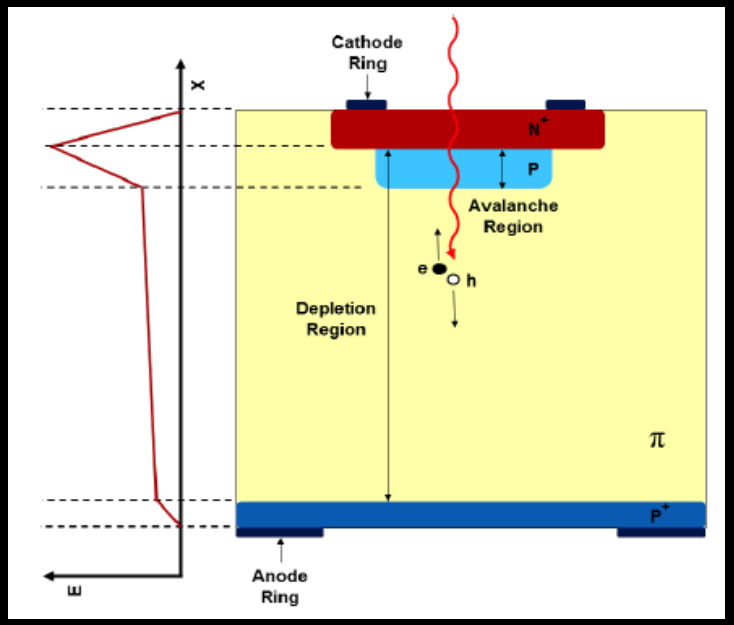
Design and requirements

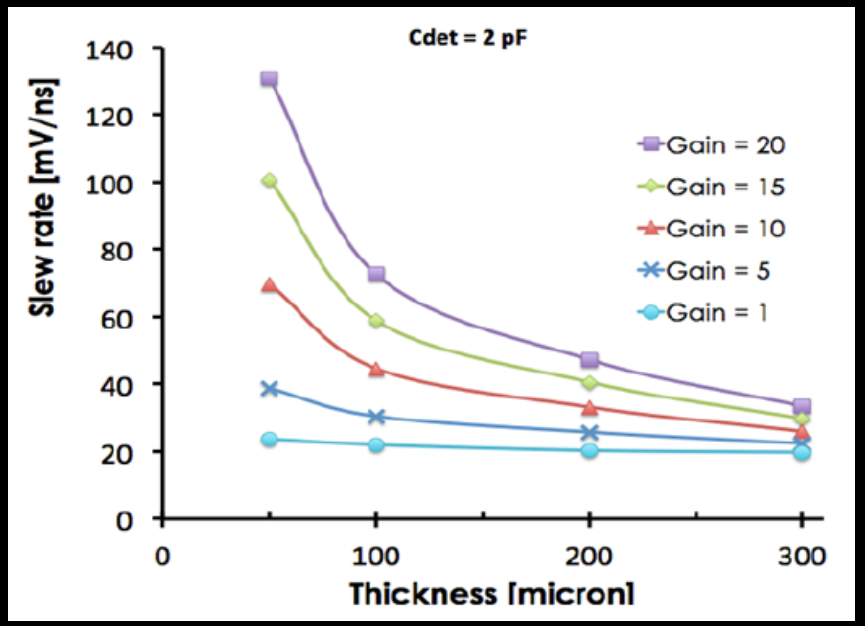
Pseudorapidity coverage	$2.4 < \|\eta\| < 4.2$
Position in z	$3420 < z < 3545$ mm including 50 mm of moderator
Position of active layers	$3435 < z < 3485$ mm
Radial extension (active area)	110–1100 mm (120 mm–640 mm)
Number of layers	4 per side
Time resolution	30 ps / mip (< 60 ps / mip / layer)
Sensor size	1.3×1.3 mm^2
Number of channels	6.3M
Number of Si modules (2×4 cm^2 each)	13952
Number of ASICs (2×2 cm^2 each)	27904
Total active area (Si sensors)	11.16 m^2

Table 1: Main parameters of the HGTD.

- 4 silicon layers (planes) in each endcap, made of Low Gain Avalanche Diode (LGAD) pads with an active thickness of 50 μm and a pad area 1.3 x 1.3 mm^2
- Big constraints coming from available space for the detector and radiation levels
- full z-envelope for detector including supports,... is only 75 mm
- at radius 120 mm: 9 x 10^{15} n_{eq} neutron fluences and 9 MGy (w/ safety factors)
  - plan to replace 20% sensors and ASICs (up to 300 mm) after about half of the expected doses
  - ⇒ requirement: 4.5 x 10^{15} n_{eq}/cm^2 and 4.5 MGy max

LGAD sensors





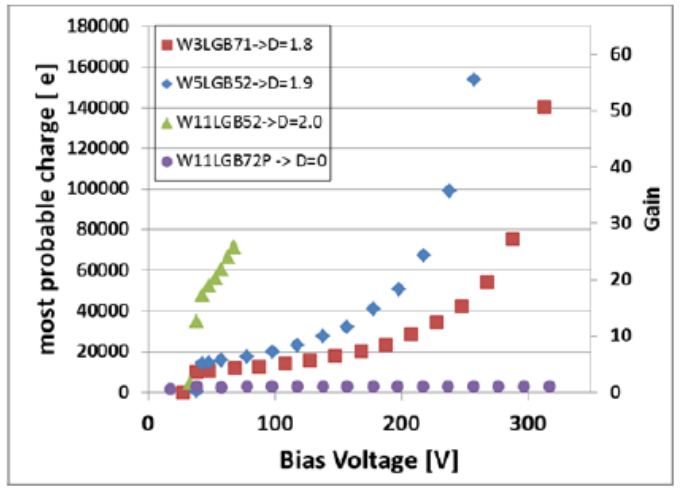
- LGAD are n-on-p silicon detectors containing an extra highly-doped p-layer below the n-p junction to create a high field which causes internal gain
- Targeting time resolutions of 60 ps/MIP on single layer, 30 ps/MIP with 4 layers
- Best time resolution favors thin sensors and large gain:
  - 50 μm thick sensors from simulations and beam tests
  - gain of about 20, compromise between good resolution and safe operation with a voltage not too near the breakdown voltage

LGAD sensors

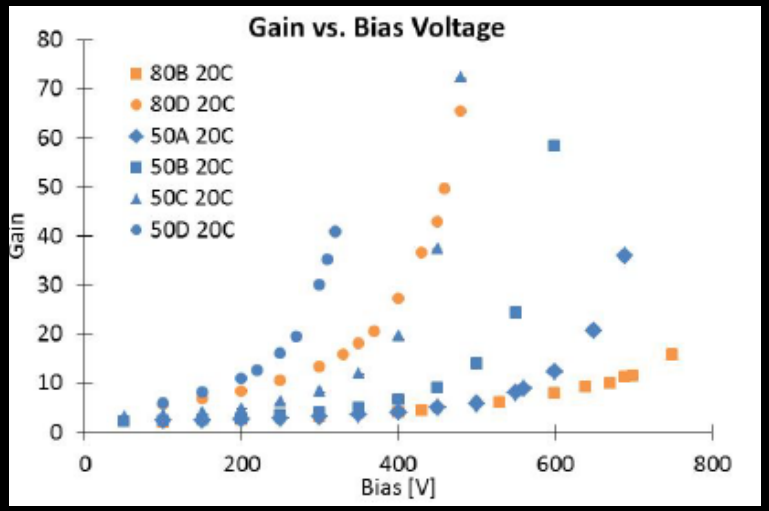
Manufacturer	Wafer size [inch]	Substrate	Thickness [μm]	Sensor types	Size [mm]	Technology enhancement
CNM	4" (2017 6")	Epi, SoI, Si-Si-bond	300, 75, 45	Single pads, 2x2 up to 8x8 array	1, 2, 3	B->Ga substitution C implantation
FBK	6"	Si-Si-bond	300, 50	Single pads, many arrays	1, 2, 3	B->Ga substitution C implantation
HPK	6"	Si-Si-bond	80, 50, 30	Single pads, 2x2 arrays	1, 3	<50 μm thick

- Several sensors studied from CNM, FBK and HPK
  - Various structures, size, doping dose tested from various production runs
  - Intense characterization in lab, test beam and after irradiation
  - overall good and consistent results from the devices

CNM

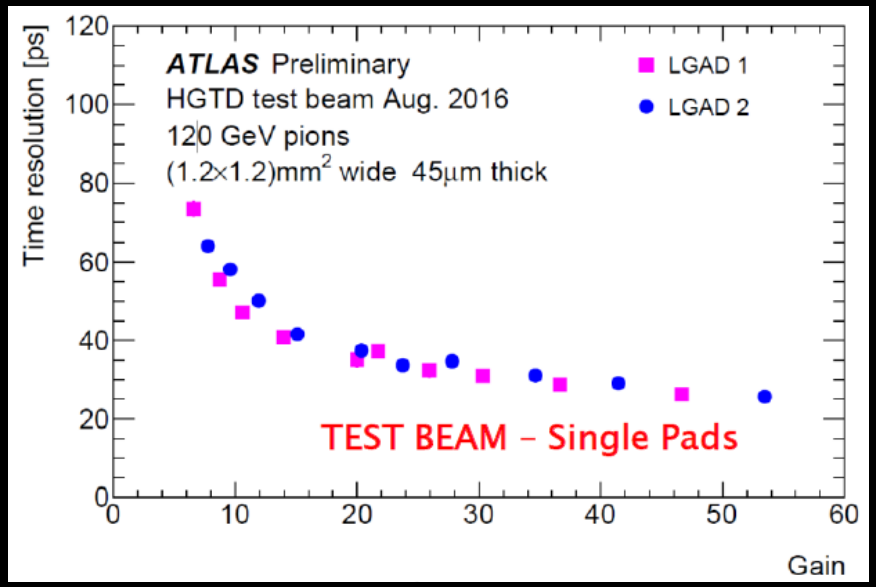


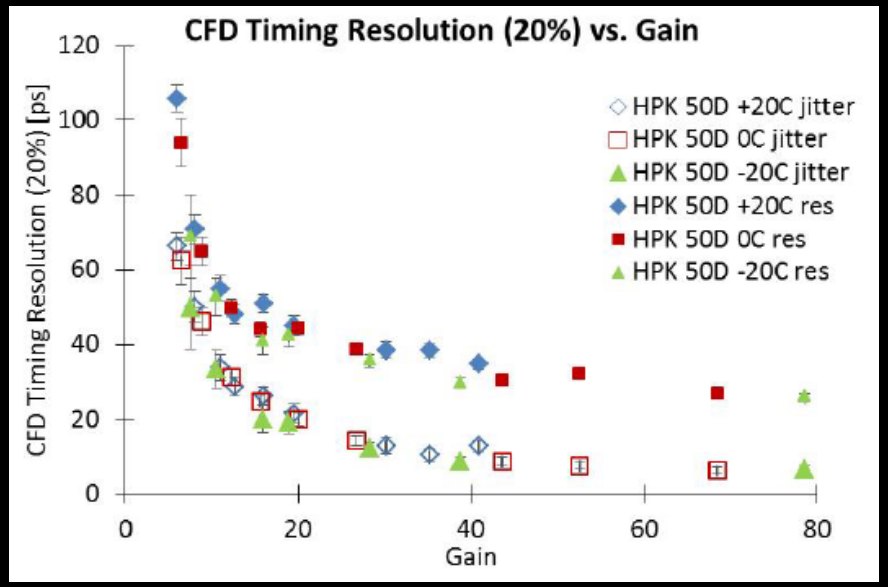
HPK



Timing resolution

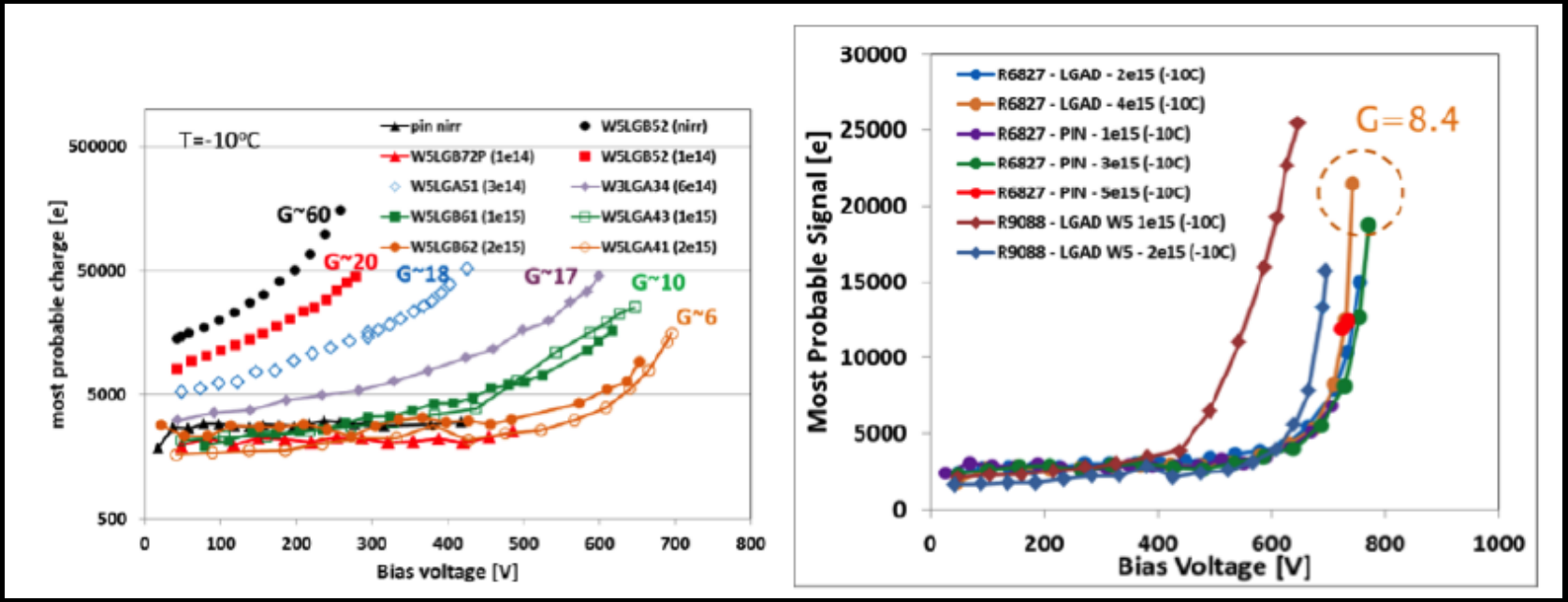
- Time resolution extensively studied in various beam
- Sub-30 ps time resolution can be achieved below the breakdown point before irradiation for the 1.3 x 1.3 mm^2 devices with about 4 pF capacitance
- Temperature dependence also studied
  - running at lower temperatures (< –20 °C) increases gain, reduces breakdown voltage and improves performance (time resolution, jitter)
  - Plan to operate at –30 °C



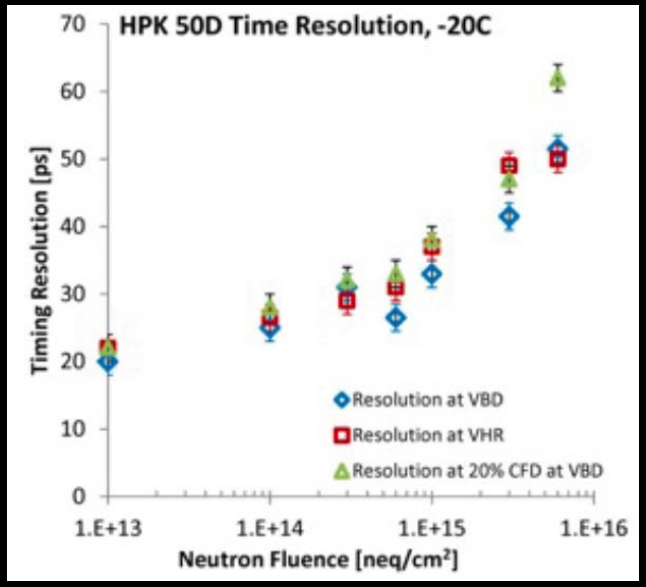


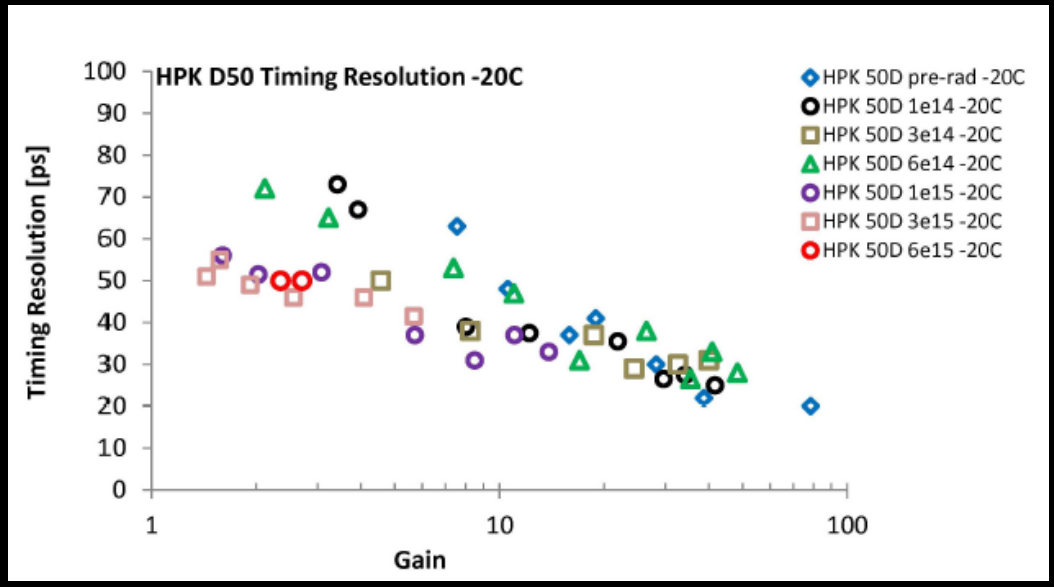
LGAD after irradiation

- Gain decreases with irradiation
  - loss of the effective doping concentration in multiplication layer due to deactivation of initial boron as acceptors
  - Beyond 2 x 10^{15} n_{eq}/cm^2 the multiplication layer has almost no effect, only bulk multiplication at high average fields, on device performance. Steep increase of charge with bias voltage: detectors are operated close to device breakdown



Time resolution after irradiation



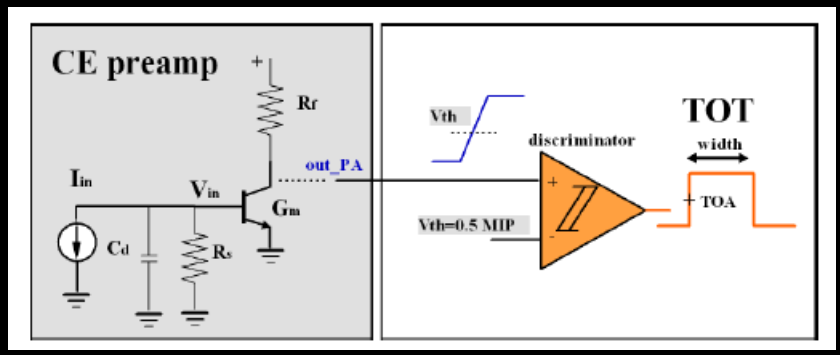


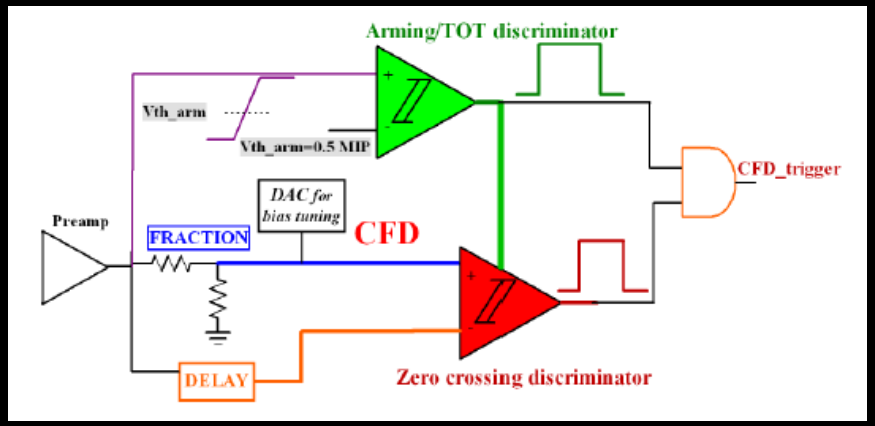
- Highly irradiated LGAD need high bias voltage, close to 700V
  - need higher bias voltage for a certain gain
- Gain relates directly to time resolution
- At highest fluences, multiplication in bulk leads to decreasing signal rise time, so leading to better time resolution at the same gain
  - from 20 ps pre-irradiation to 40 ps after 1 x 10^{15} n_{eq}/cm^2 to 50 ps after 6 x 10^{15} n_{eq}/cm^2 for HPK devices
- $\rightarrow$ Available LGAD sensors can be operated safely up to the fluence of 4.5 x 10^{15} n_{eq}/cm^2, keeping a time resolution of 50 ps (60 ps per layer required)
- However further LGAD developments in RD50 and CNM are on going to increase rad hardness by reducing the acceptor removal:
  - Ga or C (spray or diffused) in place of B, etc..

Readout electronics

- Sensors read-out by on-detector ASICs bump-bonded to the sensor
  - digitized ASIC output signals will be transferred through flex cables to the off detector electronics and finally to counting room with optical fibers
- ASIC consist in amplification, followed by discriminators, digitized by a TDC and stored in a memory until a trigger accept is received
- Strong requirements:
  - rad levels: some ASICS will be replaced during detector lifetime
  - dynamic range: simulated with electrons in the detector
  - time jitter: < 20 ps
  - low power
- To correct for the time walk dispersion, two methods (one will be chosen):
  1. the amplitude of the pulse needs to be measured. Measure the pulse width, which is proportional to the amplitude with a TOT discriminator
  2. Use a Constant Fraction Discriminator (CFD)

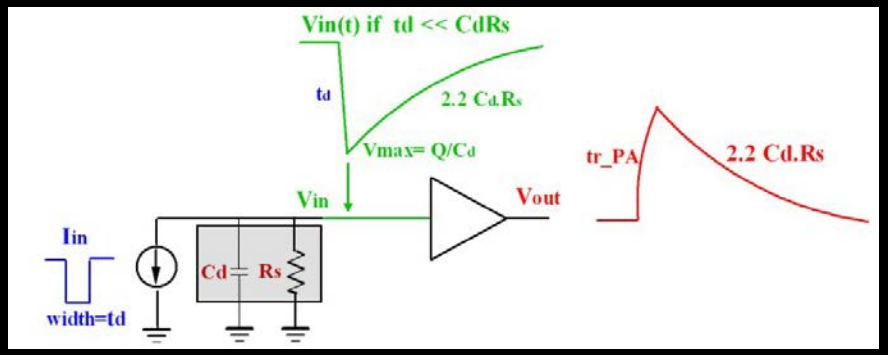
Pad size	1.3×1.3 mm^2
Detector capacitance	3.4 pF
TID and neutron fluence	Inner region: 4.5 MGy, 4.5×10^{15} n / cm^2 Outer region: 2.1 MGy, 4.0×10^{15} n / cm^2
Number of channels/ASIC	225
Collected charge (1 mip) at gain=20	9.2 fC
Dynamic range	20 mips
(preamplifier+discri) jitter at gain = 20	<20 ps
Time walk contribution	< 10 ps
TDC binning	20 ps (TOA) and 40 ps (TOT)
TDC range	2.5 (TOA) and 10 (TOT) ns
Number of bits / hit	7 for TOA and 9 for TOT
Luminosity counters per ASIC	7 bits (sum) + 5 bits (outside window)
Total power per area (ASIC)	<200 mW/cm^2 (<800 mW)
e-link driver bandwitdh	320 Mb/s, 640 Mb/s and 1.28 Gb/s

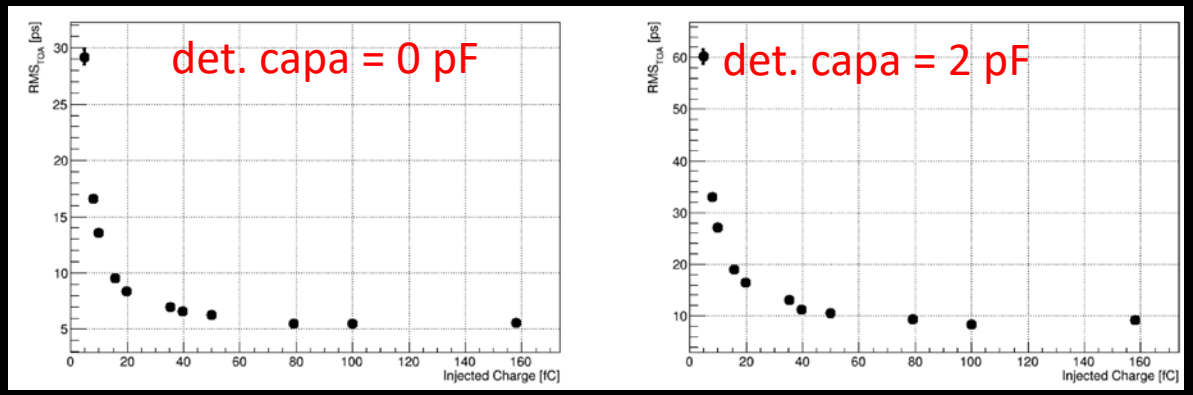




Prototype measurement

- First prototype (ALTIROC 0) in TSMC 130 nm with preamp, TOT and CFD (no TDC yet):
  - eight channels, four optimised for 2 pF detector (corresponding to a previous design of 1 x 1 mm^2 pad size)
  - also used for tests of bump bonding to sensors
  - will be used for test in lab and at test beam
- Preliminary test bench measurements:
  - voltage test pulses with rise time less 100 ps injected through a 100 fF capacitor
  - test results varying the injected charge 5-160 fC
  - discriminator threshold at 2.5 fC (25% of a MIP for a LGAD with gain=20)
- Only TOT used so far, CFD not yet satisfactory



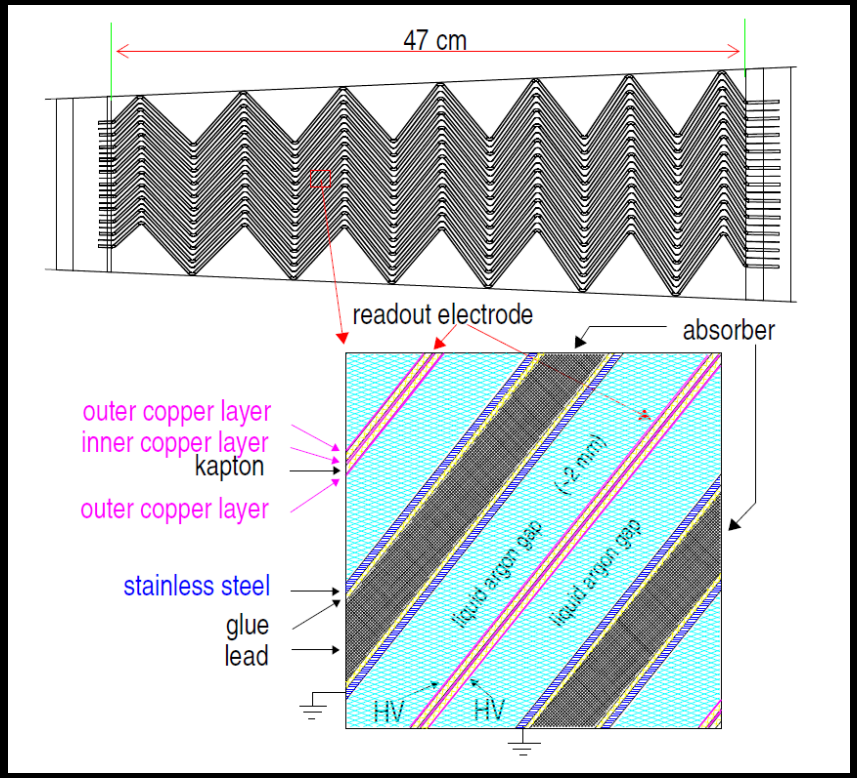


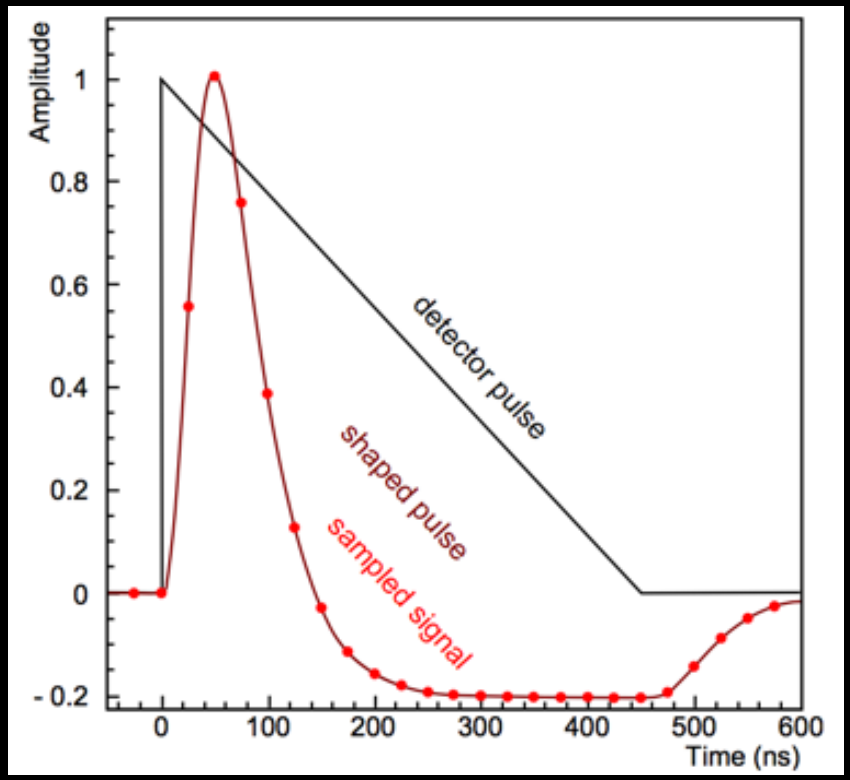
Conclusions

- The challenging conditions of operation at HL-LHC require substantial upgrades of the ATLAS detector
- Status reports on two of these upgrades have been presented:
  - upgrade of the readout electronics of the Liquid Argon calorimeter
  - new High Granularity Timing Detector for pile-up suppression in the forward region
- The projects are progressing well and latest development in several areas have been presented
- The Liquid Argon electronics upgrade is reaching a major milestone with the submission of its Technical Design Report this week
- The HGTD project just undergo an Initial Design Review that will lead to the preparation of a Technical Design Report in late 2018

Back-up

Signal in LAr





LAr electronics dynamic range

Layer	Presampler		Front		Middle		Back	
$\|\eta\|$ range	<0.6	>0.6	<0.8	>0.8	<0.8	>0.8	<0.8	>0.8
MIP values [MeV]	–	–	50	35	250	300	–	–
µA GeV^{-1}	0.84		2.67	3.16	2.67	3.16	2.67	3.16
Current electr.								
Preamp. max. current [mA]	1		1		5	10	5	
Max. energy [GeV]	1190		375	317	1873	3165	1873	1582
Req. for HL-LHC								
Max. current from 5 TeV Z' [mA]	<0.05	0.51	0.84	0.81	5.36	7.86	0.91	0.90
Max. current from jets [mA]	<0.05	0.23	0.57	0.78	6.78	7.13	1.63	2.42
Max. from both [mA]	<0.05	0.51	0.84	0.81	6.78	7.86	1.63	2.42

Table 3.2: Characteristic values for the LAr electromagnetic barrel cells: typical energies from MIP, maximum currents and energies allowed by the existing electronics, and new estimations of the maximum input currents as obtained in simulation.

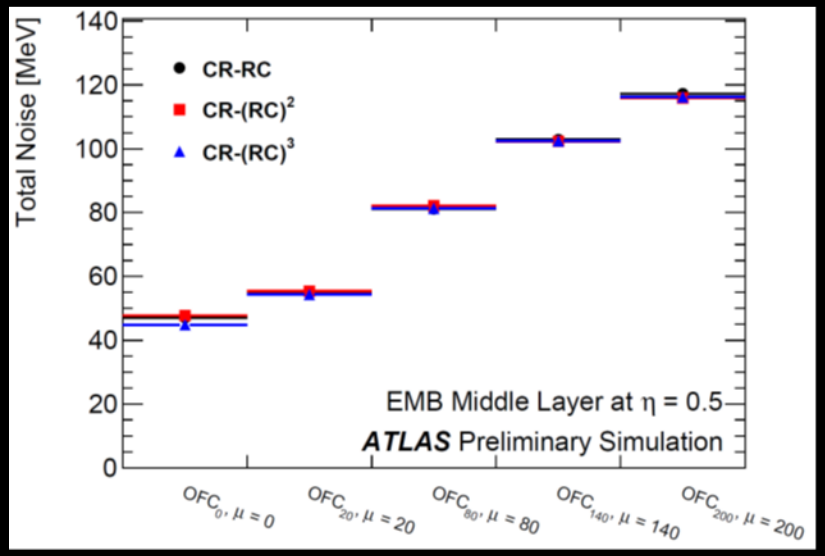
Layer	Presampler	Front		Middle		Back	
$\|\eta\|$ range	<1.8	<2.0	>2.0	<2.0	>2.0	<2.0	>2.0
MIP values [MeV]	–	42 – 32	20 – 10	250	240 – 300	–	–
µA GeV^{-1}	0.28	2.26–2.69	2.71–3.01	2.26–2.66	2.69–2.94	2.33–2.65	2.68–2.92
Current electr.							
Preamp. max. current [mA]	1	1		10		5	
Max. energy [GeV]	3570	442–372	369–332	4425–3759	3717–3401	2146–1887	1886–1712
Req. for HL-LHC							
Max. current from 5 TeV Z' [mA]	0.11	1.90	1.41	7.15	7.68	0.22	0.77
Max. current from jets [mA]	0.09	1.61	0.61	6.16	3.30	0.89	1.50
Max. from both [mA]	0.11	1.90	1.41	7.15	7.68	0.89	1.50

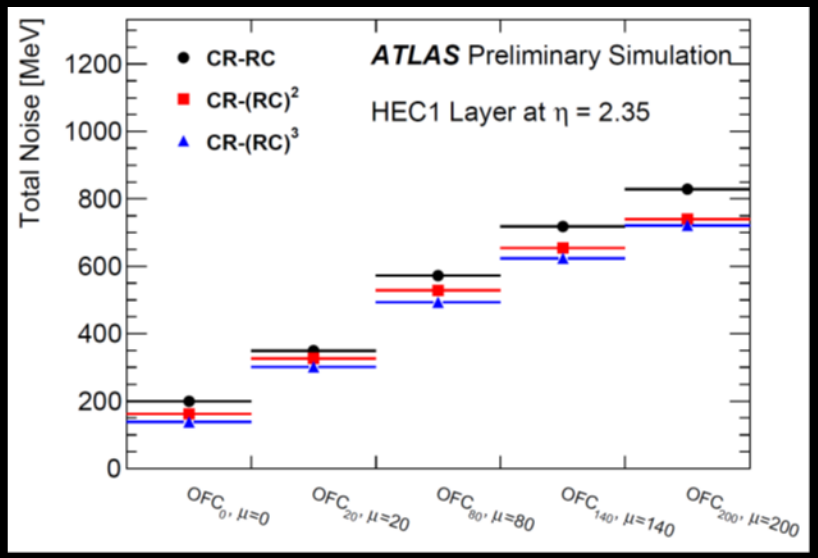
Table 3.3: Characteristic values for the LAr electromagnetic endcap cells of the outer wheel ($|\eta| < 2.5$): typical energies from MIP, maximum currents and energies allowed by the existing electronics, and new estimations of the maximum input currents as obtained in simulation.

Data transmission

- The ADC data need to be serialized and transmitted from the on-detector FEB2 boards to the off-detector LAr Signal Processor (LASP) boards using optical links.
  - Add BCID info
- 14-bit ADC word reformatted at 16 bits and serialized at a rate of 640 Mbps
- Total date rate per FEB2 of 163.84 Gbps
  - 128 chs x 2 gains x 640 Mbps
- Will use lpGBT and Versatile Link+ for optical links:
  - lpGBT is a 65 nm CMOS (TSMC), lower power and higher bandwidth version of GBT chip
- Estimate 22 lpGBT/FEB for data transmission

Digital filtering

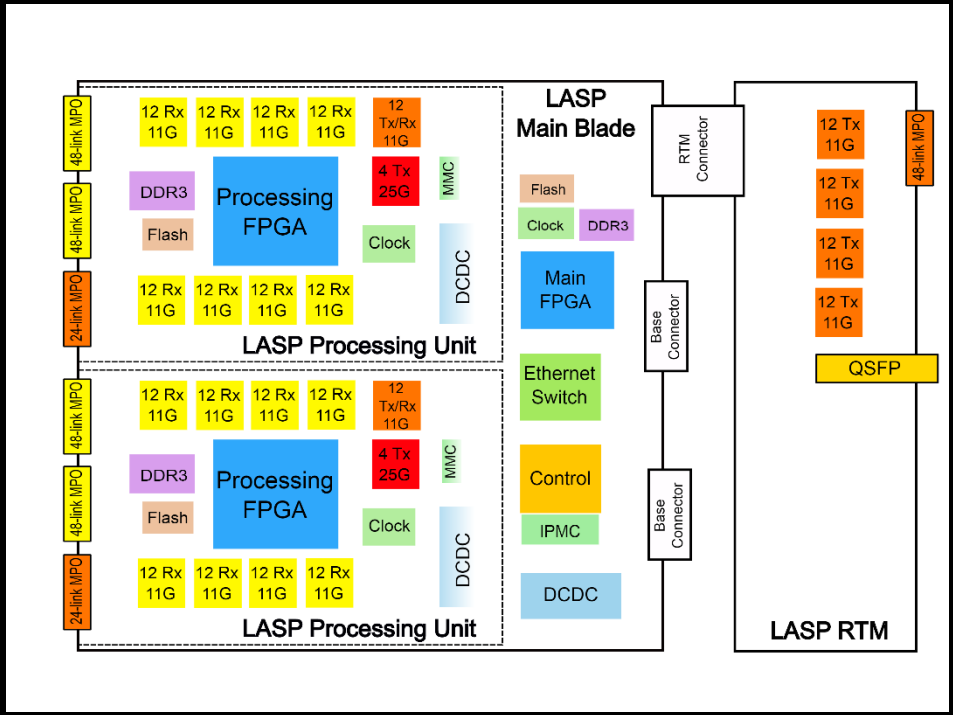




- Total noise as a function of pile-up levels for different shaping functions
- Optimal filter coefficients (OFC) are recalculated for each case
- OFC to a large extent cancel the difference in analog shaping

LASP board

- LASP boards will be realized in full-size ATCA format and based on high performance FPGA connected via high-speed links to electro-optical receivers and transceiver arrays with additional memory and clock distribution devices
- One LASP will receive data from 4 FEB2 boards
- With 512 channels input, input data rate is 655.4 Gbps per LASP processor FPGA



ASICS: next steps

- ALTIROC 0 ASIC will be characterized on test benches and in test beam in Autumn 2017 to gain experience whith the analog part
- Next iteration, ALTIROC 1, expected to be submitted in February 2018.
- This chip will contain:
  - 16 or 25 channels (still to be defined)
  - Both the analog and digital part of the single pixel read-out
  - Variants of CFD and TDC architectures to compare performances
- Will be extensively tested in Summer 2018
- Final ASICS will integrate 255 channels