The Trigger Readout Electronics for the Phase-1 Upgrade of the ATLAS Liquid-Argon Calorimeters

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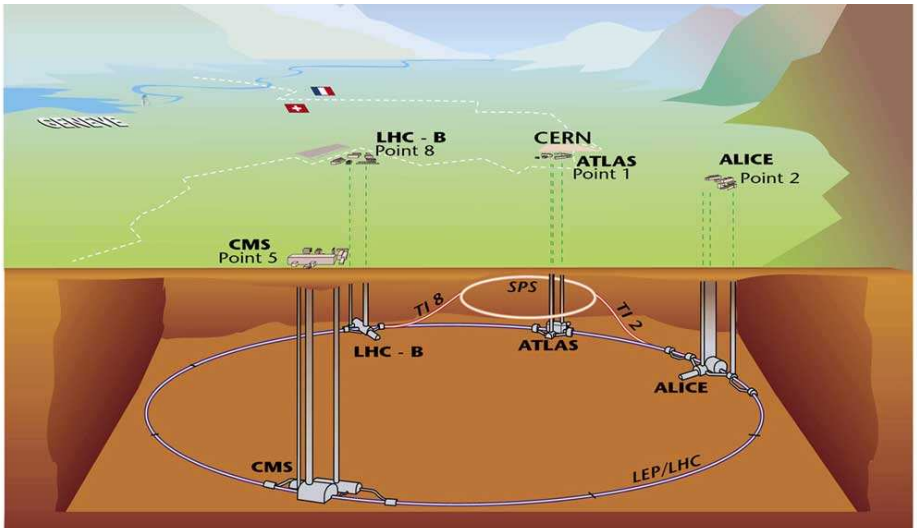
Outline

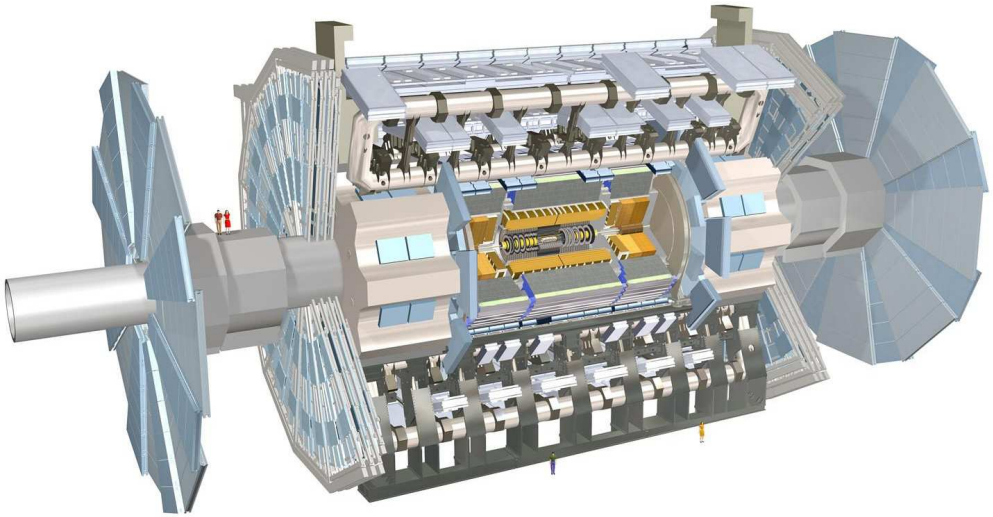
1. Introduction
   - LHC, ATLAS and LAr Calorimeter
   - Phase-1 upgrade
2. Front-End electronics
   - Baseplane, FEBs and LSBs
   - LTDB
3. Back-End electronics
   - LArCarrier Board
   - LATOME
4. LAr Demonstrator
   - LTDB and ABBA
   - calibration and data-taking

The LHC and the ATLAS experiment

the LHC (Large Hadron Collider)



the ATLAS (A Toroidal LHC ApparatuS)



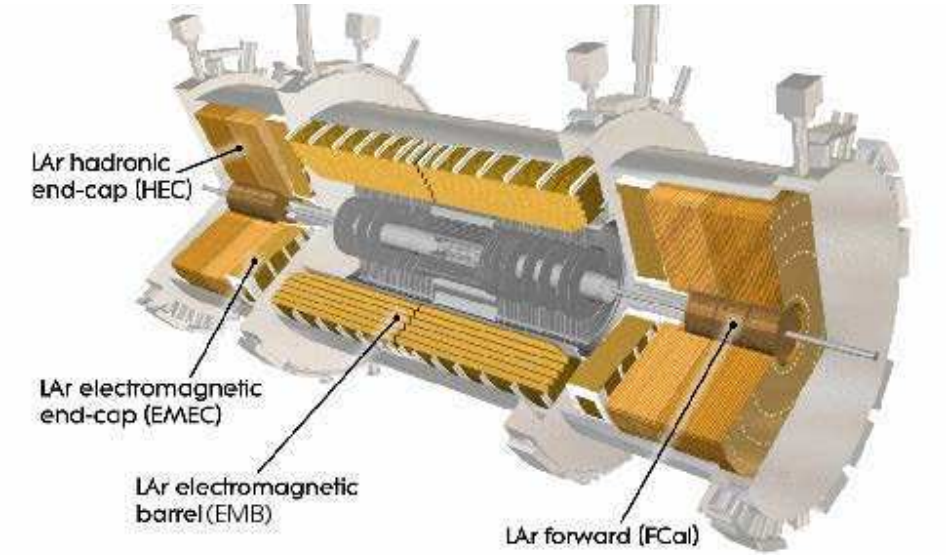
- at CERN, Geneva, Switzerland
- 27 km circumference
- four collision points

- multi-purpose detector: study the fine structure of the universe
- 44 m long, 25 m diameter & 7k tons

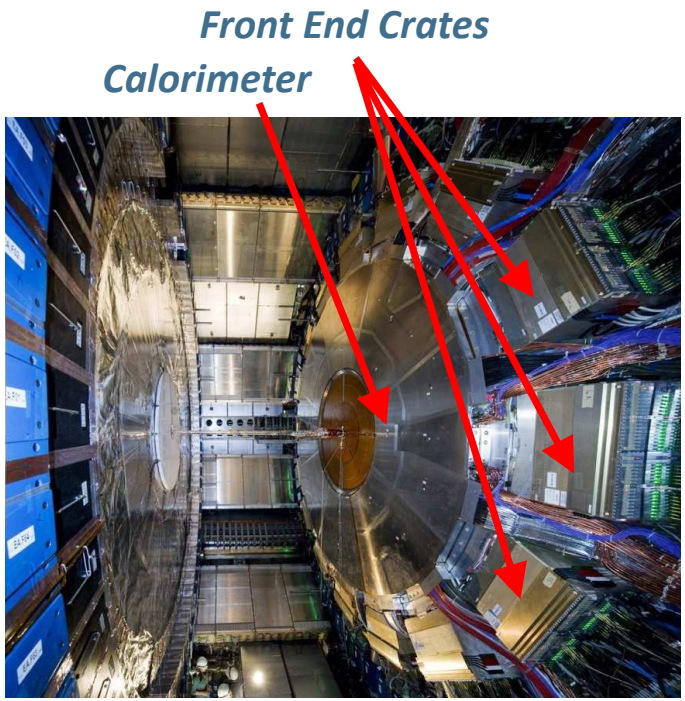
- Pixel and strip detectors, electromagnetic and hadronic calorimeters, muon chambers, solenoid and toroidal magnet systems: a total of 88 M channels.
- discovery of the Higgs boson in 2012
- since 2015 proton-proton collisions with increased energy & luminosity (Run 2) (p-p collisions at 13 TeV and 40 MHz)

Liquid Argon Calorimeter (LAr)

- LAr calorimeter is sampling calorimeter with Liquid Argon as active medium
  - EM barrel and end-caps: accordion shaped lead absorbers and copper/kapton electrodes
  - HEC: Copper absorbers and copper/kapton electrodes
  - FCAL: Copper absorbers (EM section) and Tungsten absorber (Hadronic sections)

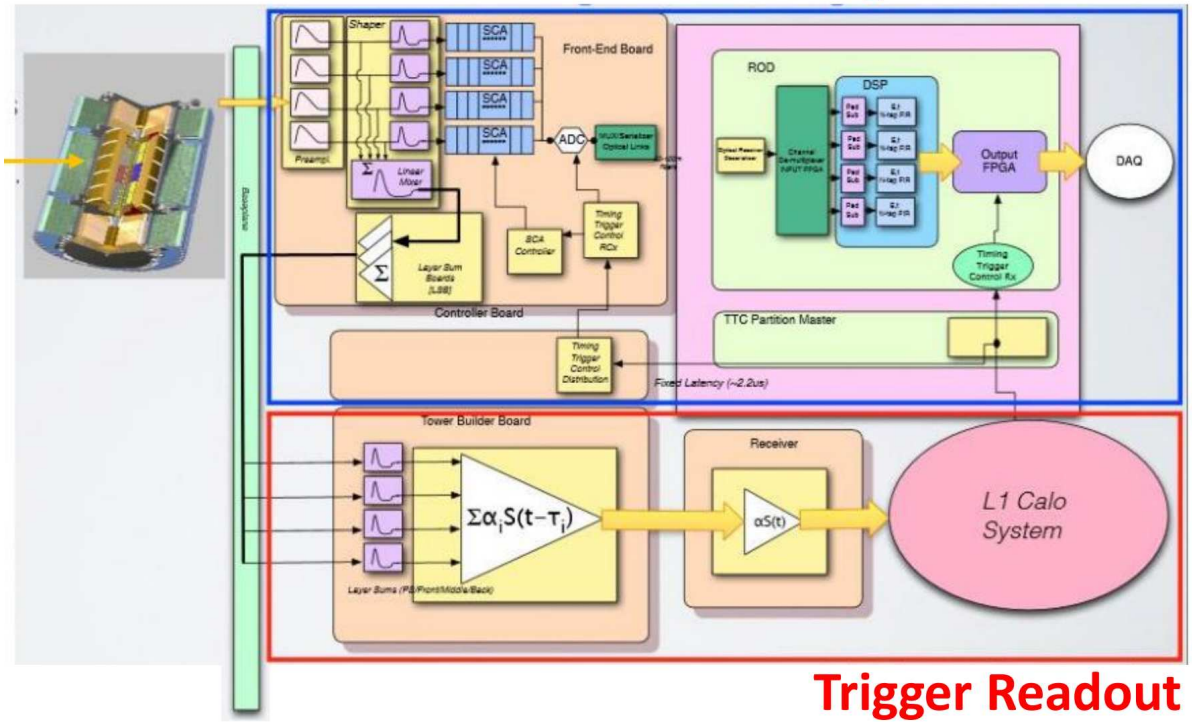


- **LAr calorimeter : 182k channels**
- **Front End : 1600 Front End Boards**
- **Back End : 200 Readout Out Driver boards**



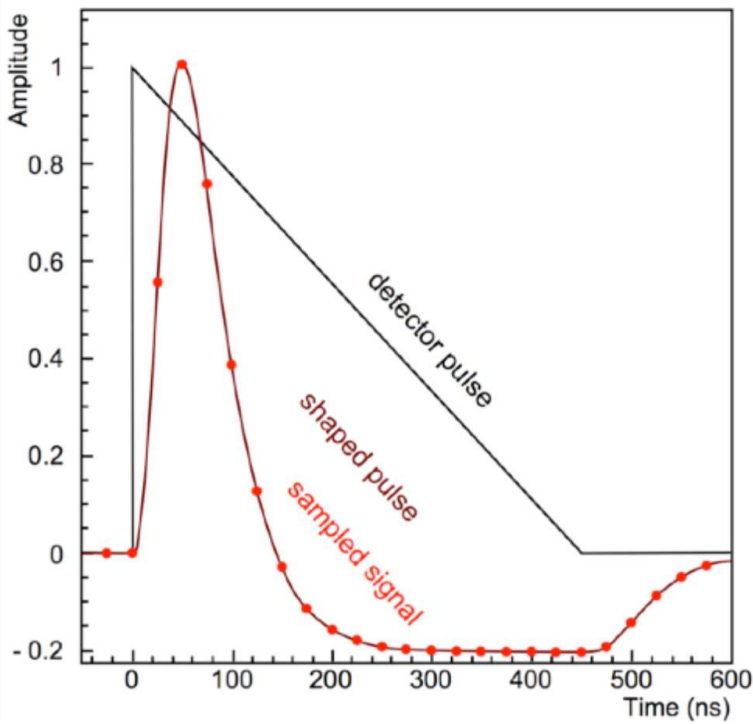
- crucial role in electron and photon reconstruction as well as jet identification and missing transverse energy measurement

Current LAr readout electronics



Regular readout (full granularity):

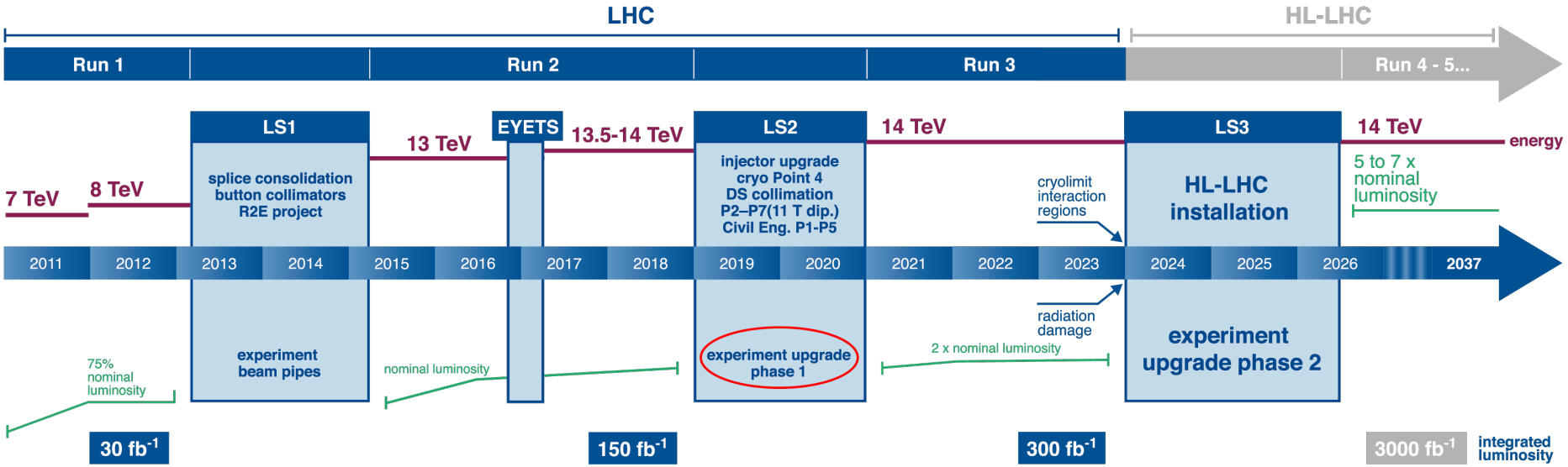
- cell signals amplified, shaped and sampled at 40 MHz
- signals digitised and data transmitted at 100 kHz upon L1 trigger decision



Trigger readout (reduced granularity):

- summing signals on Layer Sum Board (LSB)
- Tower Builder Board (TBB) to form trigger towers
- analog signals sent to L1 Calo system

Upgrade plans for LHC and ATLAS



Run 2 (current) conditions:

- max instantaneous luminosity $1.74 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$
- average number of interactions $\langle\mu\rangle \approx 25$
- 25 ns bunch spacing (40 MHz)
- L1 trigger bandwidth: (max.) 100 kHz; delay $\leq 3\,\mu\mathrm{s}$

Phase-1 upgrade 2019-2020 (LS2):

- inst. lumi. $\approx 3 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$
- $\langle\mu\rangle \approx 80$

$\rightarrow$ upgrade LAr trigger readout

Phase-2 upgrade 2024-2026 (LS3):

- inst. lumi. $\approx 7.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$
- $\langle\mu\rangle \approx 200$
- max. hardware trigger rate at 1 MHz

$\rightarrow$ upgrade LAr main readout

Motivation for upgrade of trigger readout

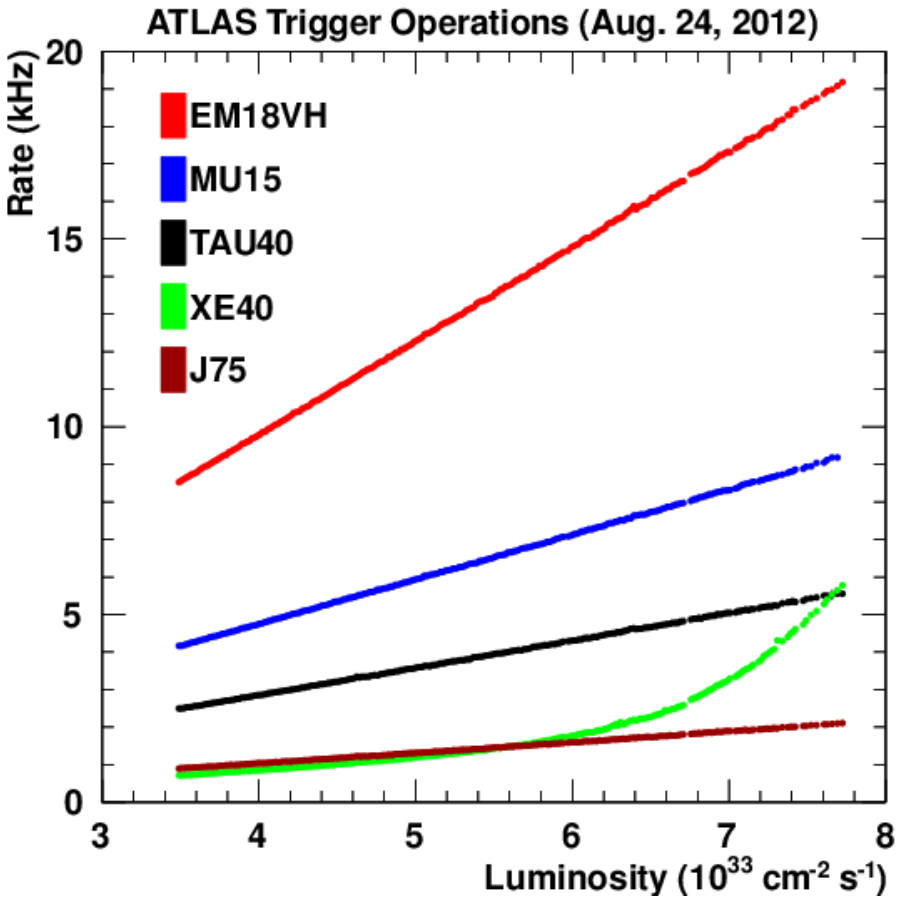
- lepton trigger rates increase linearly with luminosity
- forward-jet and missing E_T trigger rates increase exponentially
- but given level 1 (L1) trigger rate for single EM trigger is max. 20 kHz

→ increase p_T thresholds

- cuts out interesting physics!

→ improve (L1) trigger inputs

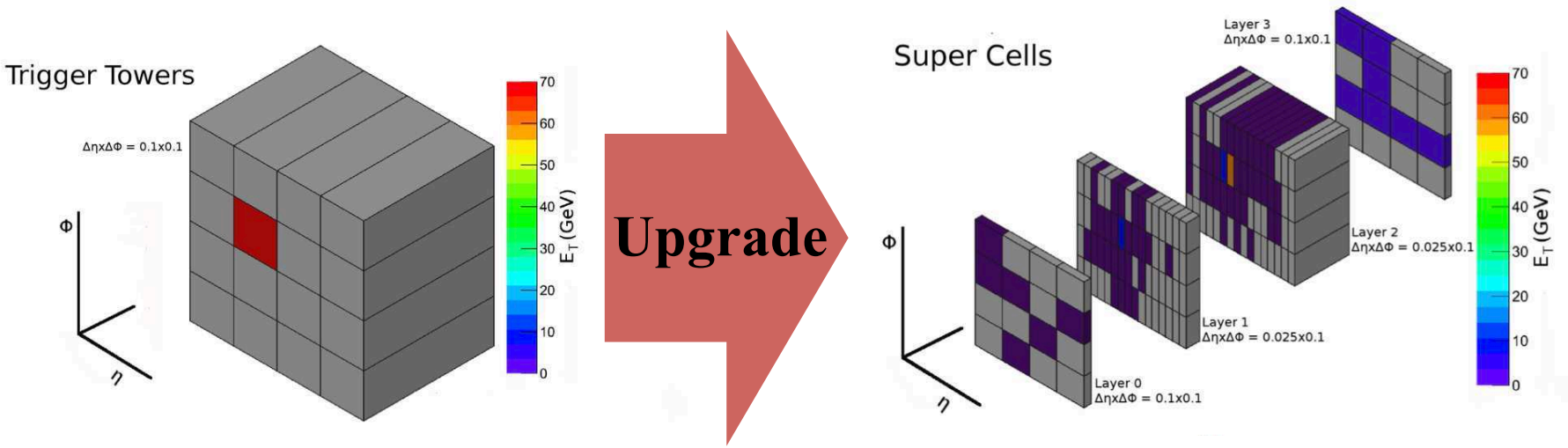
- higher granularity in LAr Calorimeter readout



From trigger towers to super cells

- width of electromagnetic shower is $\sim$ 0.08, which is smaller than current EM Trigger Towers ($\Delta\eta \times \Delta\phi = 0.1 \times 0.1$)

simulation of electron with transverse energy of 70 GeV

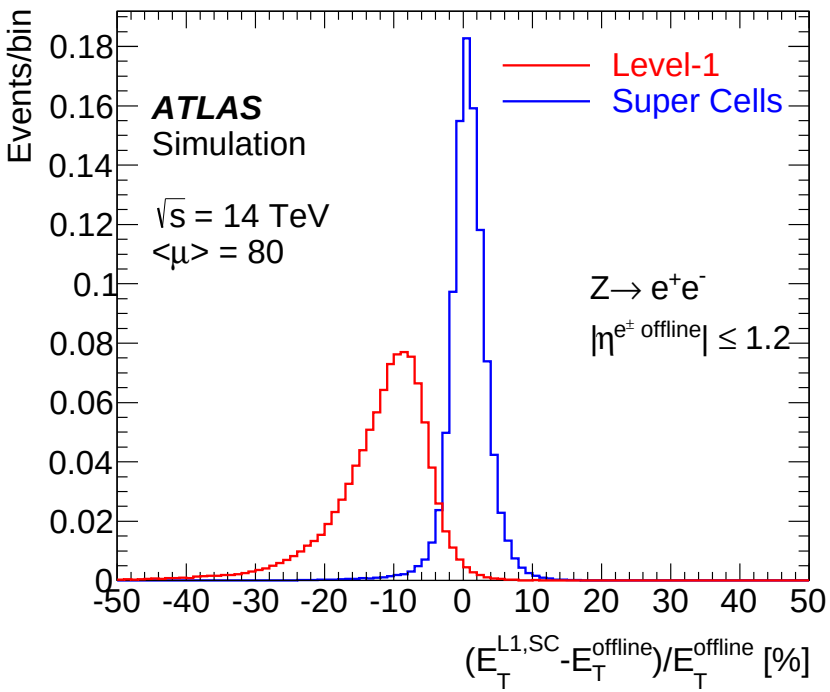


- increase of granularity in readout by factor 10 $\rightarrow$ super cells
- add longitudinal shower information to the level 1 trigger input $\rightarrow$ layers

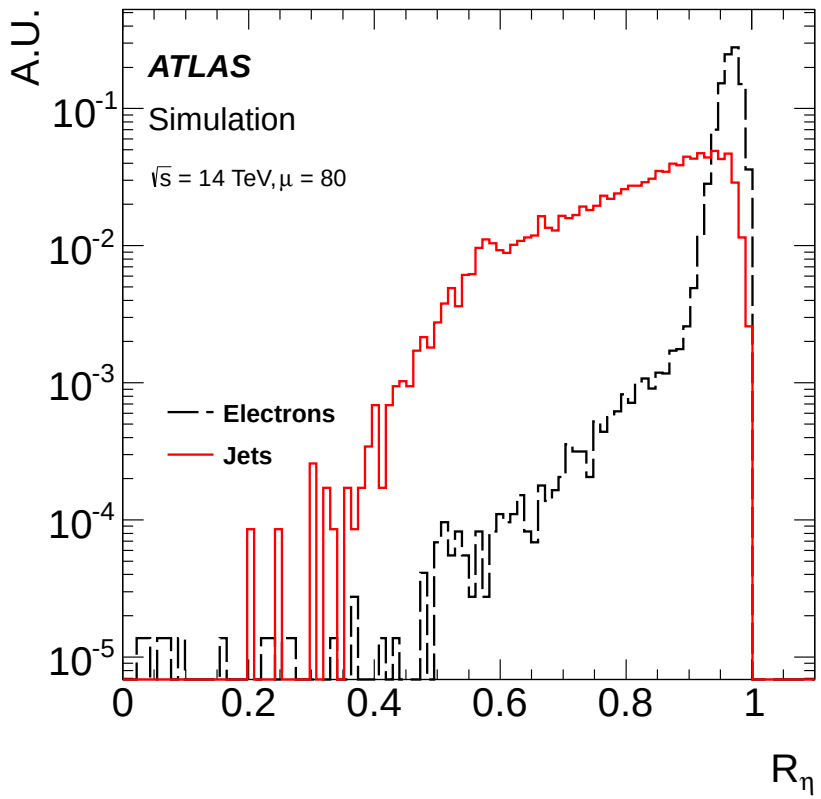
$\rightarrow$ apply (some) offline reconstruction algorithms already at level 1

Physics (simulation)

- improve electron reconstruction at level 1 stage



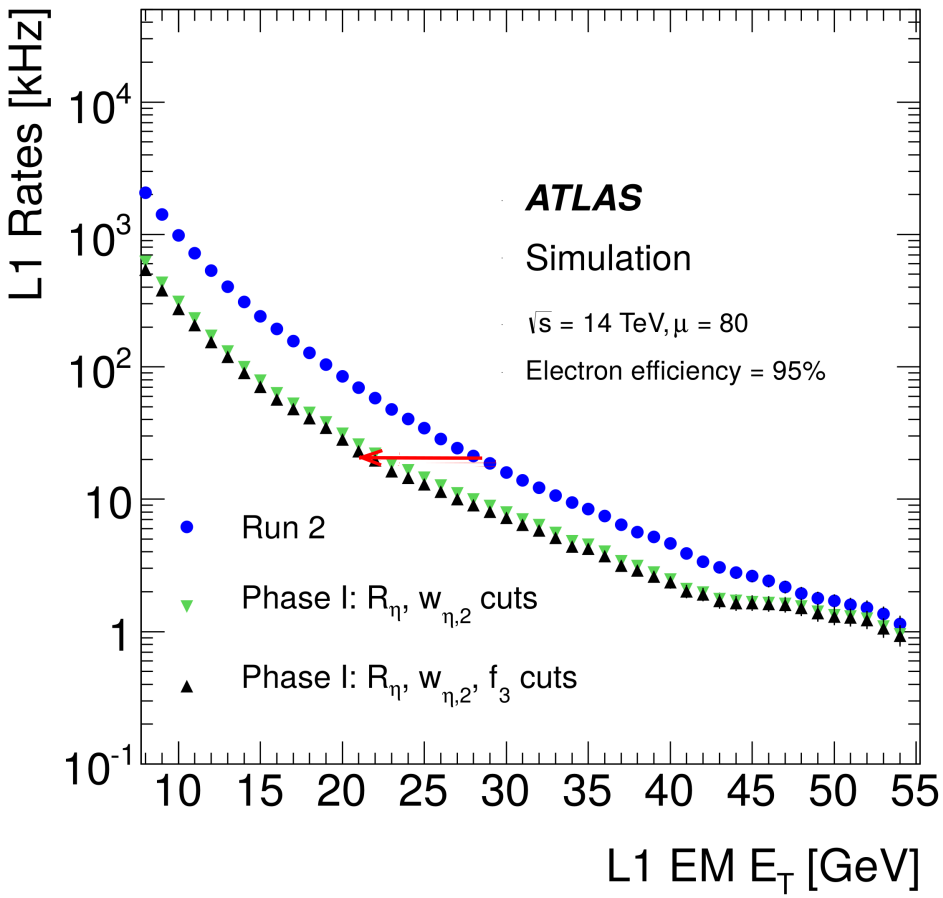
- improve jet rejection by new discriminant variables like R_η



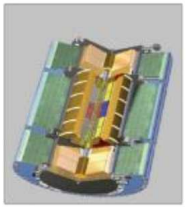
(R_η is transverse energy measured in the 3 × 2 group divided by 7 × 2 group in Middle layer)

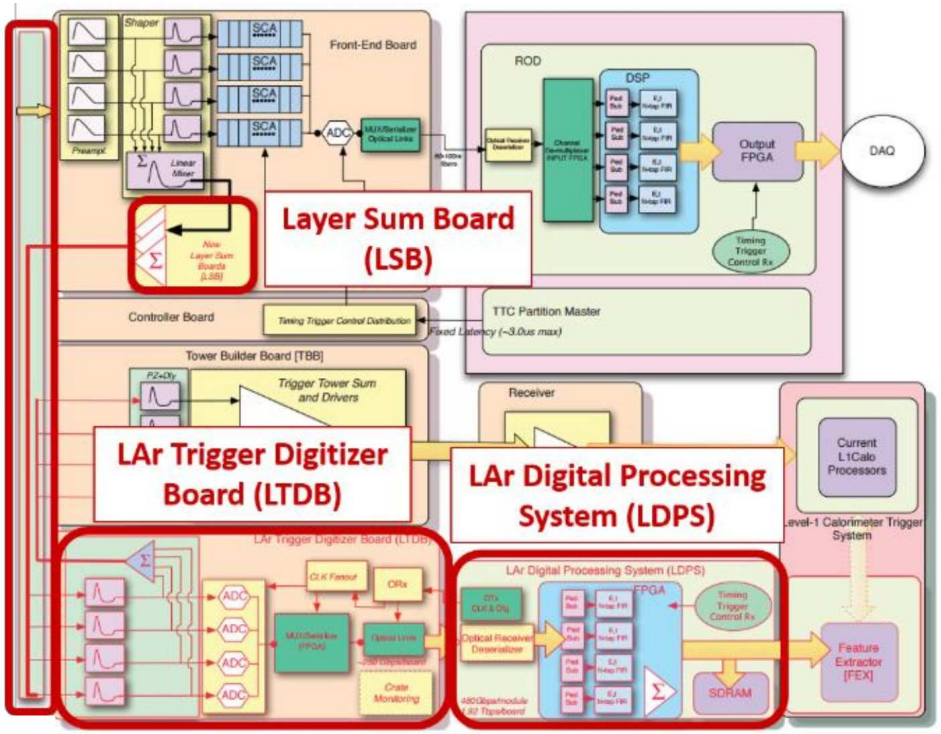
Physics (simulation)

- improve electron reconstruction at level 1 stage
- improve jet rejection by new discriminant variables like R_η
- reduction of L1 EM thresholds on transverse energy by $\sim$ 10 GeV compared to Run 2 (same rate)



Upgrade of LAr calorimeter readout electronics (Phase-1)





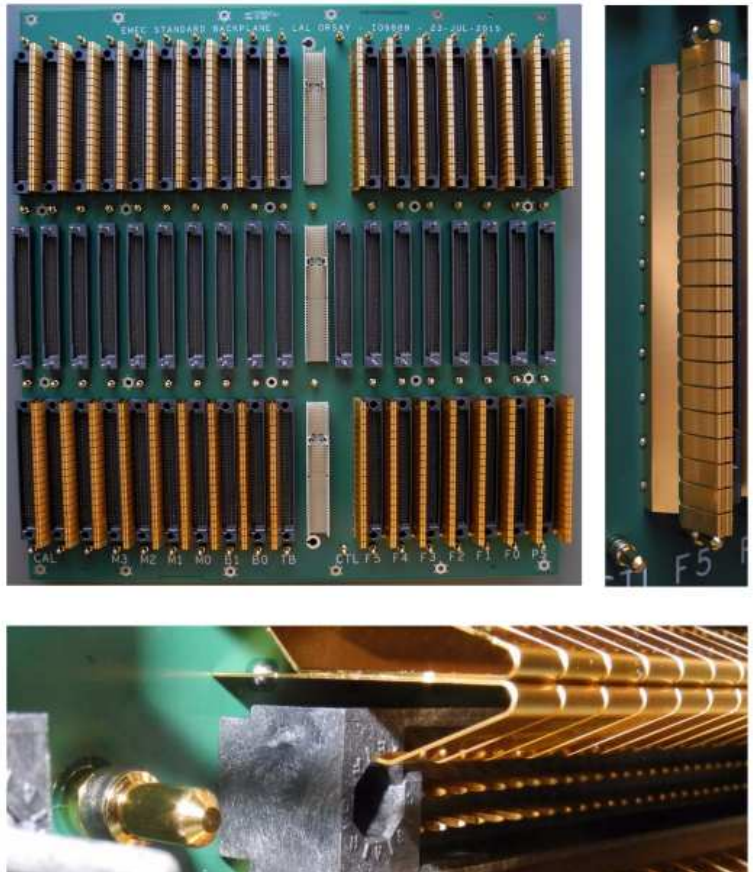
Needs to be replaced:

- new Layer Sum Boards (LSB) to perform analog sums for super cells
- new Baseplane to keep compatibility with existing set-up and route new super cell signals (10 times more signal lines)

- LAr Trigger Digitizer Boards (LTDB)
  - receive, digitize (continuously at 40 MHz) and send the super cell signals to the Back-End system
- LAr Digital Processing System (LDPS)
  - calculates the transverse energy of each super cell and various sums of super cells at fixed latency
  - sends the results at 40 MHz to the L1Calo trigger boards (FEX)
- old analog trigger path will remain for backup while commissioning

Front-End electronics: Baseplane, FEBs and LSBs

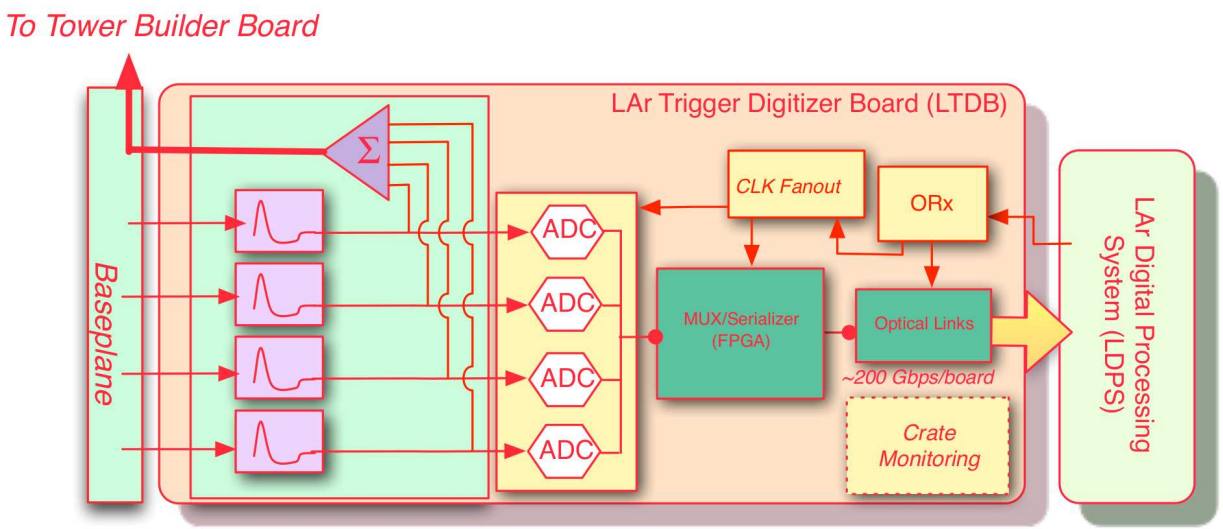
- Standard baseplanes (64 EMB, 32 EMEC):
  - verified connectivity, crosstalk, and noise performance with prototype
  - production has started
- Special (EMEC, HEC and FCAL) progressing
- common parts procurement is underway (ground springs, alignment pins)

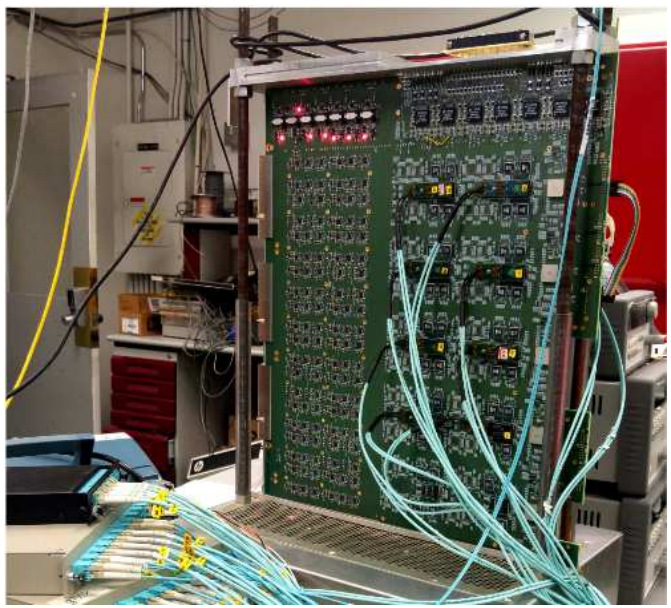


- Front-End Boards (FEB) will remain unchanged until Phase-2, but
- Layer Sum Boards (LSB) will be replaced to comply with super cell building:
  - e.g. in EM Barrel: creating analog sums of 4 (Presampler), 8 (Front-), 4 (Middle-) or 8 (Back-layer) channels to super cells
  - production is ongoing

Front-End electronics: LAr Trigger Digitizer Boards (LTDB)

- Total of 124 LTDBs reading 34k super cells
  - each LTDB reads up to 320 super cells
  - digitization of analog signals with 12 bits @40 MHz, with 80 custom ADCs
  - digital signals transmitted using 40 optical links @ 5.12 Gbps with custom ASICs (LOCx2 + LOCId)
  - 5 GBTx (serializer-de-serializer) links for Trigger, Timing and Control (TTC) signals
  - power distribution board (PDB) with total consumption ~125 W
  - compatibility with Phase-2 upgrade





- whole system is on-detector, all parts need to be radiation-tolerant
- final design has been fixed and prototype is being produced

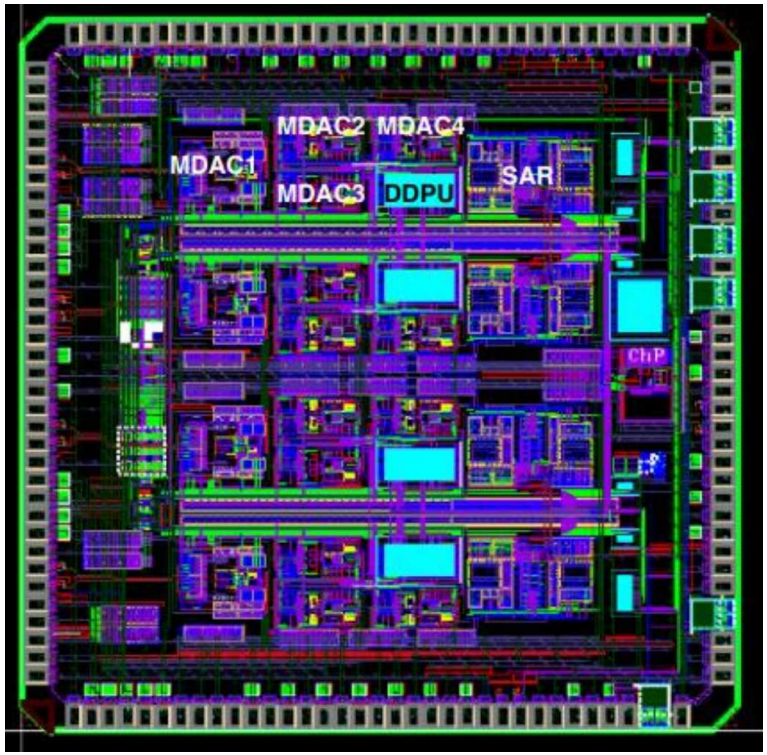
Front-End electronics: LTDB – Custom ADC

Requirements:

- calorimeter signals continuously sampled and digitized at 40 MHz
- four channels per chip
- power dissipation $<$ 50 mW per channel
- latency must be less than 200 ns
- radiation-tolerant
- dynamic range of 11.7 bits

NevisADC:

- 4 MDAC for most significant bits,
- SAR ADC for lower 8 bits
- tested for radiation up to 10 Mrad (100 krad expected at HL-LHC)

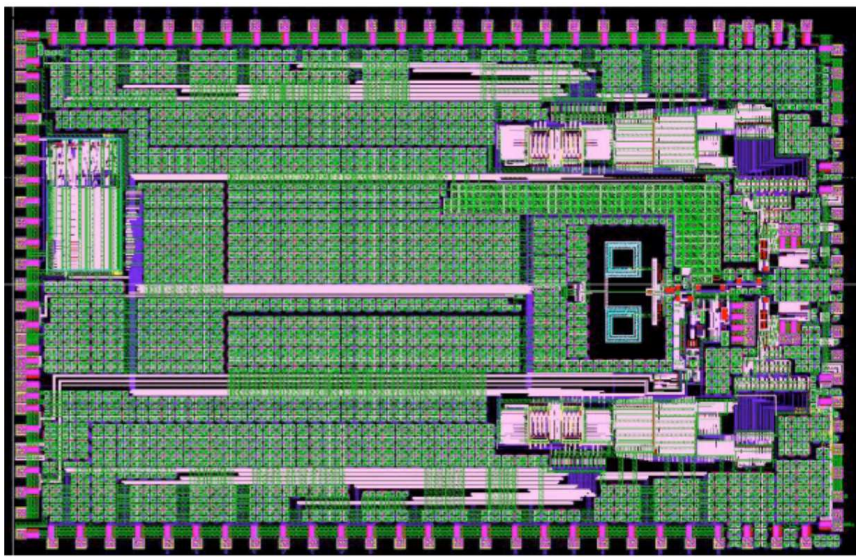


- IBM8RF 130nm CMOS
- 3.6 x 3.6 mm
- 72 pins QFN

Front-End electronics: LTDB – Optical Links

LOCx2 (Serialiser)

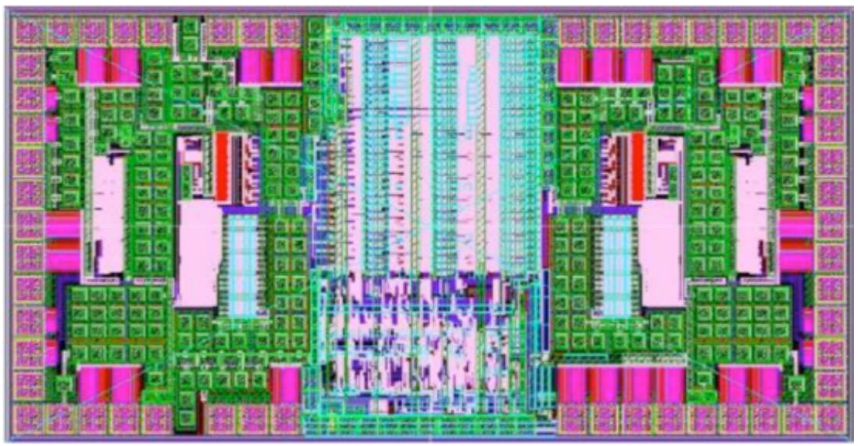
- 250 nm Silicon-on-Sapphire
- Dual-channel 8 x 14 bits
- Output at 5.12 Gbps
- Power consumption: 1 W
- Latency < 75 ns



Die: 6.0 x 3.7 mm, 100 pins QFN

LOCId (Laser driver)

- same technology as LOCx2
- Dual-channel VCSEL driver



Die: 2.1 x 1.1 mm, 40 pins QFN

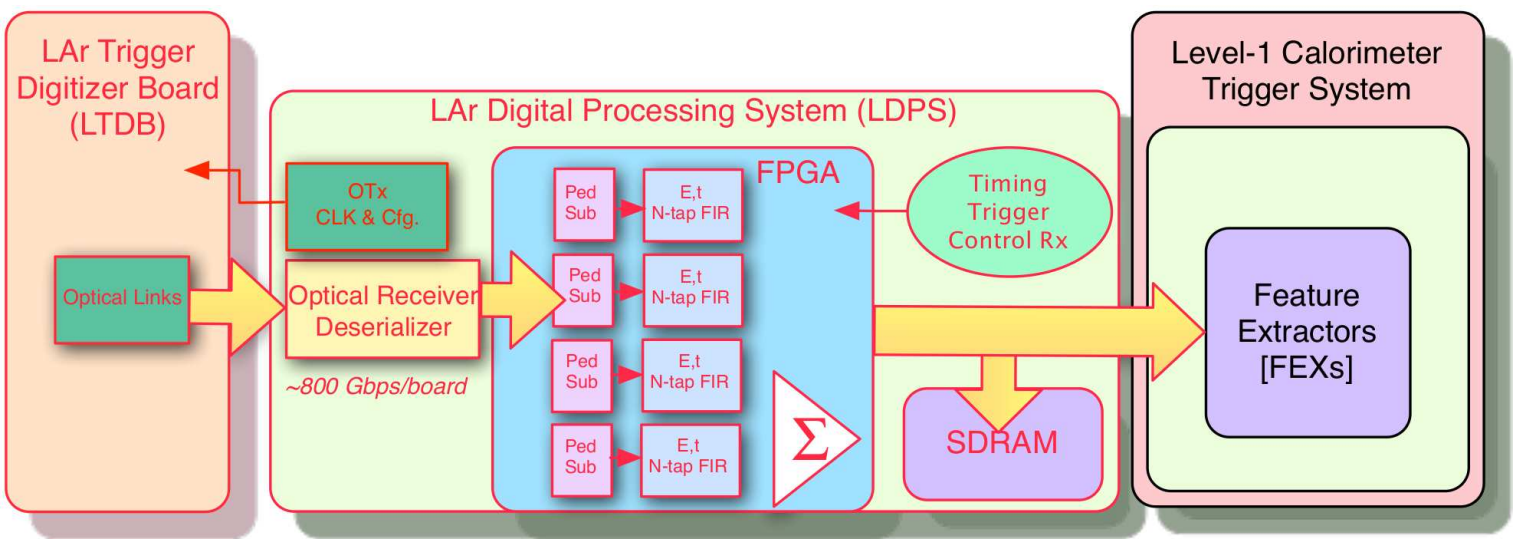
- Both ASICs radiation tolerant: few change in output eye diagram after ∼ 200 kRad

LOCx2 after 182 kRad →

- Wafers produced, test on LTDB prototype ongoing

Back-End electronics: LAr Digital Processing System (LDPS)

- Purpose of LAr Digital Processing System (LDPS):
  - receives the 12-bit data from the LTDBs
  - calculates the transverse energy of each super cell and various sums of super cells at fixed latency
  - transmits the results at 40 MHz to the L1Calo trigger boards (various FEX)
  - buffers calculation for readout upon L1 decision (for debug/monitoring)
- main component: LAr Digital Processing Blade (LDPB)
  - ~ 30 LDPBs to read 124 LTDBs:
    - 4 x 48 input fibers @5.12 Gb/s
    - 4 x 48 output fibers @11.2 Gb/s

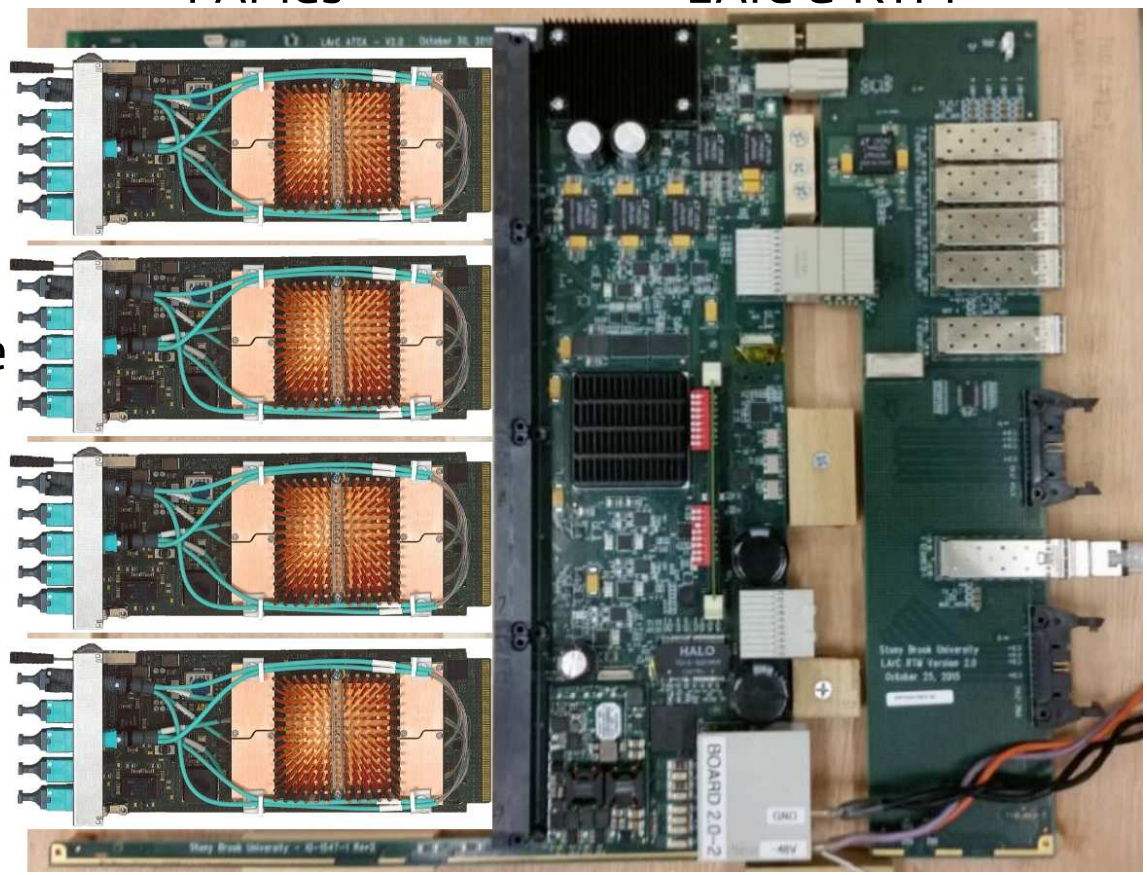


Back-End electronics: Carrier Board LArC

- One carrier board has four Advanced Mezzanine Cards (AMC) and a Rear Transition Module (RTM)

4 AMCs

LArC & RTM



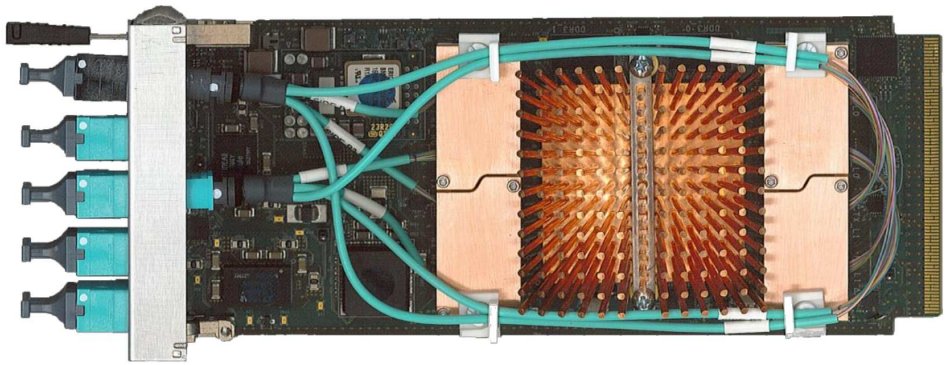
LAr Carrier Board (LArC):

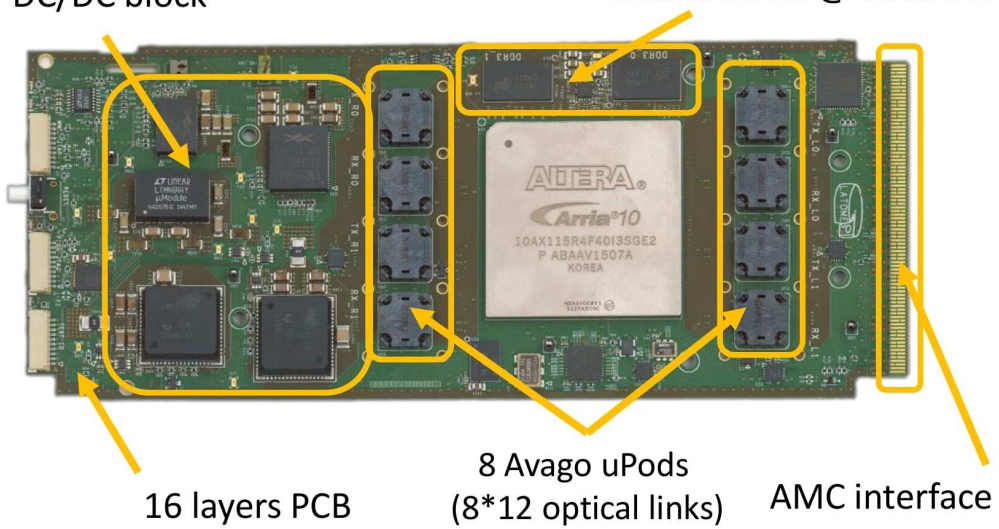
- ATCA custom board
- drives communication to the Felix system and the Data Acquisition (DAQ) for the data monitoring
- Virtex7 (Xilinx) FPGA

Back-End electronics: LATOME Hardware

LAr Trigger prOcessing MEzzanine (AMC):

- Main data flow:
  - receives super cell data from LTDB @5.12 Gbps on up to 48 optical links
  - compute transverse energies (of super cells and sums) using optimal filtering at fixed latency
  - bunch crossing assignment by timing measurement
  - sends data @11.2 Gbps on up to 48 optical links to L1 trigger
- monitors data and sends report to DAQ system upon request
- ARRIA-10 (Intel) FPGA

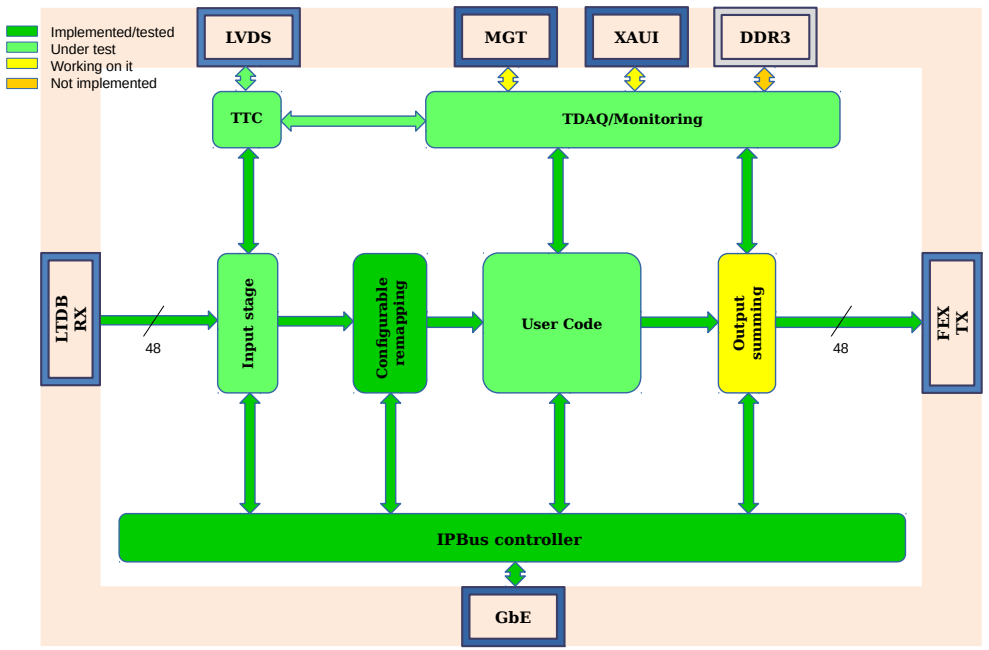




- prototypes have been tested and integrated: validated features include optical links up to 11.2 Gbps, 1 GbE and GBT interfaces
- system test ongoing to check all functionalities and the communication of the LDPB with other systems

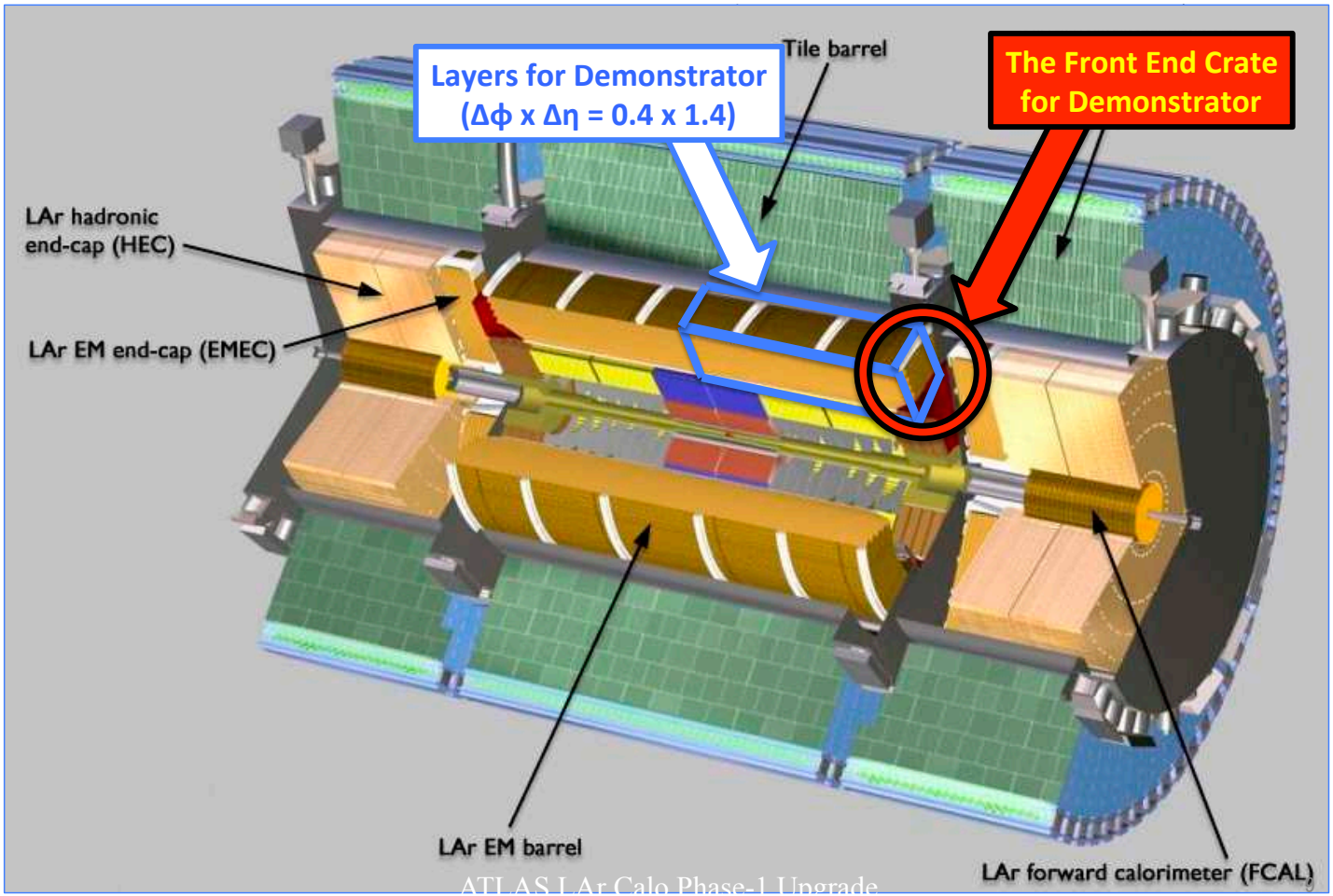
Back-End electronics: LATOME Firmware

- Input stage:
  - receive ADC data (40 MHz)
  - align input fibers to the same time reference (TTC)
- Configurable remapping:
  - remap channels to match detector geometry
- User Code:
  - compute energy at the correct bunch crossing (time)
- Output summing:
  - sum super cell transverse energies for various L1 FEX
  - send data to L1 trigger system (40 MHz)
- latency $<$ 375 ns
- buffer ADC data and energy for at least 2.5 μs
  - allows monitoring at L1 trigger rate (100KHz)



- all LATOME firmware blocks have been developed and are under test
- overall system test on the hardware is ongoing

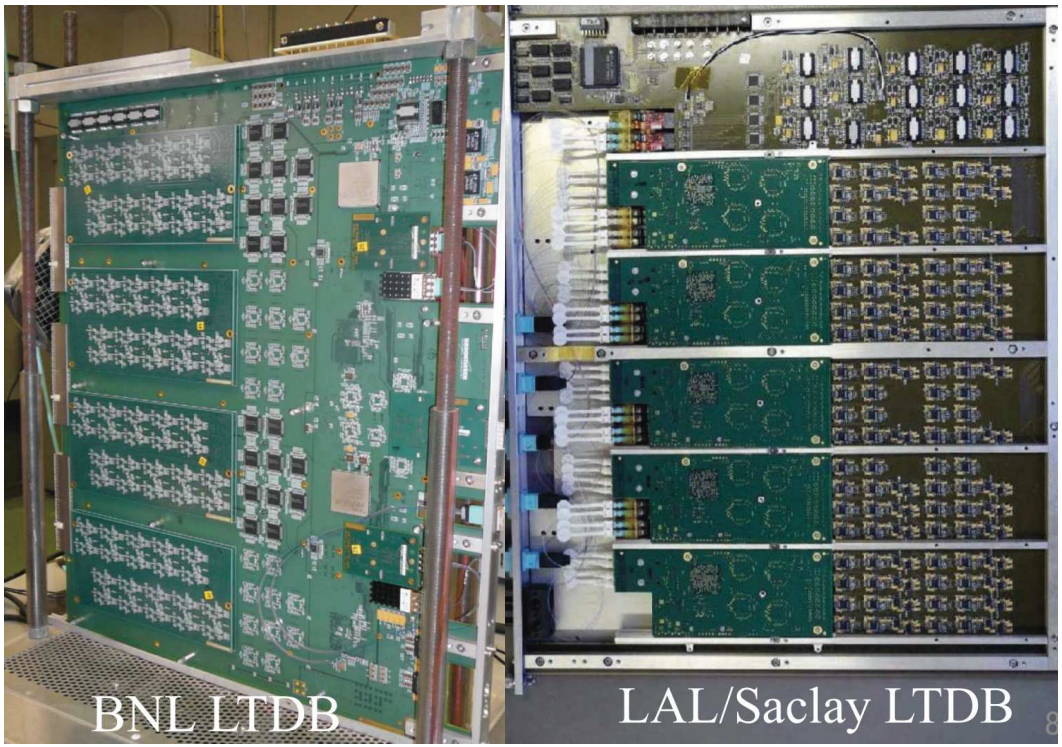
The LAr Demonstrator



- installed in 2014 (LS1), covering 1/32 of barrel region
  - verified no disturbance of current system before installation
  - validates energy reconstruction and bunch crossing identification development
  - calibration and data-taking with proton-proton collisions during Run 2

The LAr Demonstrator: LTDB

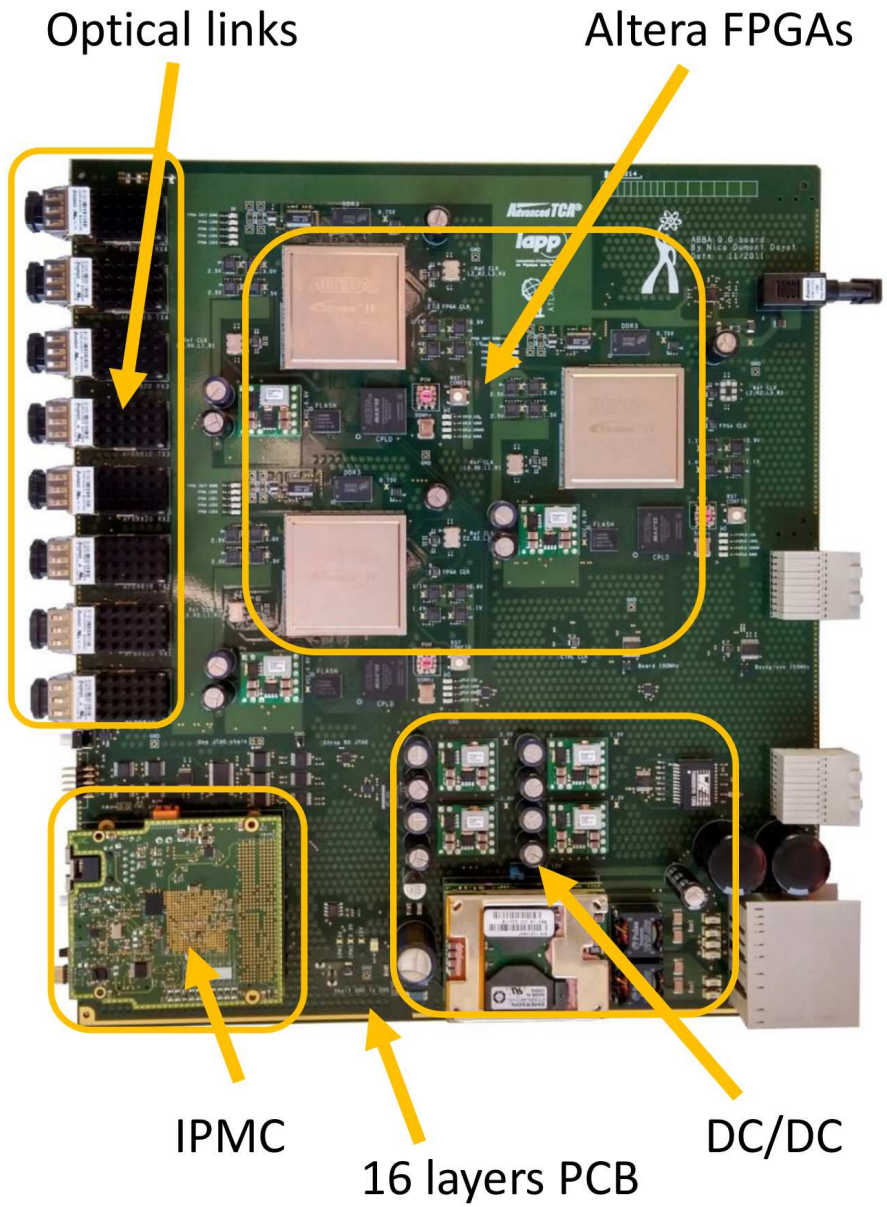
- Handles up to 320 super cell signals (284 super cells in EM Barrel)
- super cell signals digitized with 12 bit ADC @ 40 MHz
  - Commercial 12-bit ADC (TI ADS5272)
  - not radiation-hard
- Multiplexing 8 super cells on one 4.8 Gbps optical link
- 2 prototypes developed by several institutes:
  1. BNL: analog mezzanine, digital main board
  2. LAL/Saclay: digital mezzanine, analog main board



- Status: 2 LTDB versions developed and installed in 08/2014 and successfully operated during Run 2

The LAr Demonstrator: ABBA

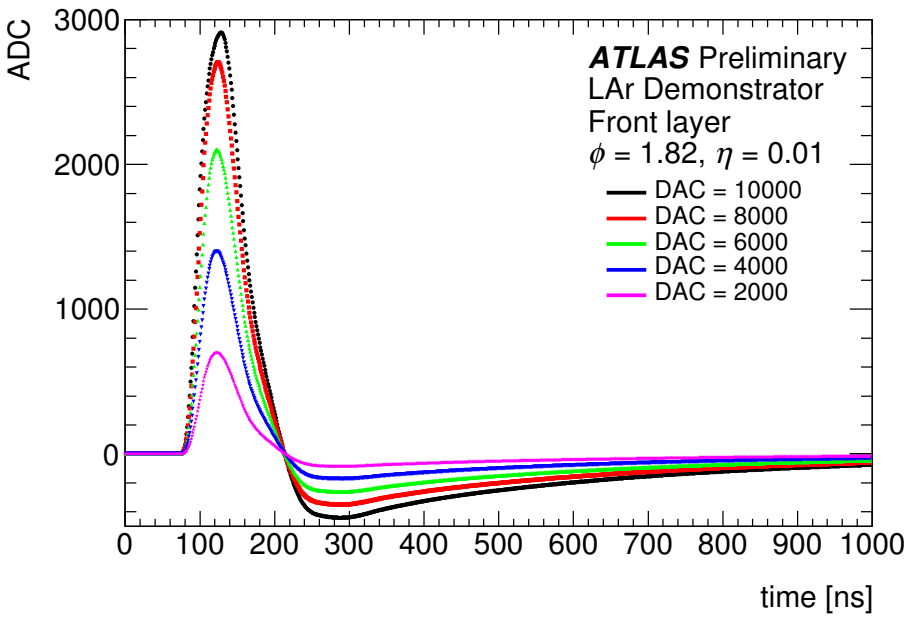
- ATCA board: 3 Stratix IV (Intel) FPGAs
- Receives up to 320 super cell signals from one LTDB
- Up to 48 optical links @ 4.8Gbps
- Stores data in circular buffers
- Waits for level 1 trigger accept to readout ADC super cell data ("monitoring mode")
  - readout using IPbus protocol over UDP on 10 GbE network
- Status:
  - 3 ABBA boards installed in counting room (US15)
  - online software operational
  - readout in parallel with ATLAS default readout since 10/2015
  - integrated in automated ATLAS data taking since 11/2016 (separate data flow)



The LAr Demonstrator: calibration

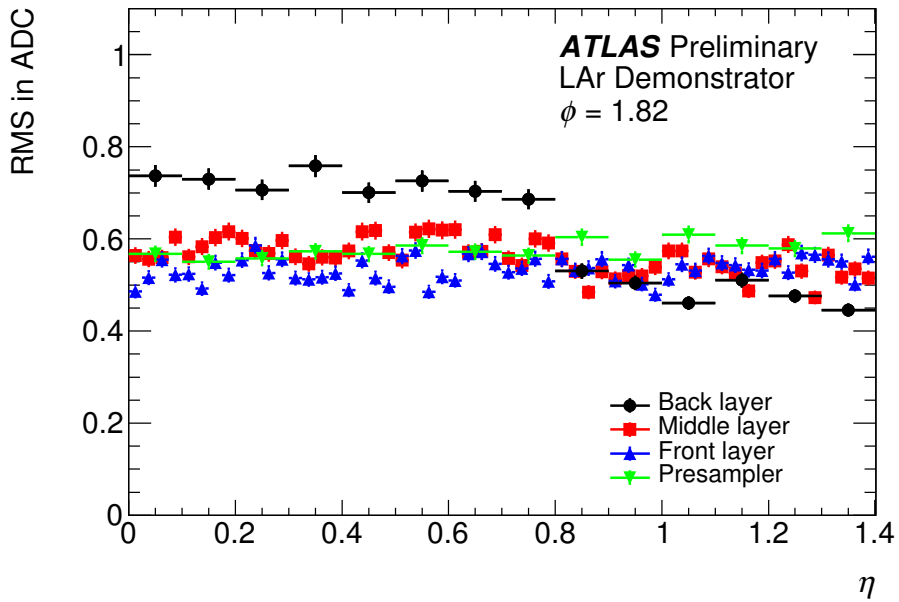
- measure electronic pulses sent by calibration board

Pulse shapes of a front layer super cell



- Good linearity up to DAC 8000, beyond analog saturation

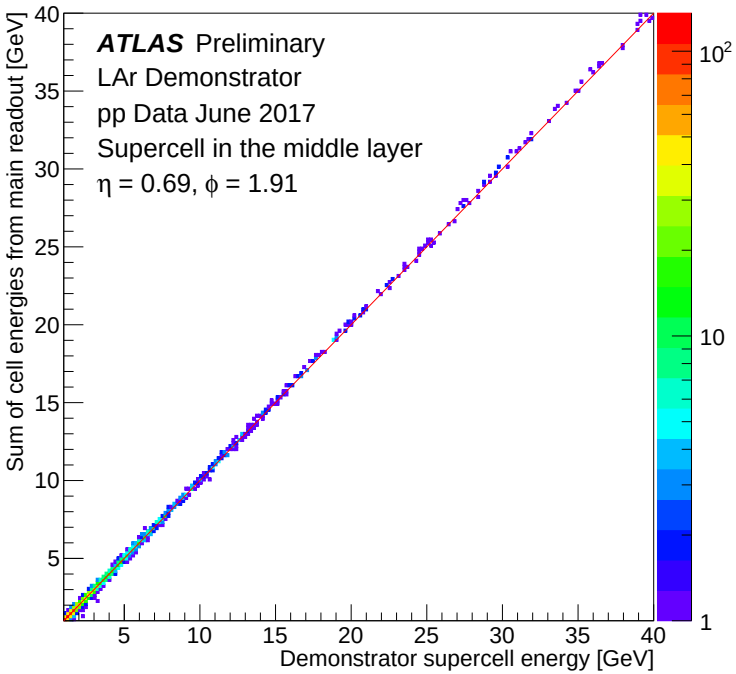
Noise level of super cells in ADC counts

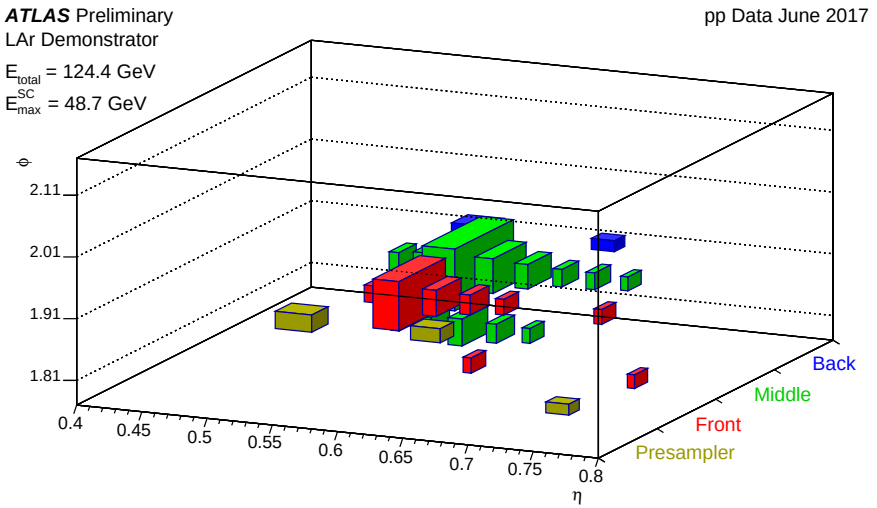


- noise level well below 1 ADC count and consistent with test bench measurements

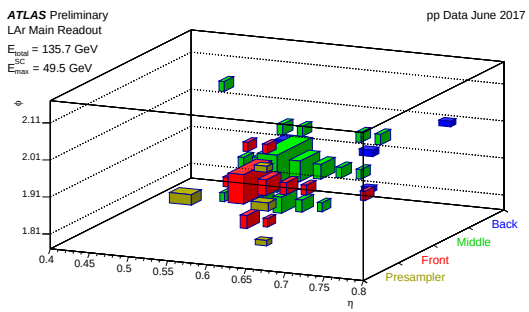
The LAr Demonstrator: data taking in physics collisions

- data taking with proton-proton and heavy-ion collisions since 2015
- collect data triggered in LAr Demonstrator region (L1Topo)
- compare LAr Demonstrator readout and ATLAS main readout





main readout:



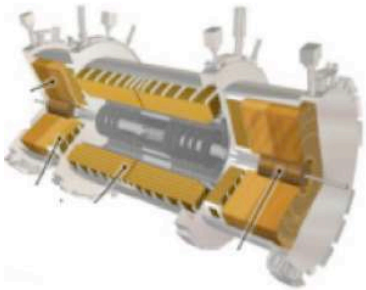
- Good agreement is observed between the two read-outs
- Plan: replace with LTDB and LDPS final prototypes in early 2018.

Summary

- the ATLAS Liquid Argon calorimeter electronics will be upgraded during the long shut-down 2 (2019-2020)
- the trigger path will be digitized at the front-end level with increased granularity
- new LTDB (front-end) and LDPS (back-end) systems have been developed
  - digitization and readout at 40 MHz
  - radiation tolerant ADCs and optical links have been specifically designed
  - Total data output rate to trigger system 40 Tbps
  - production will start in 2018
- a demonstrator system has been installed and successfully run in 2015, 2016 and is currently taking 2017 data
  - valuable data to study filtering algorithm development
  - plan to replace with LTDB and LDPS final prototypes in early 2018
  - test the full pre-production readout chain with real proton-proton collision data in 2018
- the Phase-1 upgrade is a stepping stone towards the full readout upgrade during the long shut-down 3 (Phase-2)

Backup slides

Backup: Architecture of the upgraded trigger electronics



Front End Crate

Front-end Board (FEB)

Readout HLT/DAQ

accept

Central Trigger

Trigger Tower (legacy path)

Tower Builder Board (TBB)

Calo Trigger

Super Cell (new path)

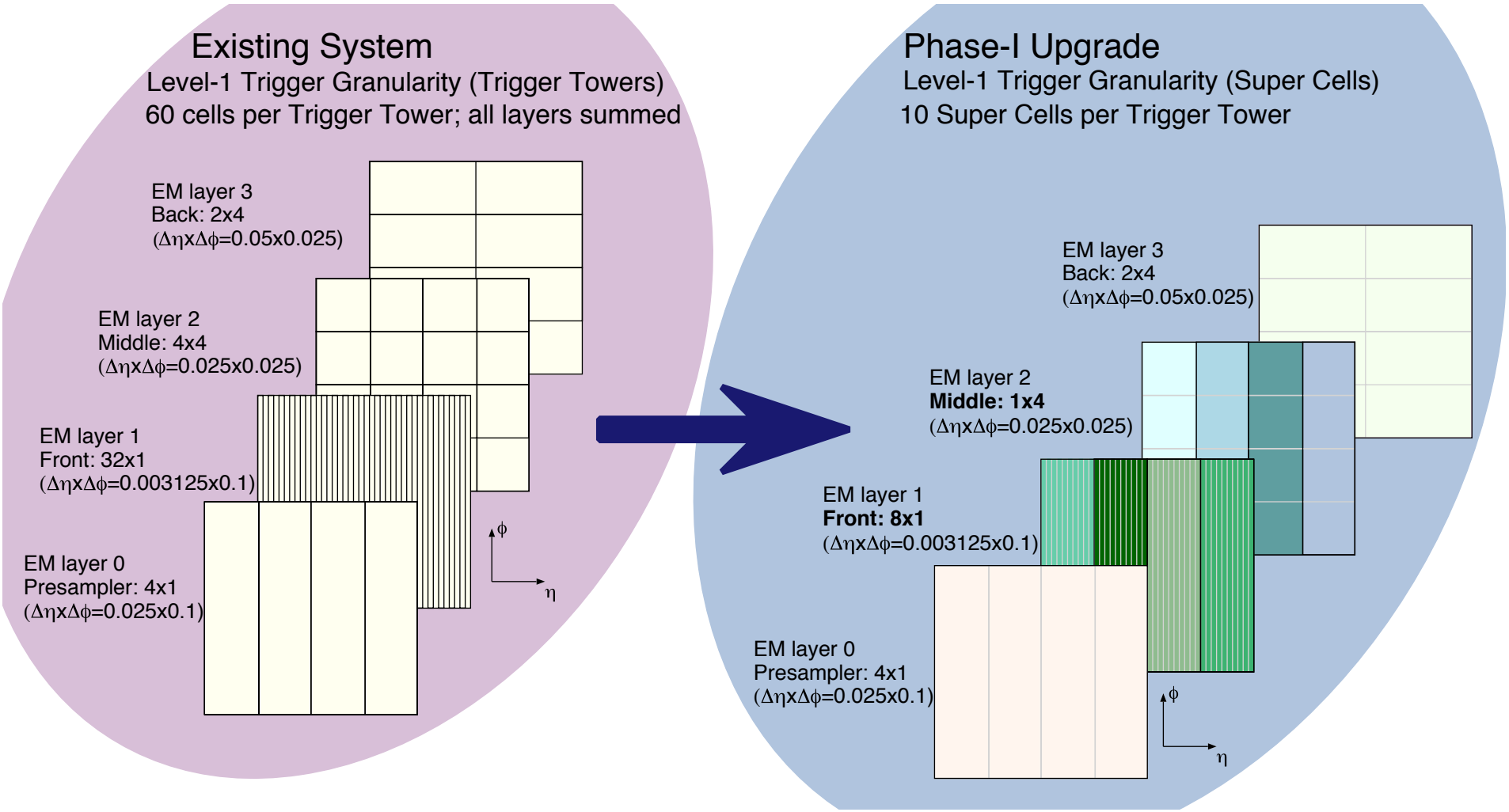
LAr Trigger Digitizer Board (LTDB)

LAr Digital Processing System (LDPS)

FPGA

Trigger Feature Extractor

Backup: Super cells mapping in EM Barrel



Backup: ADC radiation tolerance

Table 1: Measurements of ADC performance before and immediately after irradiation in a 227 MeV proton beam at $f_{in} = 10$ MHz. The change in the ENOB is within the measurement errors of the testing setup.

Chip no.	Dose [MRad]	SNDR [dBc] Pre/Post-Irradiation	SFDR [dBc] Pre/Post-Irradiation	ENOB Pre/Post-Irradiation
1	2	62.43/61.05	67.27/70.06	10.08/9.85
2	1	63.54/62.36	70.92/72.98	10.26/10.10

Total Ionizing Dose

- **1 Mrad is 10 times the dose expected in 4000 fb-1**

Table 2: Measurements of ADC SEE performance in a 227 MeV proton beam.

Single Event Effect

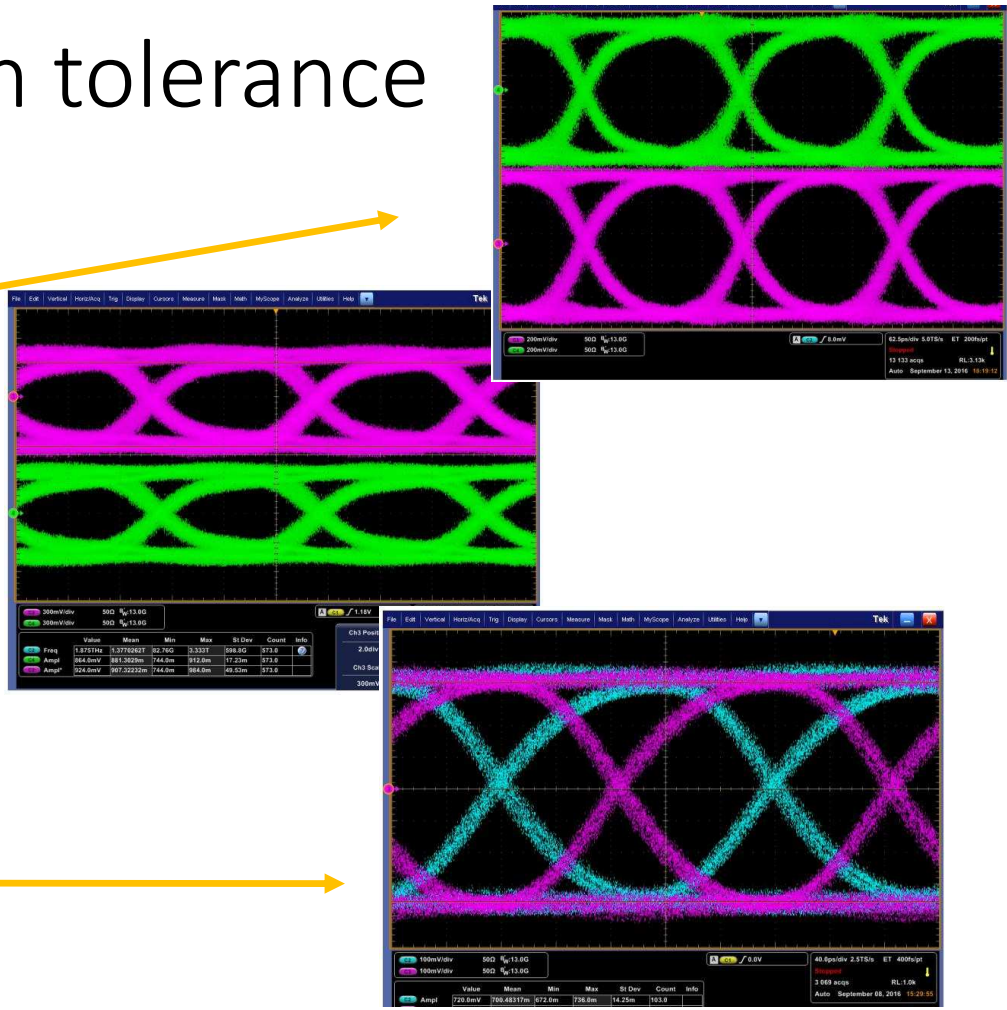
Chip no.	Rate [10^8proton/cm^2/s]	Dose [kRad]	SEFI	SEU (Analog)	SEU (Digital)	SEE	Cross section (w/analog errors) [10^{-12} cm^2]
3	19.0	101	0	8	1	9	0.6 (5.7 ± 1.9)
3	76.0	283	0	41	2	43	0.6 (9.8 ± 1.5)
4	18.6	203	1	10	0	11	0.3 (3.5 ± 1.1)

LOCx2 & LOCId: radiation tolerance

LOCx2

- Eye Diagram 5.12 Gbps
- 2 Channels chip soldered on PCB
- Total jitter ~ 50 ps (loop filter = 800 kHz)

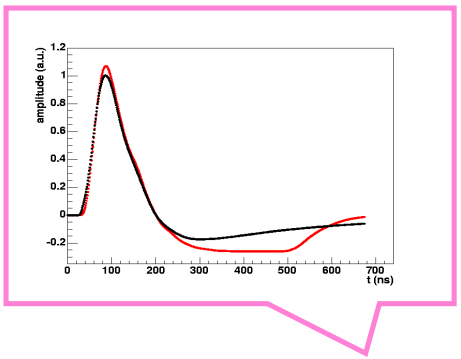
- Eye Diagram after 182 krad TID
- Low or high dose rate (3krad/hr or 30 krad/h)



LOCId

- No eye diagram change after 200 krad
- 2 channels shifted for display clarity
- Current change after irradiation < 10%

Backup: Energy reconstruction in LAr calibration



$$E_{\text{cell}} = F_{\mu\text{A}\to\text{MeV}} \cdot F_{DAC\to\mu\text{A}} \cdot \frac{1}{\frac{M_{\text{phys}}}{M_{\text{cali}}}} \sum_{i=1}^{M_{\text{ramps}}} R_i \left[\sum_{j=1}^{N_{\text{samples}}} a_j \left(s_j - p \right) \right]^i$$

Cell energy

Sampling fraction

Calibration board

ADC to DAC (Ramps)

Pulse Samples

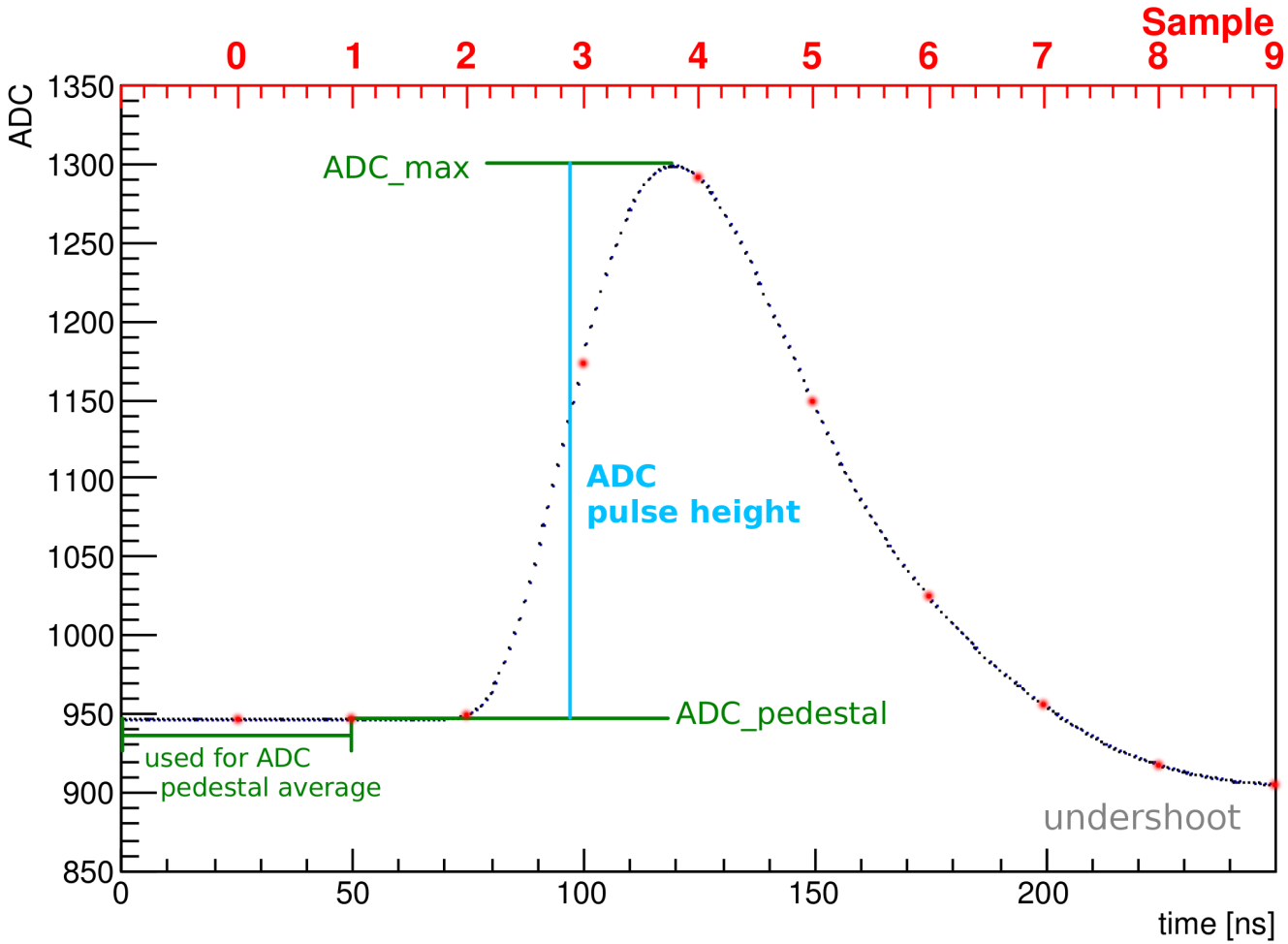
Optimal Filtering Coefficients

Pedestals

The above formula describe the LAr electronic calibration chain (from the signal ADC samples to the raw energy in the cell. Note that this version of the formula uses the general M_{ramps}-order polynomial fit of the ramps. Actually we just use a linear fit (electronic is very linear, and additionally we only want to apply a linear gain in the DSP in order to be able to undo it offline, and apply a more refined calibration). In this case, the formula is simply:

$$E_{\text{cell}} = F_{\mu\text{A}\to\text{MeV}} \cdot F_{DAC\to\mu\text{A}} \cdot \frac{1}{\frac{M_{\text{phys}}}{M_{\text{cali}}}} \cdot R \left[\sum_{j=1}^{N_{\text{samples}}} a_j \left(s_j - p \right) \right]$$

Backup: ADC pulse measurement at the LAr Demonstrator



- measured quantity is ADC, digitized electronic signals
- readout only every 25 ns → red points
- measure points in between by delaying readout by steps of 1 ns

Backup: Phase-2 upgrade