Silicon Tracking System of BM@N

Dementev Dmitrii for CBM-BM@N STS collaboration

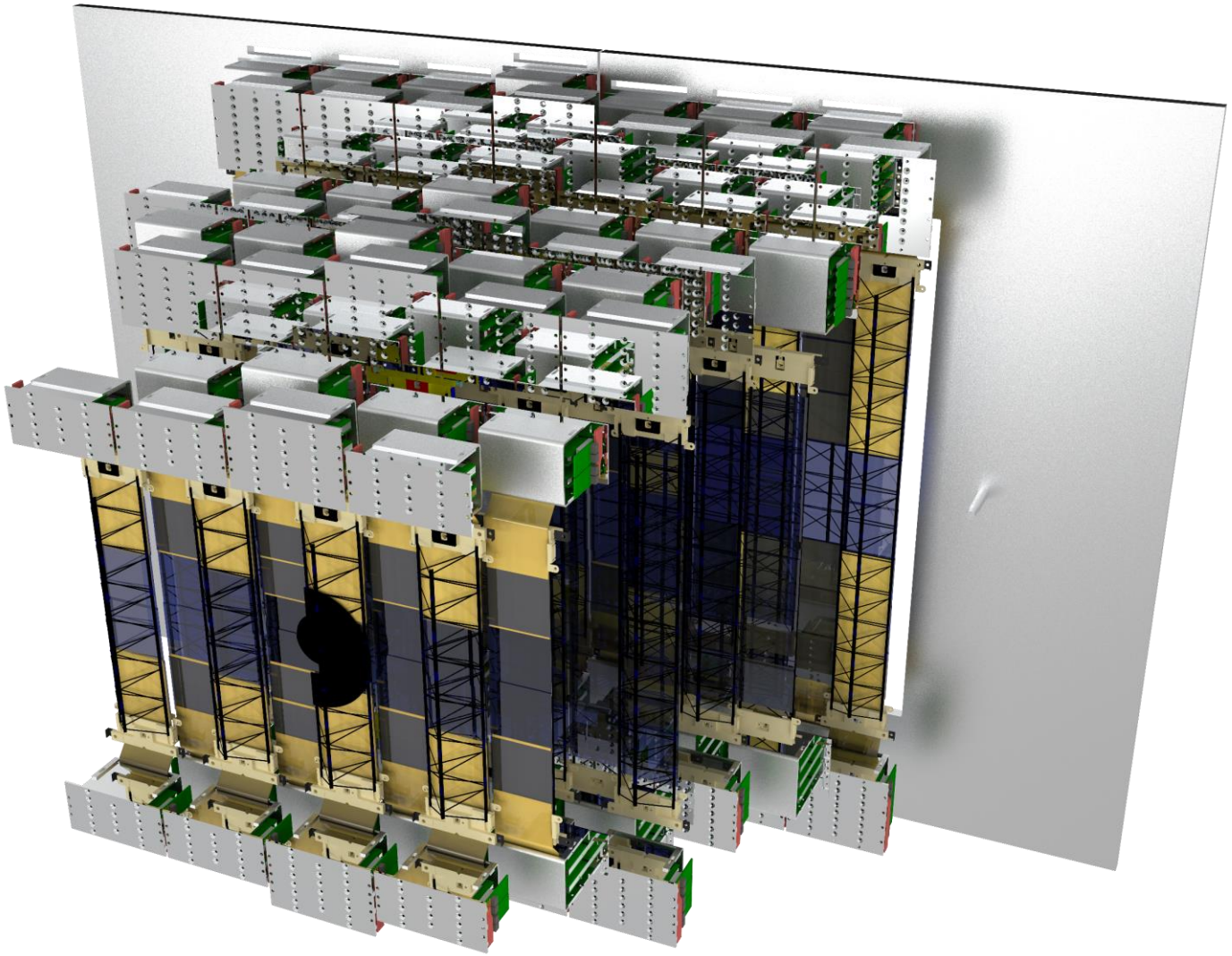
"6th BM@N Collaboration meeting",
26-27 October 2020,
VB LHEP, JINR, Dubna

RUSSIAN FOUNDATION FOR BASIC RESEARCH

CREMLIN PLUS
Connecting Russian and European Measures for Large-scale Research Infrastructures

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 871072

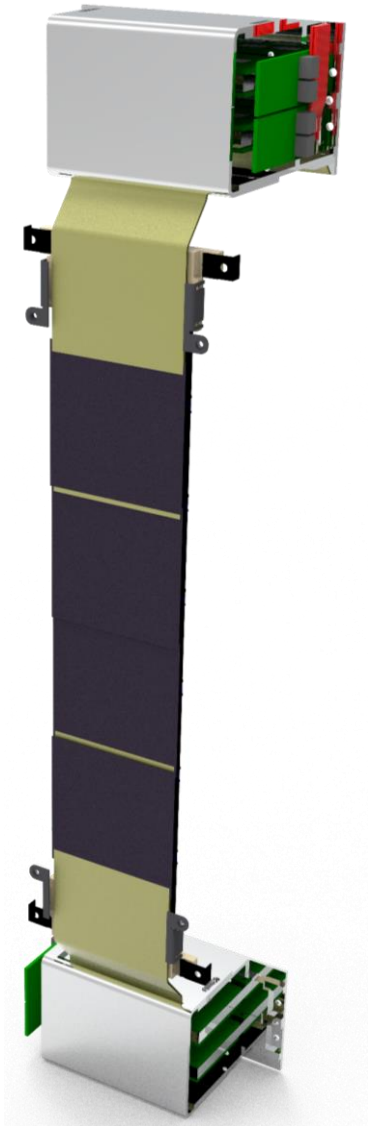
Outline



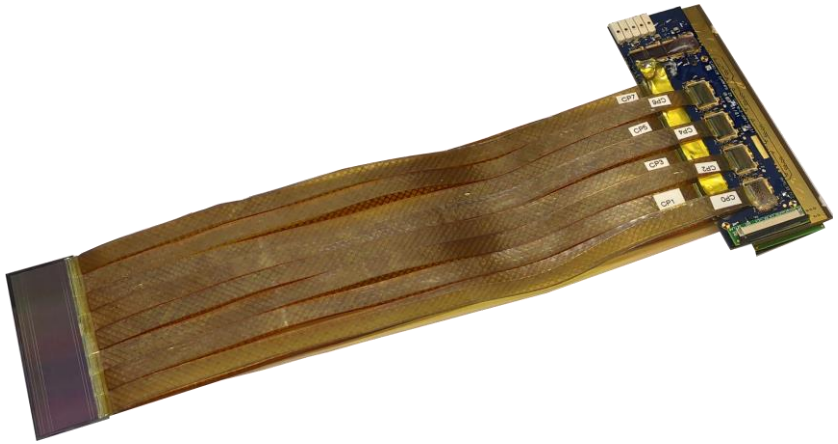
- Module assembly
- Front-end electronics
- Ladder assembly
- Readout electronics
- Mainframe

STS components

4 x STS stations



34 x Ladders



292 x Modules

ELOG for the module assembly

BMN STS

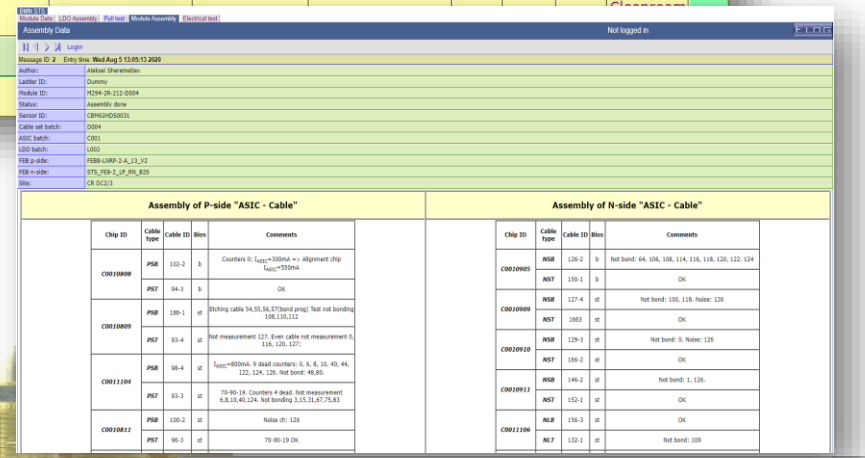
Module Data | LDO Assembly | Pull test | Module Assembly | Electrical test

Pre-production Data, Page 1 of 1 — Not logged in — ELOG

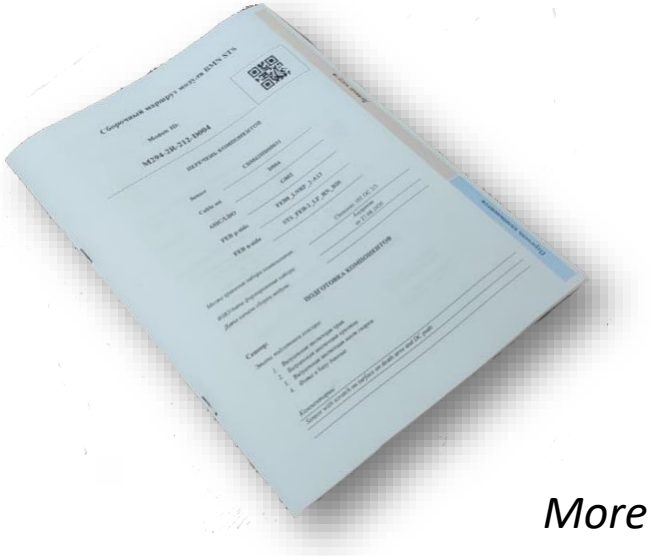
Login

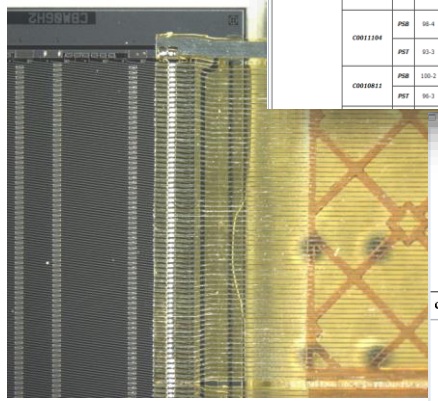
Full | Summary | Threaded — -- Ladder ID -- | -- All entries -- | -- Status -- | 5 Entries

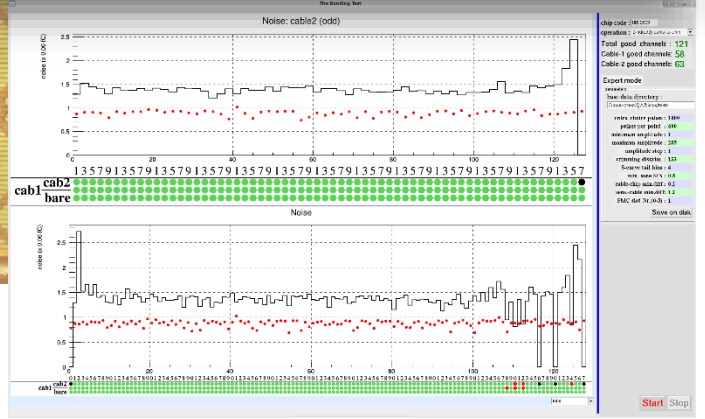
ID	Date	Author	Ladder ID	Module ID	Status	Sensor ID	Sensor ID visually checked	Cable set batch	Cable set batch visually checked	ASIC batch	ASIC batch visually checked	LDO batch	LDO batch visually checked	FEB p-side	FEB p-side visually checked	FEB n-side	FEB n-side visually checked	P-Box	N-Box	E-Box	Site	
1	Thu Jun 18 10:19:20 2020	Aleksei Sheremetiev	Dummy	M294-2R-212-D003	Assembly done	CBM62HDS0030	Yes	D003	Yes	G001	Yes	G001	Yes	FEB8-LNRP-2-A_8_V2	Yes	STS_FE8-2_LP_RN_B28	Yes				Cleanroom DC2/3	52x
2	Wed Jul 29 13:54:07 2020	Aleksei Sheremetiev	Dummy	M294-2R-212-D004	Assembly done	CBM62HDS0031	Yes	D004	Yes	G002	Yes	G002	Yes	FEB8-LNRP-2-A_13_V2	Yes	STS_FE8-2_LP_RN_B26	Yes	BP002	BN002	BE002	Cleanroom DC2/3	71x
3	Thu Jul 30 14:33:25 2020	Aleksei Sheremetiev	Dummy	M294-2R-212-D005	In the process	CBM62HDS0032	Yes	D005	Yes	G003	Yes		Yes									
4	Tue Aug 11 14:37:28 2020	Aleksei Sheremetiev	Dummy	M294-2R-212-D006	Not ready	CBM62HDS0033	No	D006	No	G004	No		No									
5	Tue Aug 18 15:17:58 2020	Aleksei Sheremetiev	Dummy	M294-2R-212-D007	Not ready	CBM62HDS0033	No	D006	No	G004	No		No									



ELOG integration,
disk space,
and maintenance
are provided by
LIT JINR group
(A.Kondratyev, A. Bondyakov)

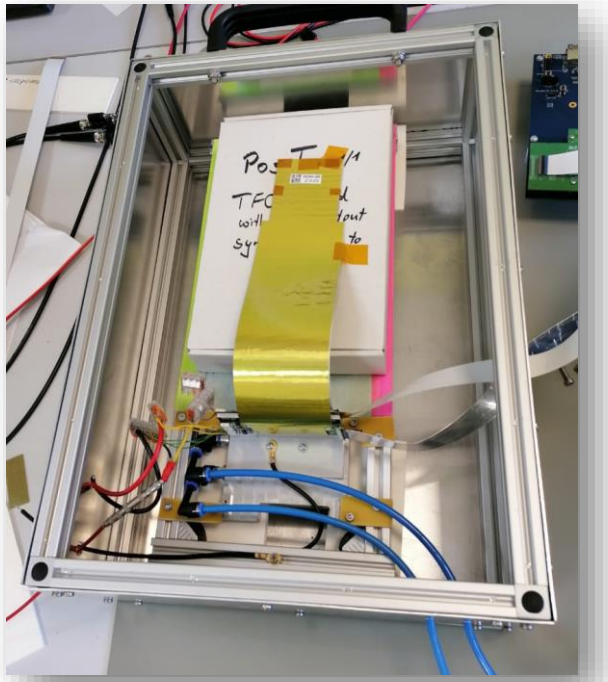






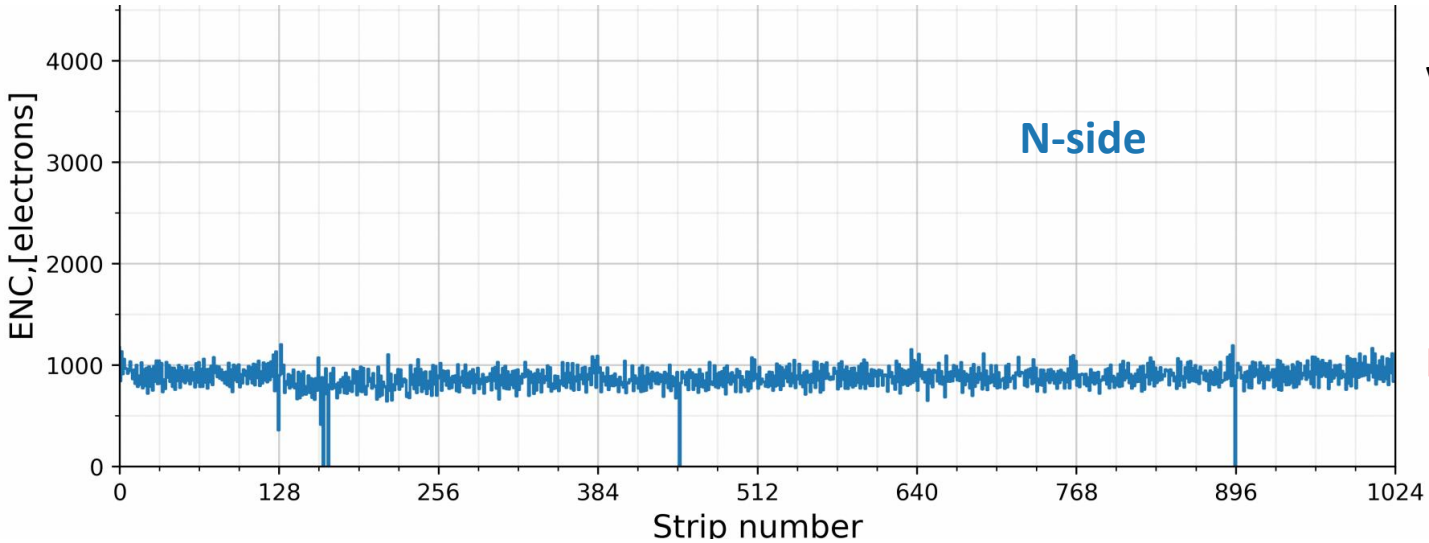
More details about module assembly are presented in the talk by A. Sheremetev

Assembled modules



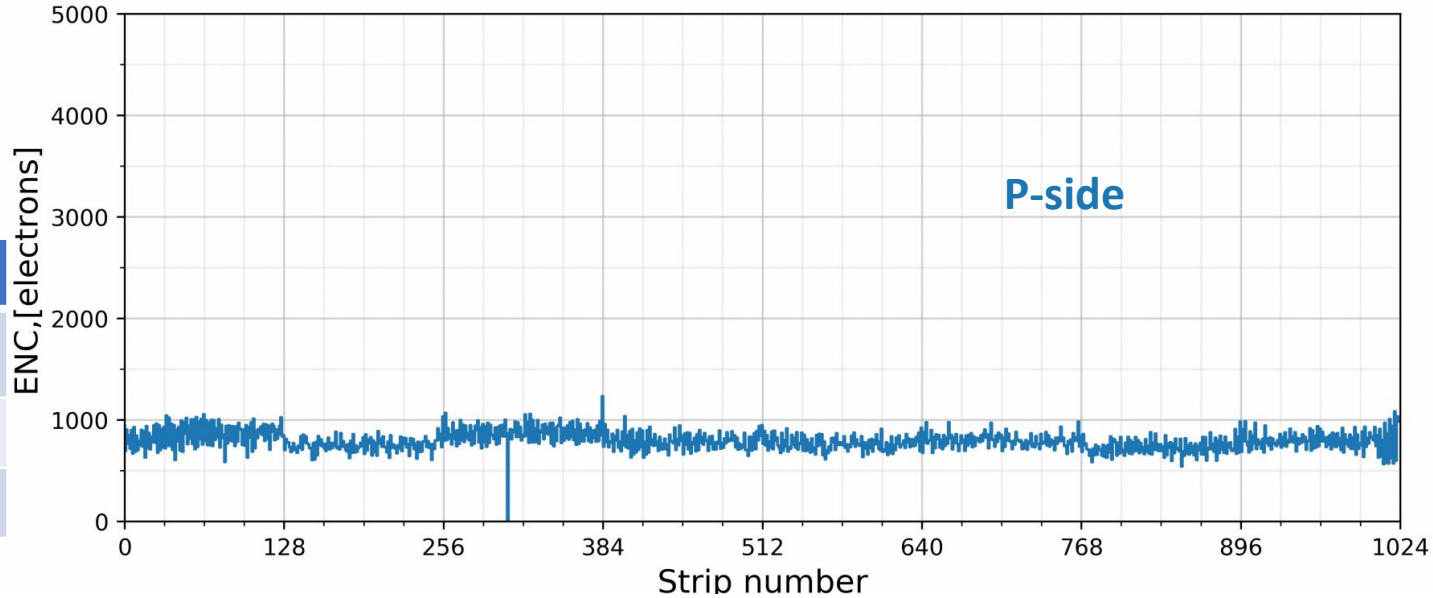
% of not-operable channels per side :

Module	N-side	P-side
M294-6R-212-D001	40 (4%)	23 (2,3%)
M294-2R-212-D003	5 (0.5%)	10 (1%)
M294-2R-212-D004	7 (0.7%)	11 (1.1%)



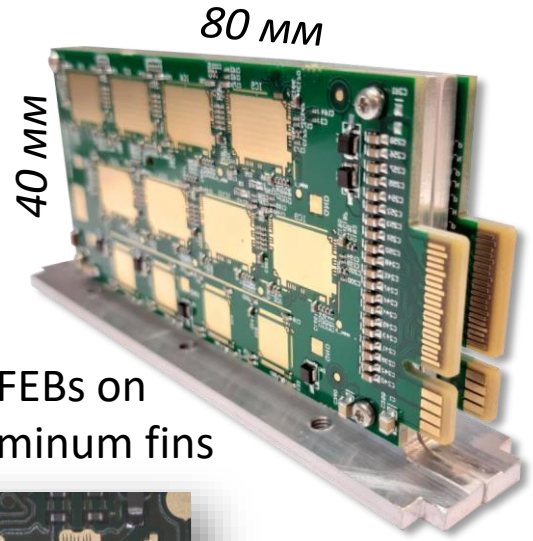
V_{bias} = 100V;

Mean: 880 e⁻



Mean: 795 e⁻

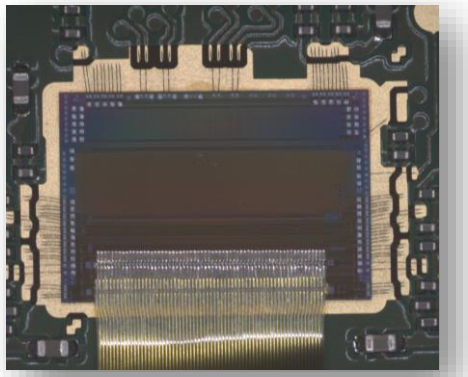
BM@N FEB v. 2.1



2* FEBs on aluminum fins

One FEB provides the following interfaces:

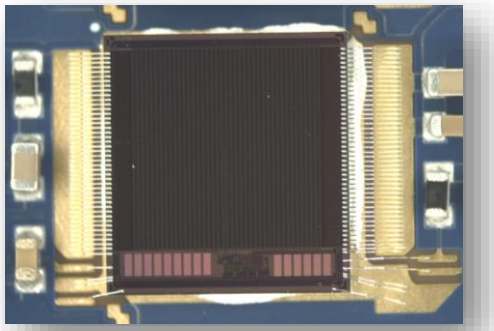
- **1x Down link – 40 Mb/s**
- **1x Clock - 40 MHz**
- **8x Up links – 80 Mb/s**



8x STS-XYTER ASICs

Self-triggered readout provides digitized hits:

- 5 bit pulse height
- 14 bit timestamp
- Hit frame: 30 bits

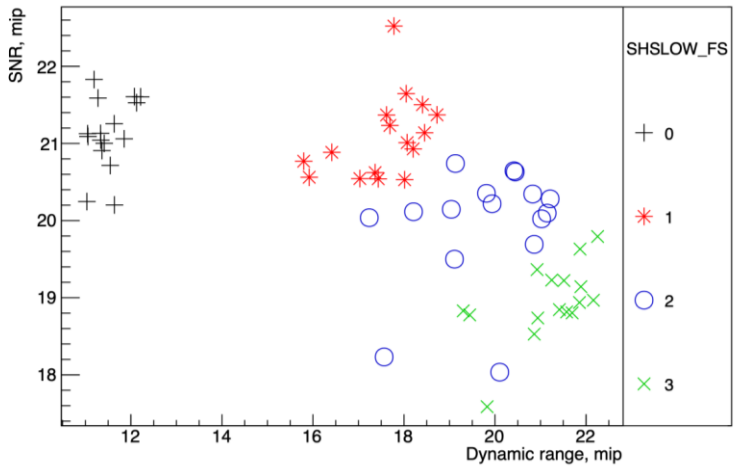


4x skimming LDOs

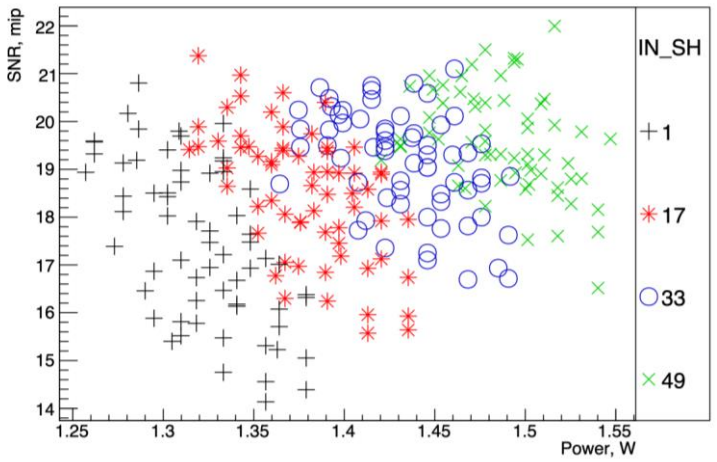
- up to 2.5 A at 1.2 V for the analog part
- up to 2.3 A at 1.8 V for the digital part

Signal is transmitted via AC –coupled LVDS links
~ 10 m electrical connection to GBTxEMU

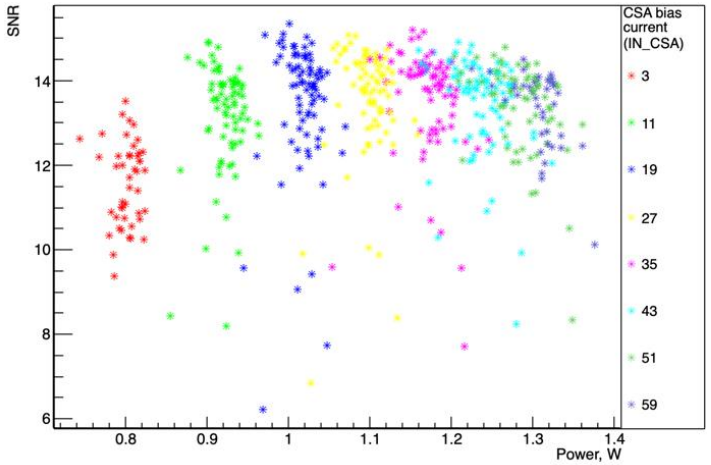
Certification of the STS-XYTER ASICs



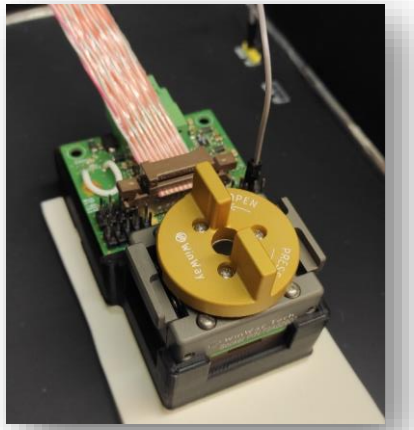
Signal to noise ratio and dynamic range dependence on the slow shaper shaping time



Signal to noise ratio and power consumption dependence on the fast shaper bias current register value



Signal to noise ratio and power consumption dependence on the CSA bias current register value

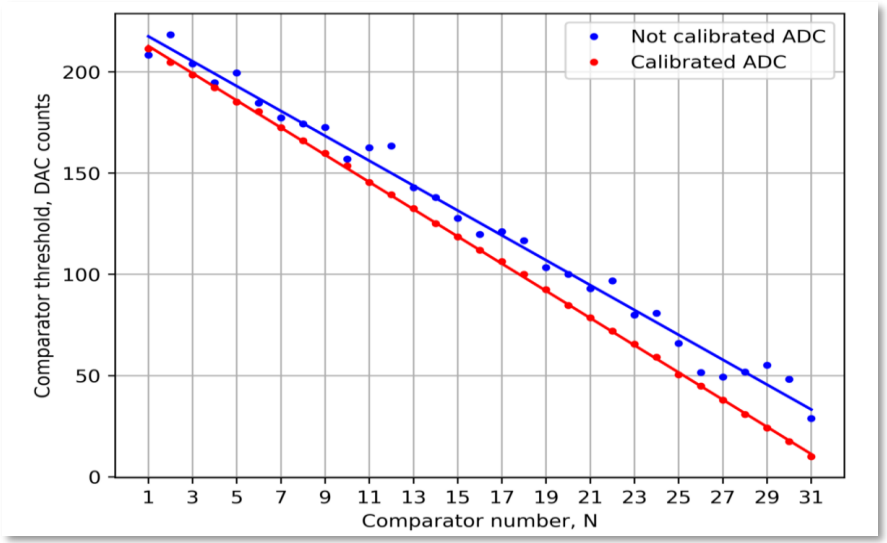


Pogo-pin test circuit

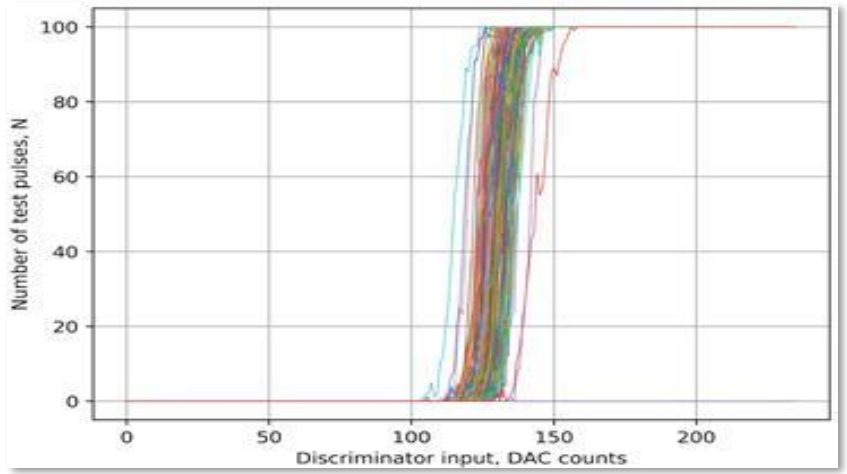
STS-XYTER has a number of variable settings for both analogue and digital parts. To optimize these settings, one needs to measure key characteristics of the ASIC in every point of multidimensional phase space of its parameters and to choose an optimal operation point

Tests of analogue part: A.G. Voronin et.al

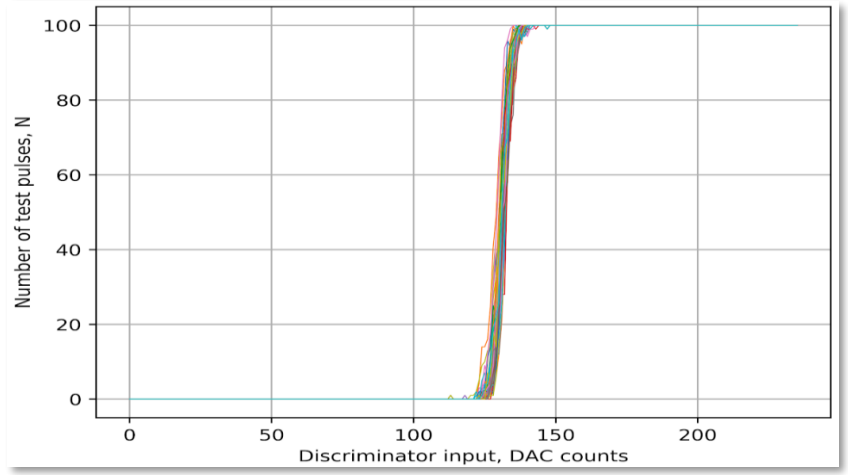
Calibration of the ADC



Inverse transfer function of the ADC



Thresholds of the ADC comparators before calibration

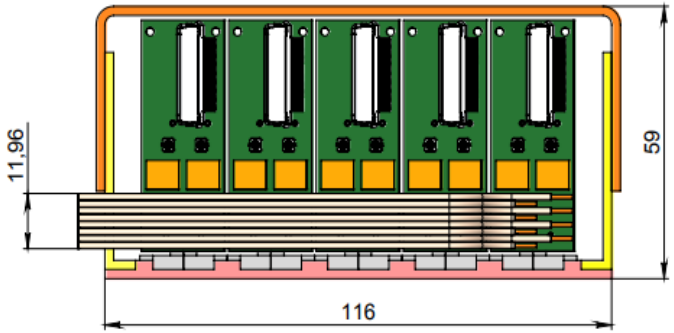


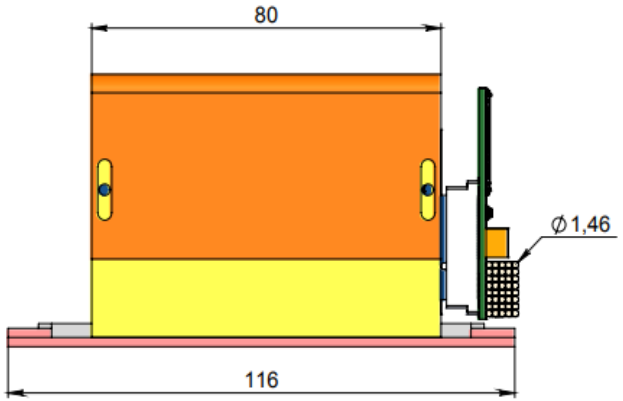
Thresholds of the ADC comparators after calibration

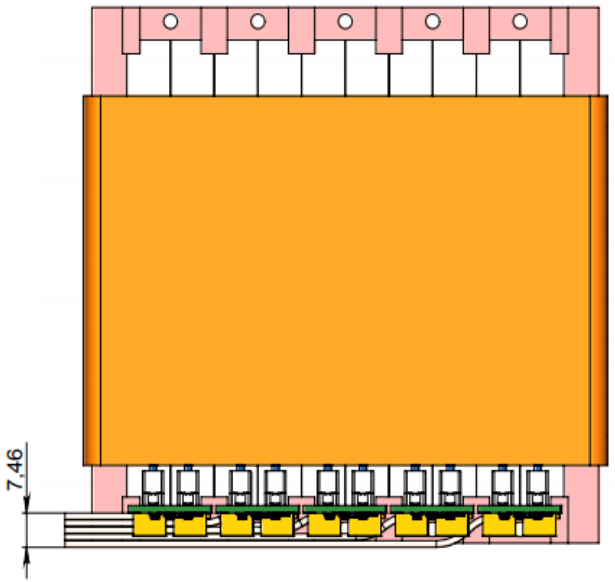
Calibration of the ADC and fast discriminator of each channel of the ASIC are performed before the assembly of the module

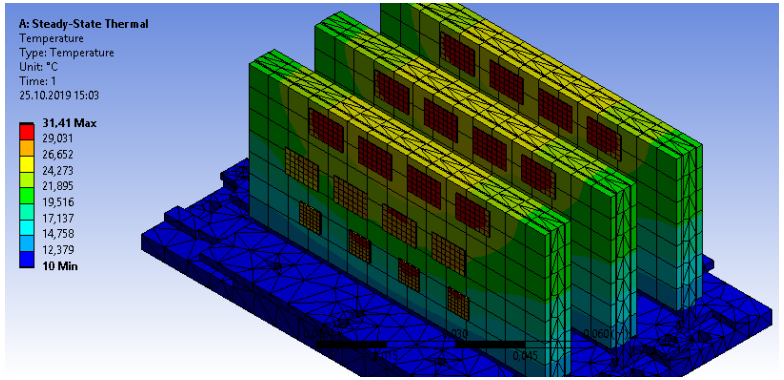
By M. Shitenkow

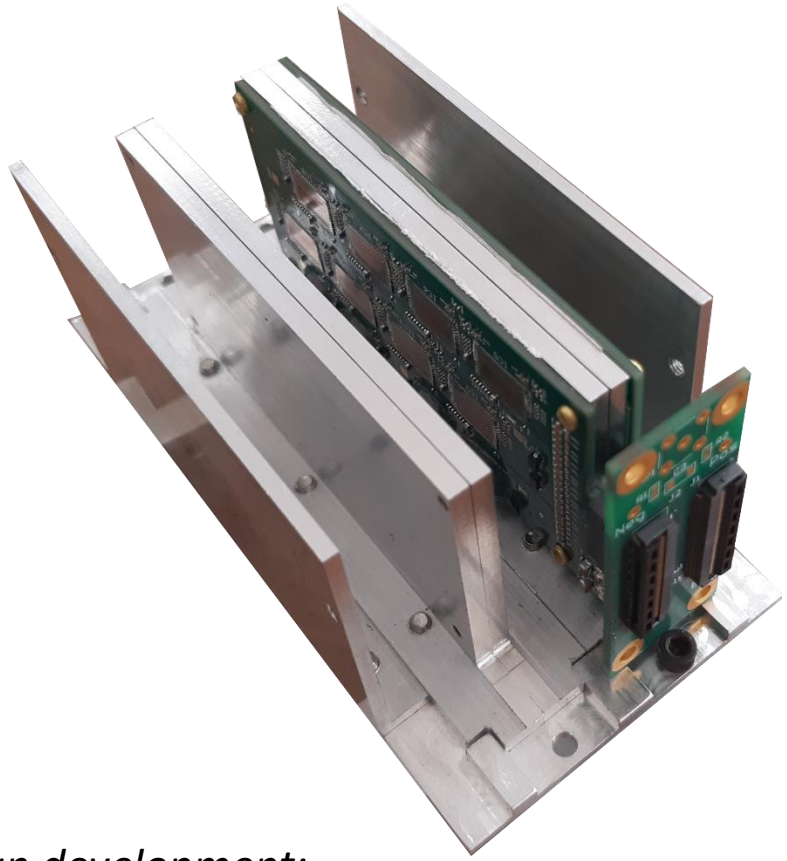
FEB-box





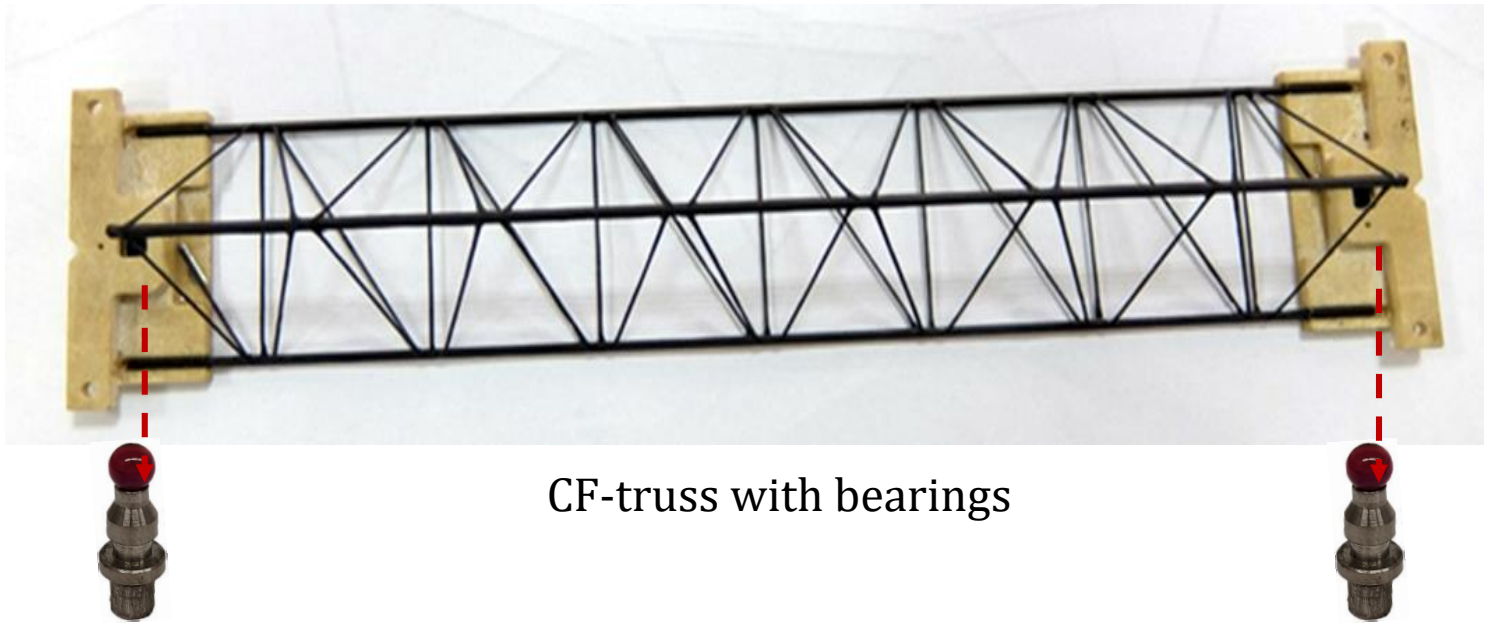




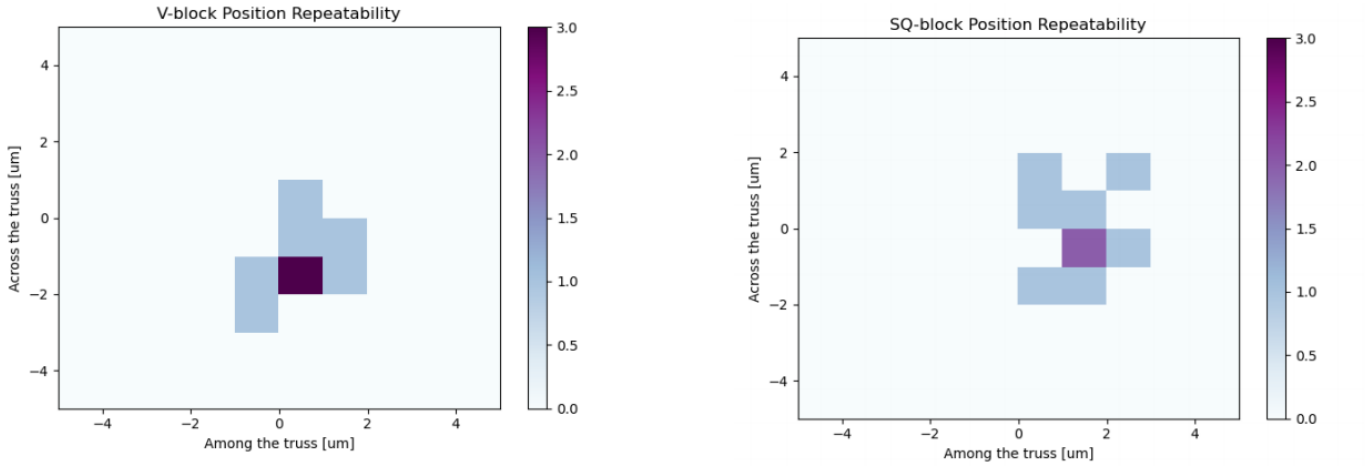


A. Baranov (SINP MSU) - design development;
T. Lygdenova (LHEP) – thermal simulations and tests.

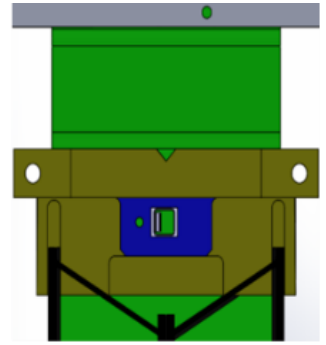
CF frame and bearings



CF-truss with bearings

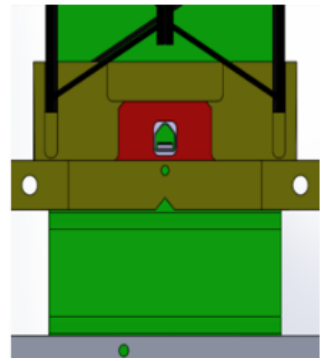


CF-truss position repeatability test



SQ - block for upper side

V - block for lower side



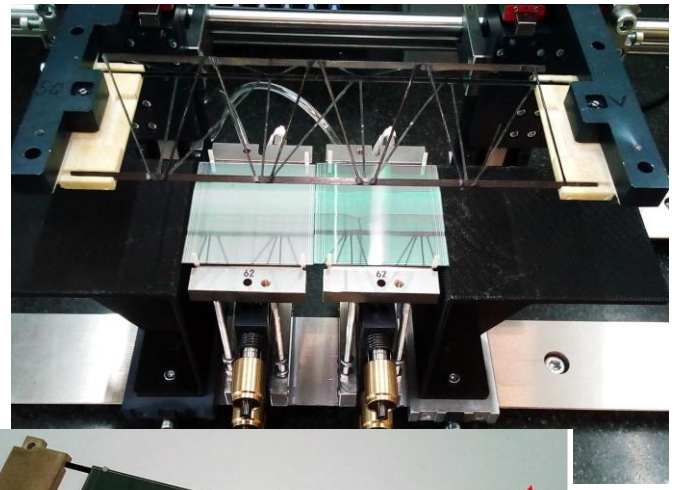
Bearings for the precise positioning of the ladder on ruby-balls pins

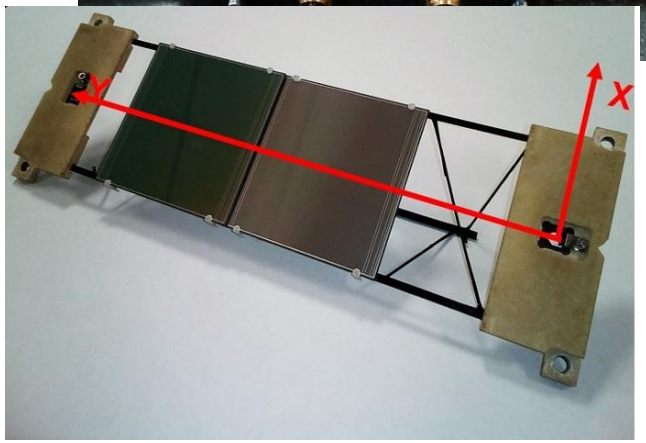
Developed by Van den Brink A.

Ladder assembly

Milestones:

- Mockup of the ladder of 1st BM@N STS station – Dec 2020
- 4 Modules + spare operational and tested for the assembly of 1 STS ladder – Jan 2021
- Operational ladder for the 1st BM@N STS station assembled and tested – Feb 2021





Task	Taskforce
Upgrade of jigs for LAD:	V. Elsha, Planar Ltd
Software developments for LAD:	M. Korolev (SINP MSU), Planar Ltd
Cable-clamp development:	V. Elsha
Development of the ladder-carrying jig:	V. Elsha
Development of the ladder test box	V. Baranov, M. Merkin (SINP MSU)

Delays caused by pandemic control measures in RF:

2.5 month pause in the assembly cite;

Metrology of assembled ladders

Coordinate-Measuring Machine

Features:

- Measuring area (XYZ): 905 x 2005 x 605 mm
- Equipped with a contact and optical sensor;
- Accuracy ~ 1.8 um;

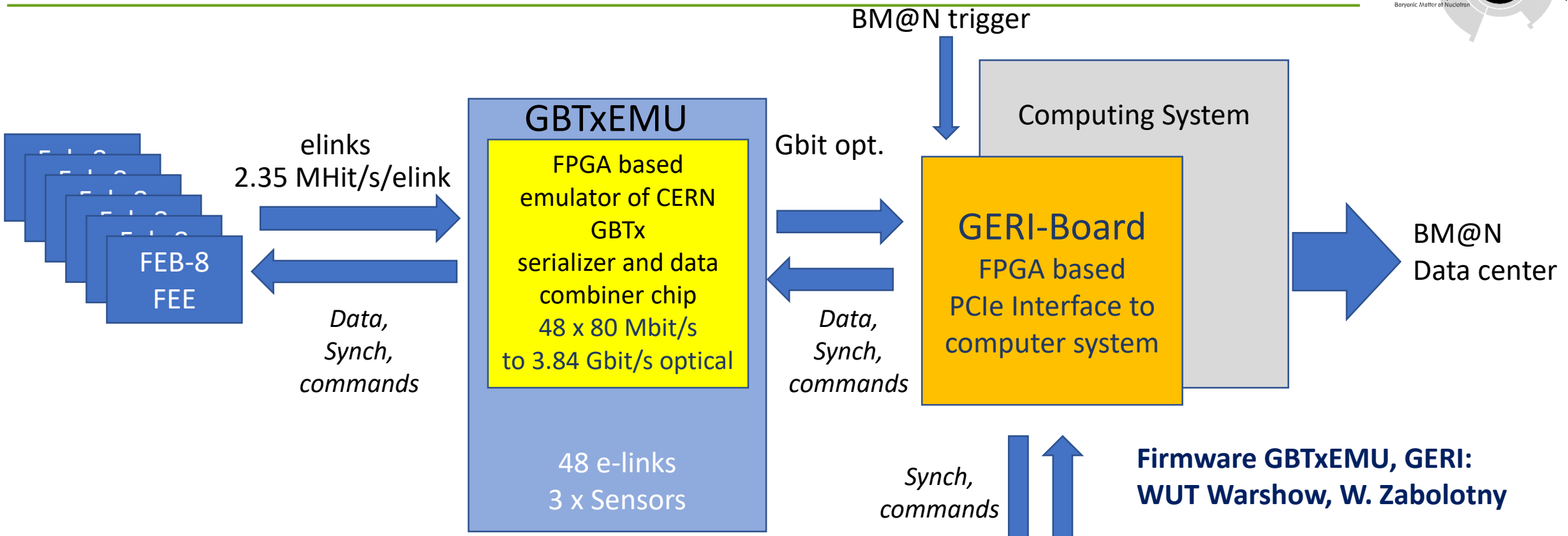
Current status:

- Delivered to JINR;
- Installation is postponed till 2021 due to absence of available space

Personnel:

- One vacant CREMLIN Plus position for the metrology

Readout electronics of BM@N STS



Firmware GBTxEMU, GERI:
WUT Warshow, W. Zabolotny

Firmware TFC:
KIT Karlsruhe, Vladimir Sidorenko

Hardware developments: GSI Detector Lab, JINR, MSU

TFC
Timing and Fast
Control

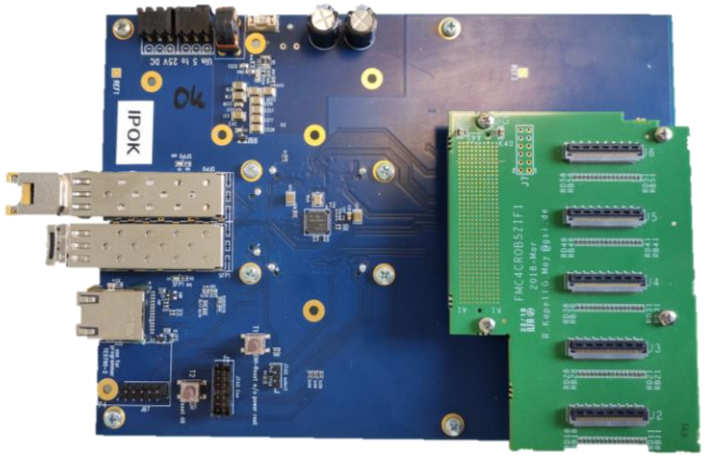
GBTxEMU h/w platform

Features:

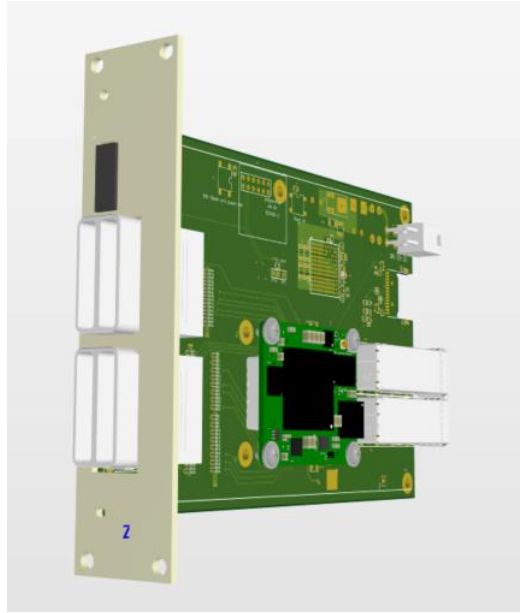
- 3U crate format;
- 12 layers PCB design;
- HDI6 connectors instead of mezzanine card;
- Minimal of s/w modifications are needed according to the prev. h/w platform
- The platform has the ability to upgrade and increase the clock to 80 MHz

Status:

- PCBs are already produced,
- Waiting for the components to be installed
- First operational boards on the table – Dec 2020.



Prototype of the GBTxEMU board



A new GBTxEMU board

New H/w design: JINR

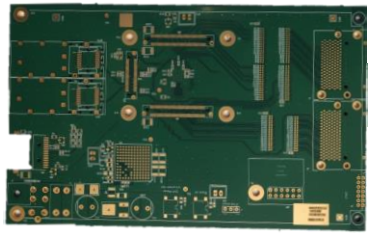
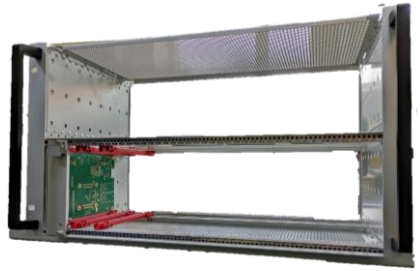
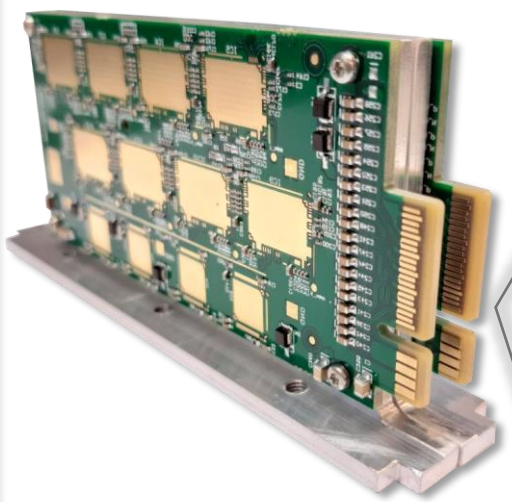


Photo of the PCB



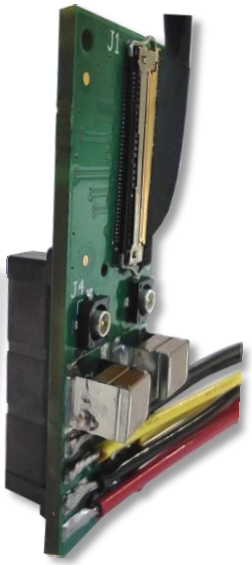
GBTxEMU crate

Connectivity between FEBs and GBTxEMU



Front-end boards

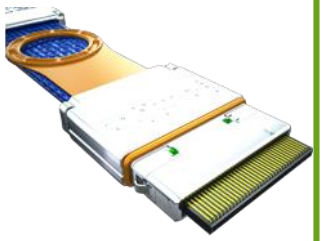
STS-box



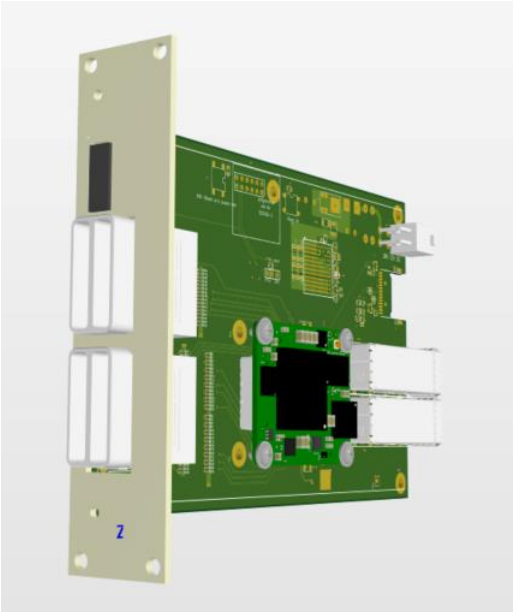
FEB-panel

Micro coax. cable
~0.7 m long

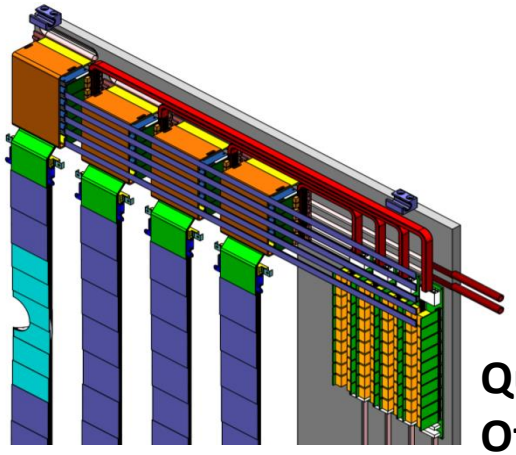
Cross-Panel



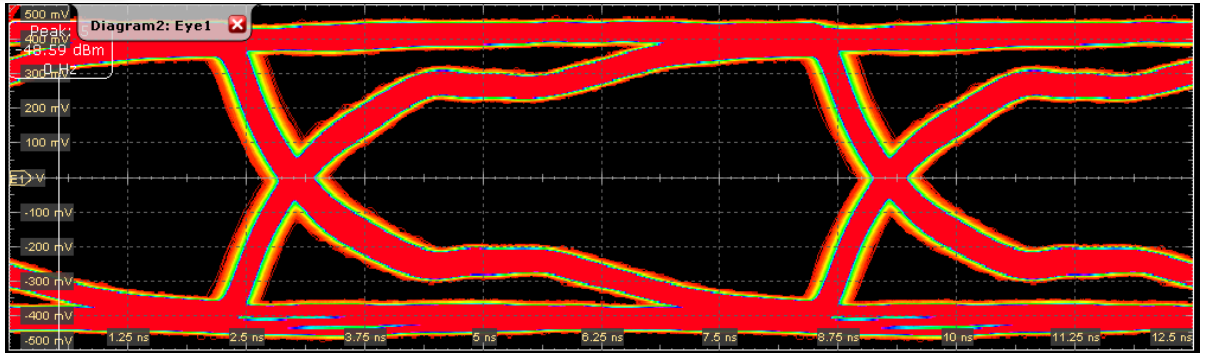
Twinax cable
~10 m long



GBTxEMU

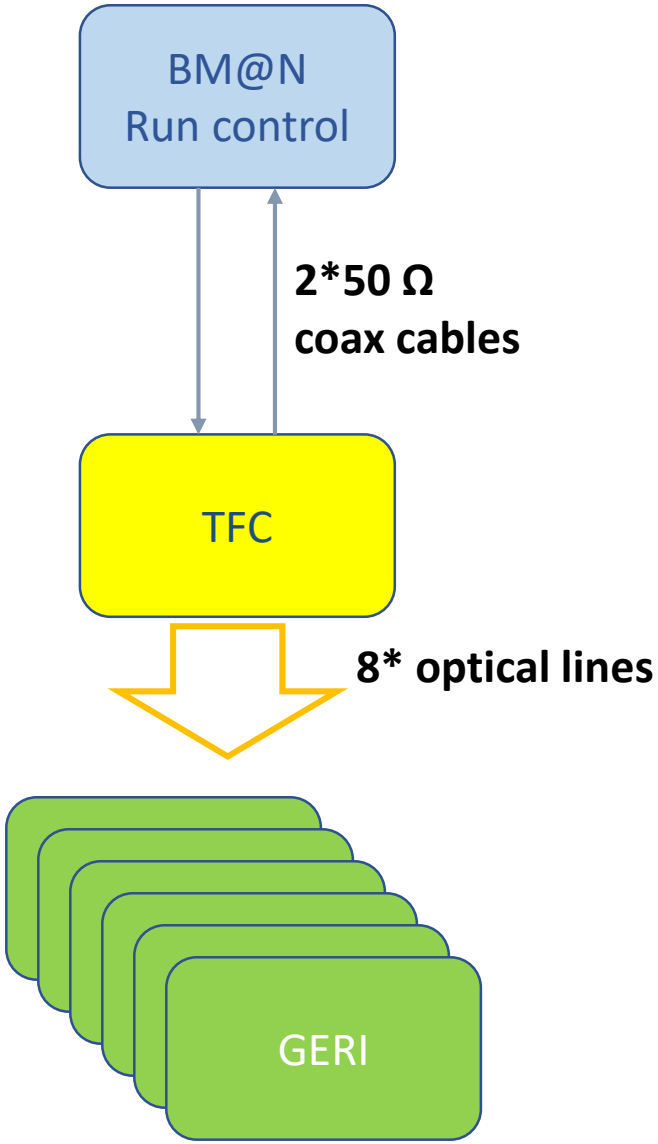


Quarter-station Of BM@N STS



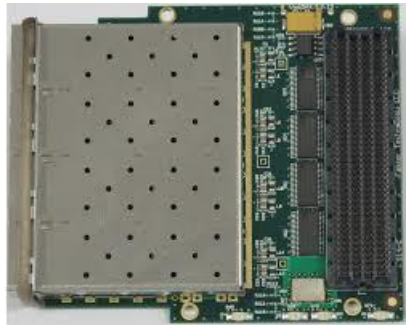
Eye diagram of the Down link signal at 160 MHz Clock

Trigger distribution



- Trigger will be collected by the Timing and Fast Control (TFC) module
- Two SMA connectors for trigger and busy signals
- Trigger signal will be distributed through the GERI boards via optical lines
- Expected trigger latency is ~5 μs

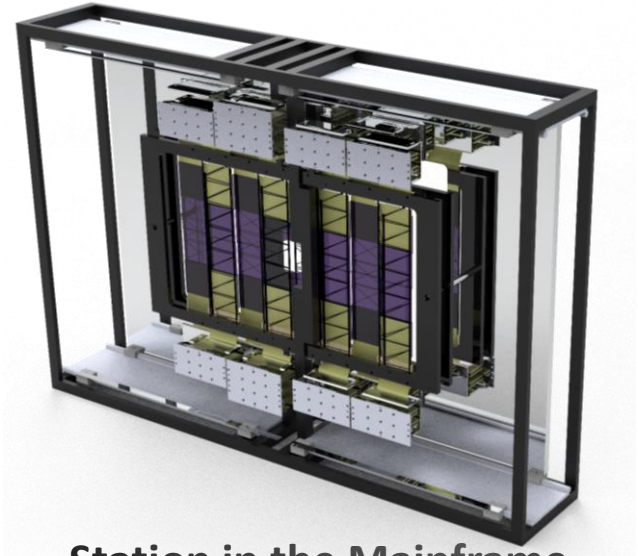
Timing mezzanine (COTS) – FM-S14



Timing and Fast Control (TFC) hardware

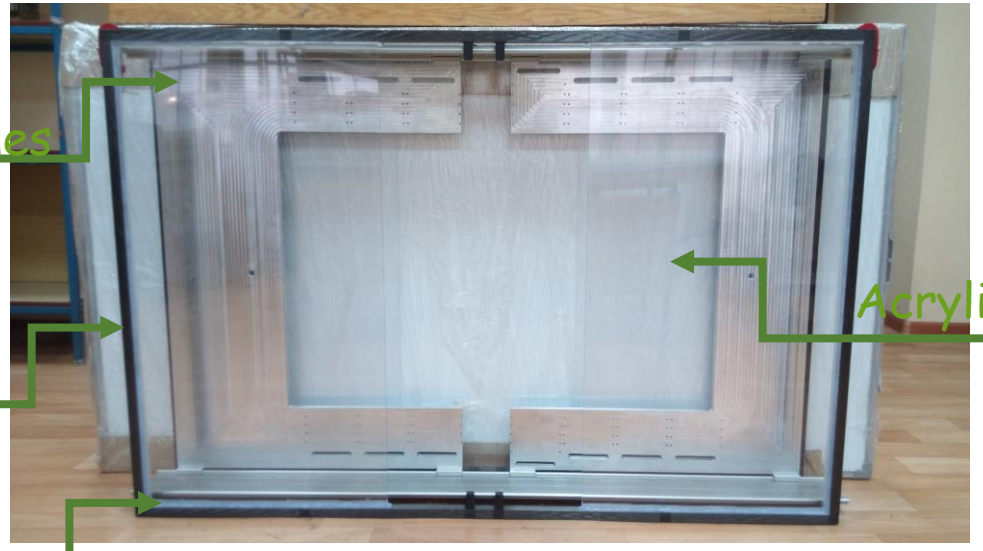
STS Mainframe

Schematic view of the Mainframe



Station in the Mainframe

Master-Jig for the assembly of CF Mainframe



Mainframe prototype with 2*Al. C-frames

Work is carried out by MSU group
More details in the talk by M/Merkin

Delays caused by COVID-19

- Delays in the module & ladder assembly caused by pandemic :
  - 2.5 month delay in the module assembly
  - Delays in the supplying of components
  - Delays in the production of jigs
  - Delays in the maintenance of Delvotec machine
- To speed up the assembly:
  - Ordering of a new Delvotec machine
  - Second shift for the module assembly
- **Risk assessment :**
  - **Module production could be stopped due to a delays in the component supply from Germany**

THANK YOU FOR YOUR ATTENTION!