Beam and Forward Silicon Detectors

upgrade status

Bogdan Topko behalf on Forward Silicon Detectors team

6th Collaboration Meeting of the BM@N Experiment at the NICA Facility,

26 October 2020

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- Forward Silicon Detectors Configuration
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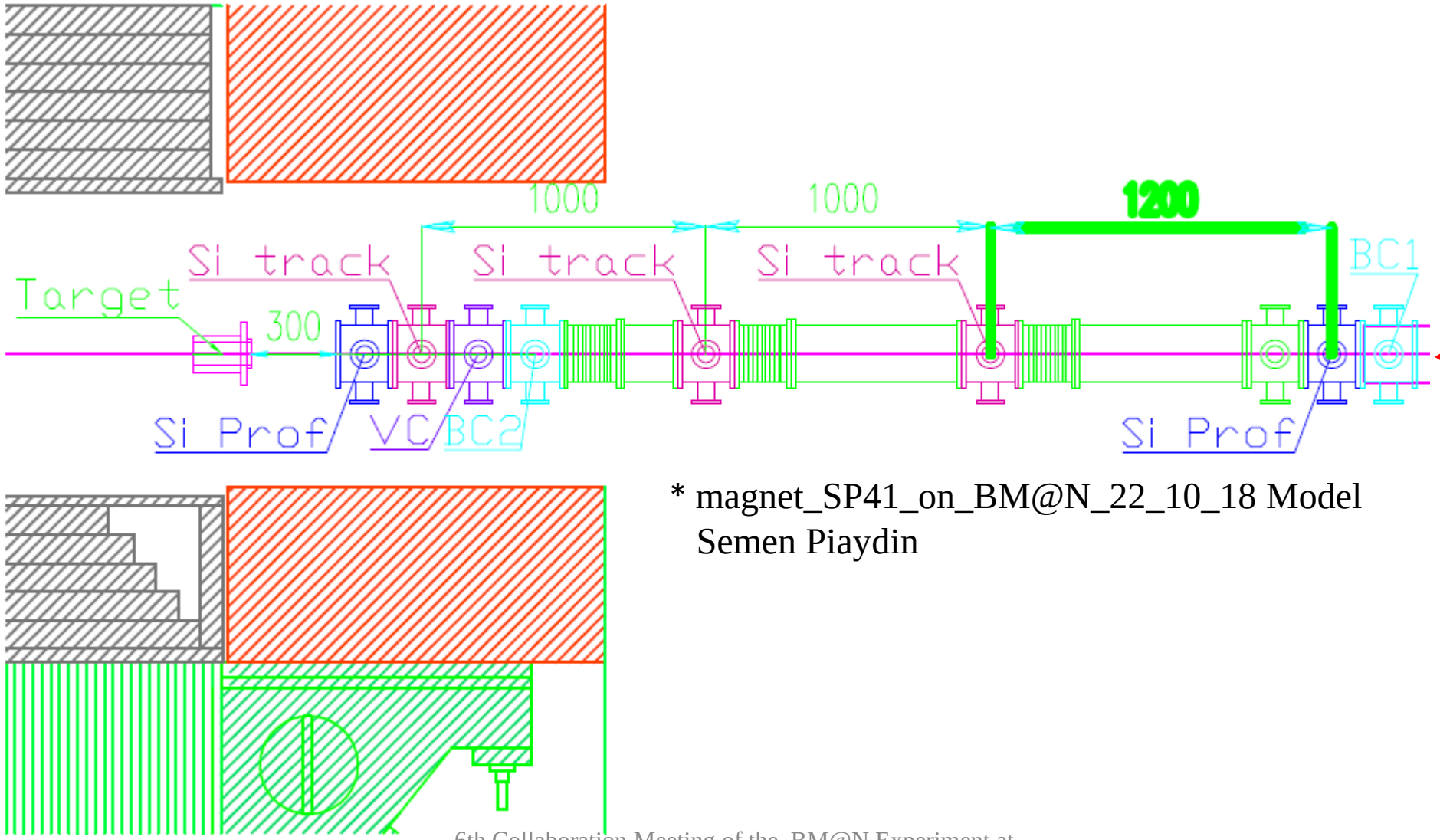
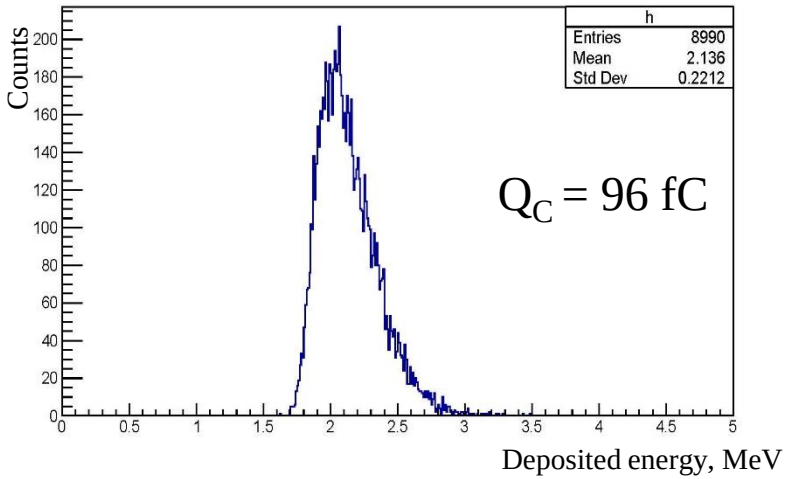
Detectors before the analyzing magnet



* magnet_SP41_on_BM@N_22_10_18 Model
Semen Piaydin

Simulation of deposited energy in 175 um silicon

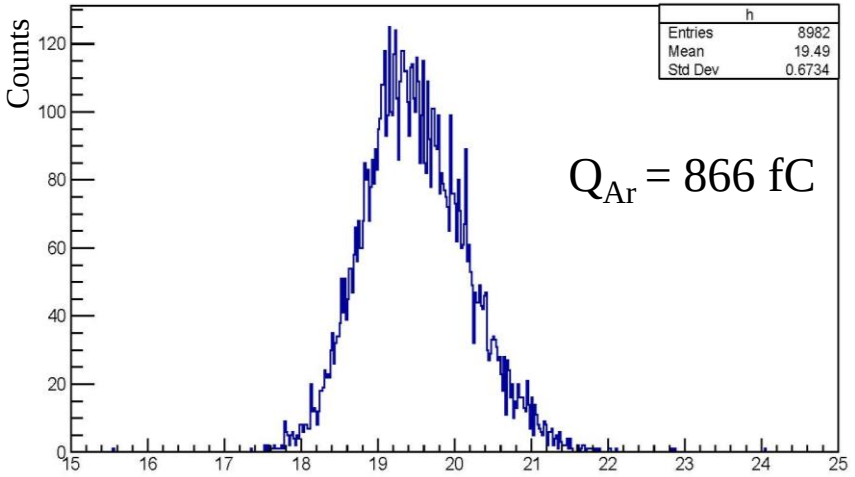
Carbon 4 AGeV ions deposited energy



Q_C = 96 fC

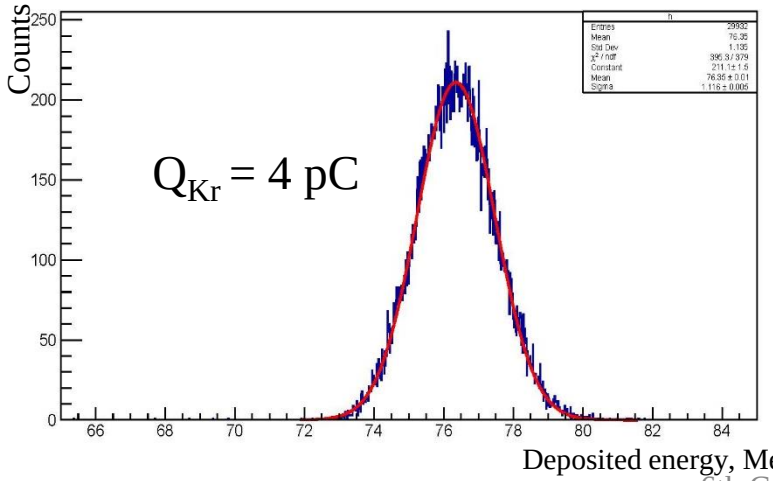
VA163 (IDEAS) as FEE ASICs for *light ions*

Argon 4 AGeV ions deposited energy



Q_{Ar} = 866 fC

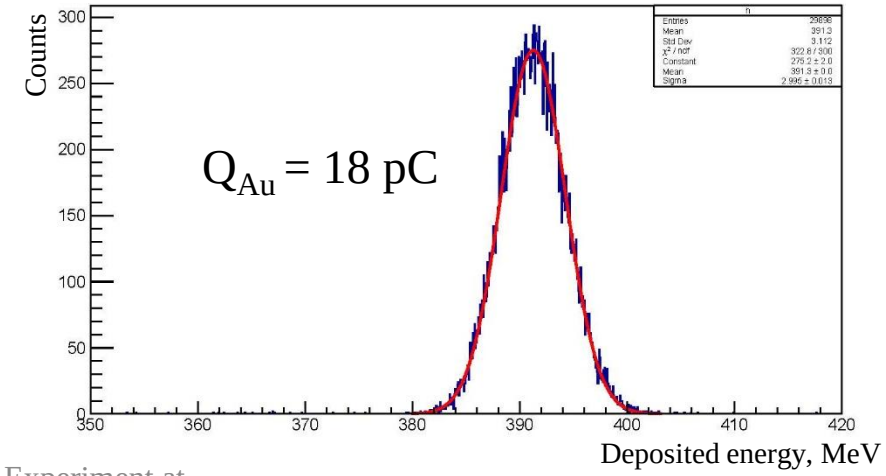
Krypton 4 AGeV ions deposited energy



Q_{Kr} = 4 pC

VA32HDR11, VATA64HDR16.2 for *heavy ions*

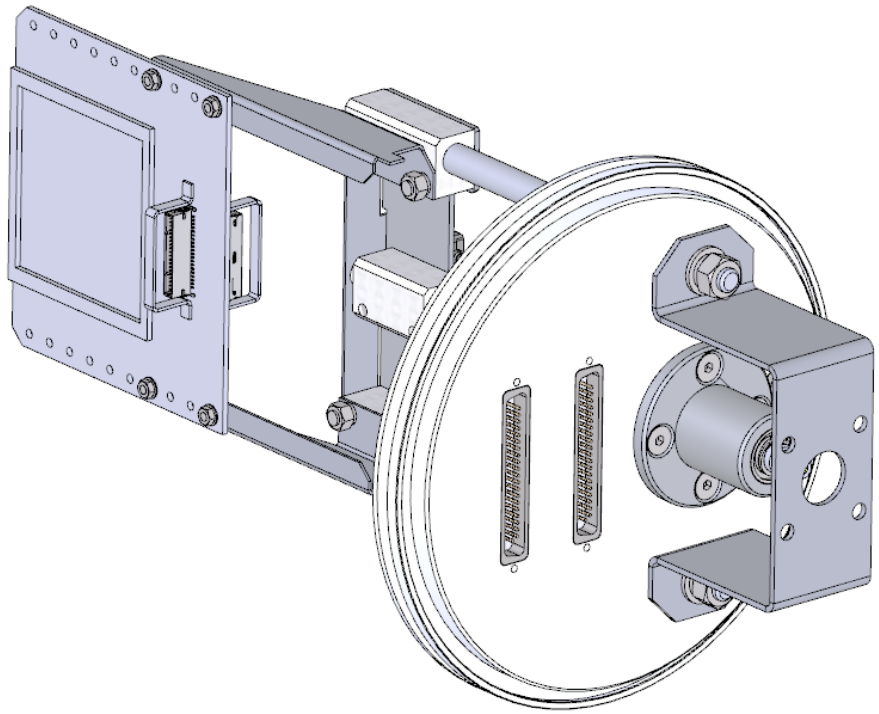
Gold 4 AGeV ions deposited energy

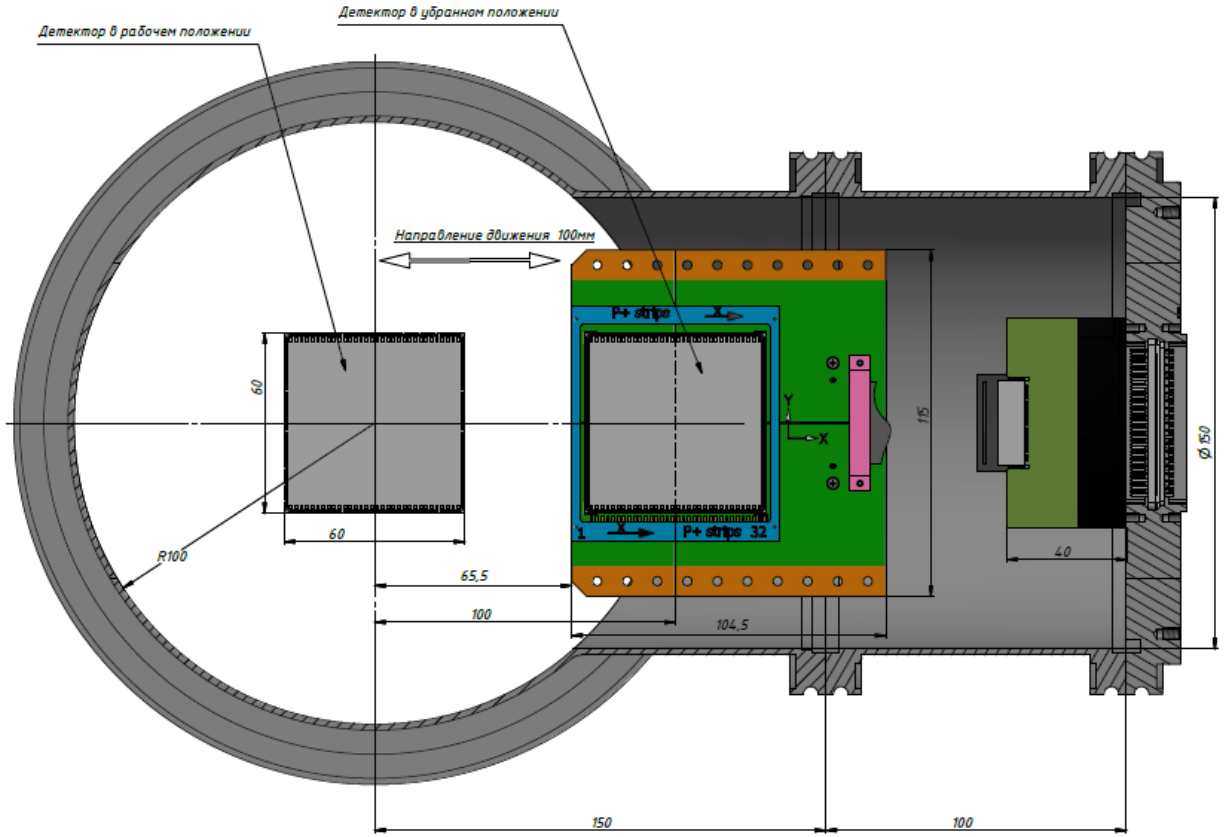


Q_{Au} = 18 pC

Beam profilometer status

Beam direction



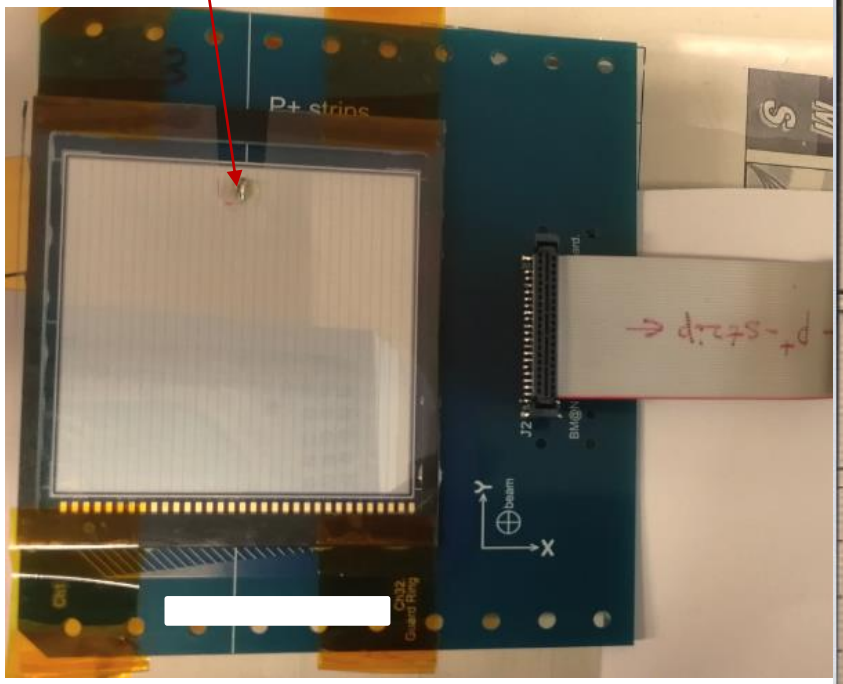


New vacuum flange construction with pneumatic drive to move the coordinate detector

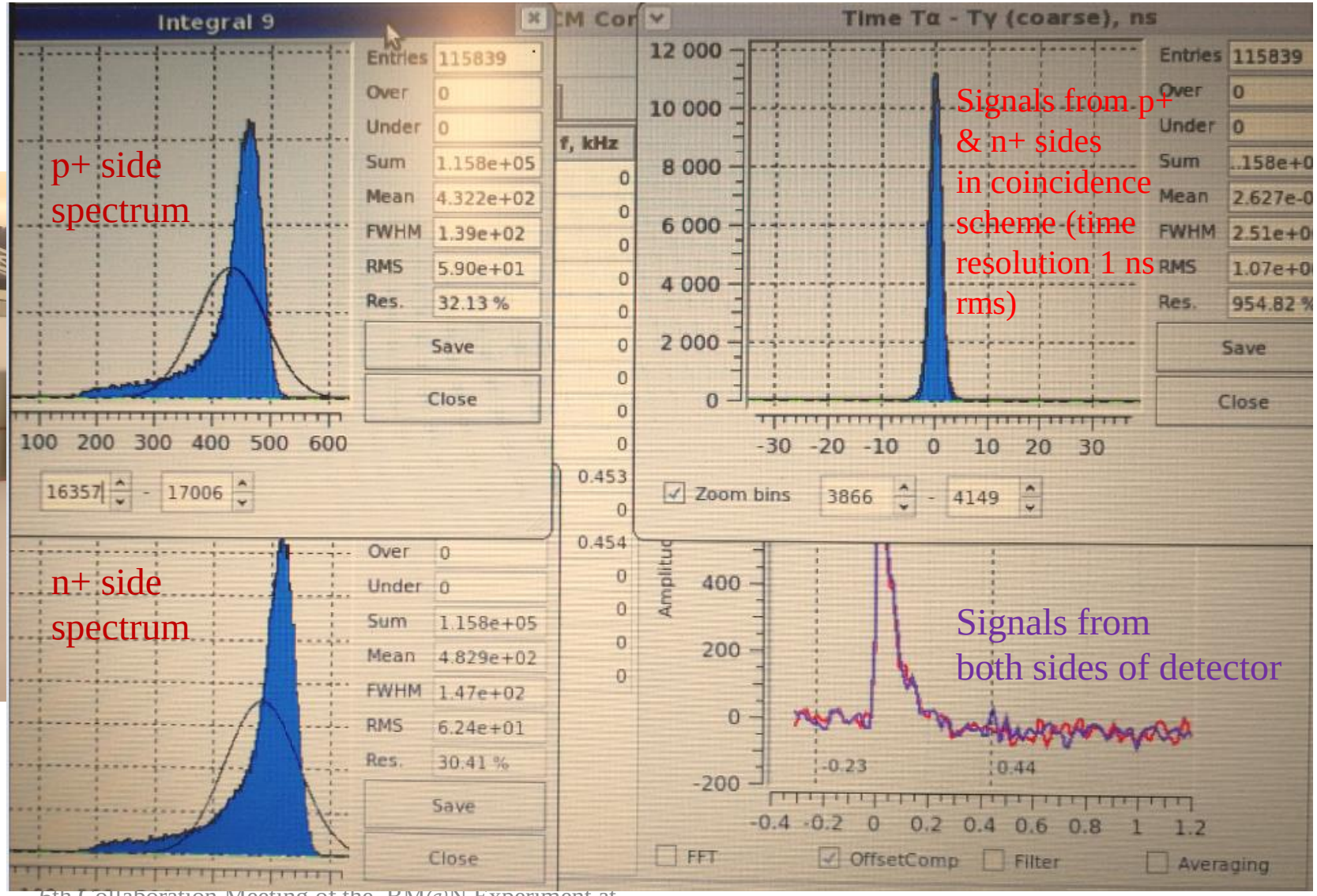
Beam profilometer (32x32 strips, thickness 175 um) inside beam-pipe

First test of beam profilometer Si detector

^{241}Am (E=5.5 MeV)



Silicon detector (32x32 strips) assembled at PCB, p+ side



Beam profilometer status summary

Silicon Detectors assembled on PCBs and tested (4 planes);
FEE electronics design in progress (first version tested with profilometer prototype) based on ASICs:

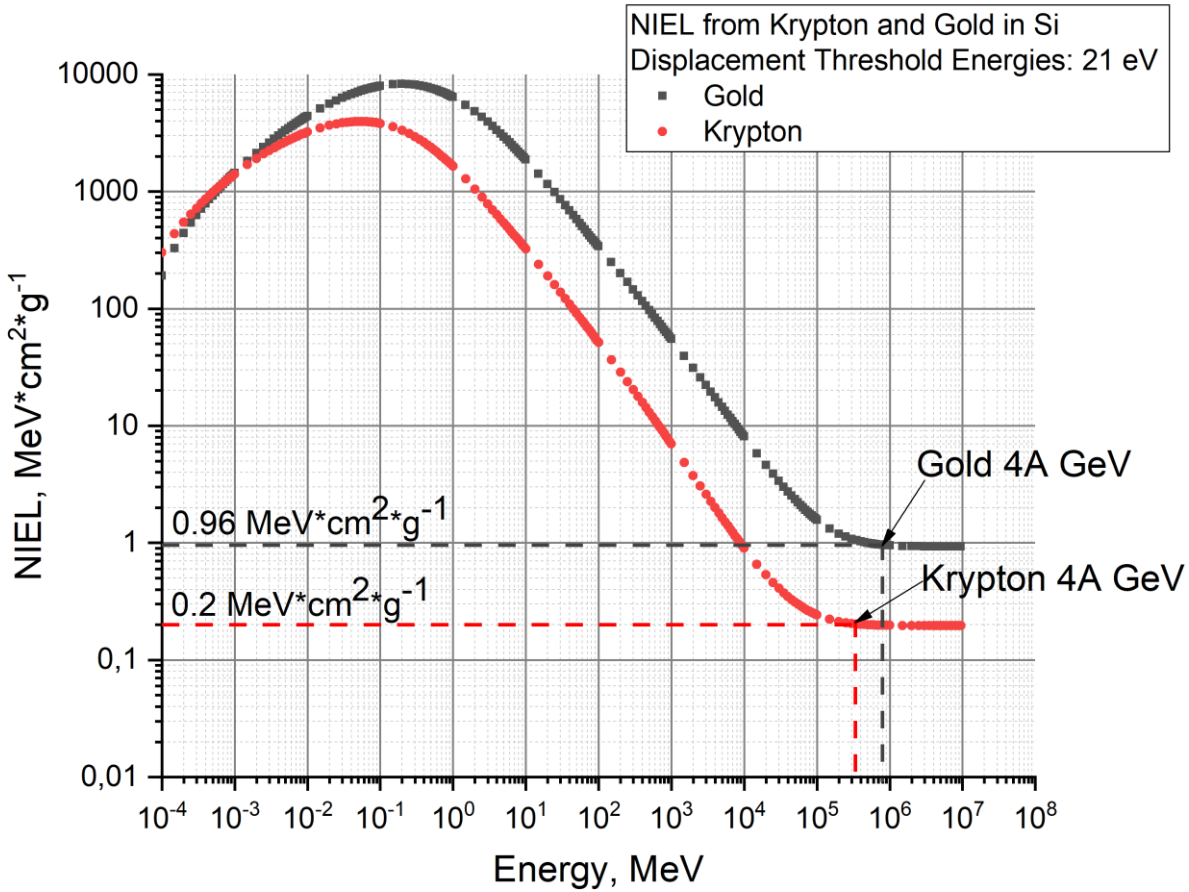
* VA163+TA32 (Dynamic Range: ±750 fC) – «light» ions up to argon;
* VA HDR16+TA32 (Dynamic Range ± 30 pC) – «heavy» ions from krypton to gold;

Design in progress:

* 16-channel ADC and autonomous DAQ;
* cross-boards for assembling FEE PCBs on flange;
* mechanical supports/flange+cooling FEE/

Ready to assembly on flange – March 2021

Expected radiation damage of beam tracker



SR-NIEL modeling results of NIEL in silicon detector for Kr^{36+} (red) and Au^{79+} (black) ions.

NIEL from 1 MeV neutron in Si (ASTM Standard E722-09):
NIELn=0.00204 MeV*cm^2* g^{-1}
Hardness factor of 4A GeV Gold: NIELgold/NIELn≈470;
Hardness factor of 4A GeV Krypton: NIELkrypton/NIELn≈98;

Radiation conditions in beam tracker positions:
Beam diameter: d=3 cm;
Flux of ^{197}Au: F=10^6 nucl./sec;
Time of irradiation: t=2 months;
$NIEL_{Au}(4\ GeV/nucl)$=$9.6107 \cdot 10^{-1}\ MeV \cdot cm^2 \cdot g^{-1}$;

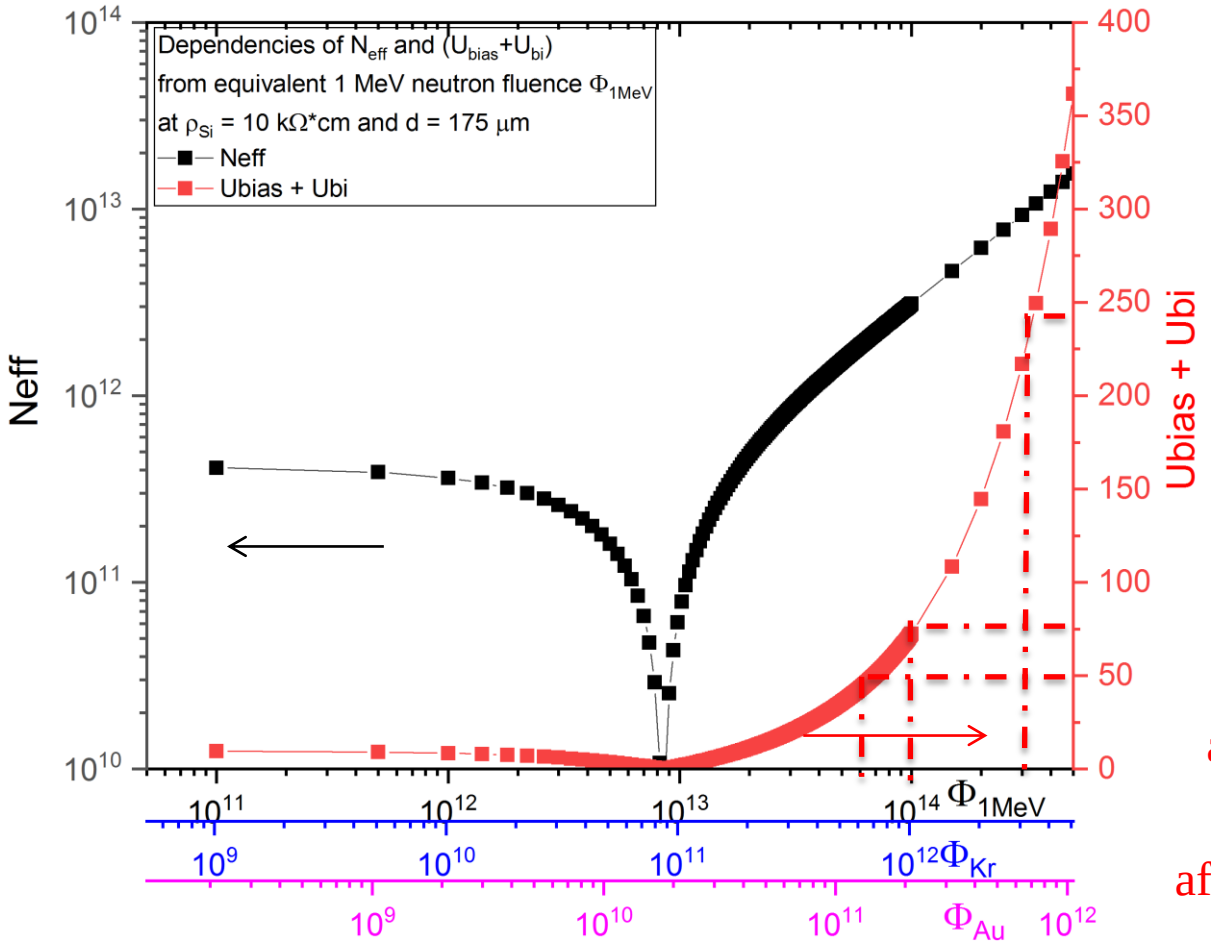
$$\Phi_{1MeV} = \frac{NIEL_{Au}(4\ GeV/nucl)}{NIEL_{neutrons}(1\ MeV)} \cdot \Phi_{Au} = \\ = \frac{NIEL_{Au}(4\ GeV/nucl)}{NIEL_{neutrons}(1\ MeV)} \cdot \frac{4 \cdot F \cdot t}{\pi \cdot d^2} \approx 3.45 \cdot 10^{14}\ cm^{-2}$$

Expected total dark current increase after 2 months at +20 Cº (without self annealing):

$$\Delta I = \alpha \cdot S_{beam} \cdot h_{detector} \cdot \Phi_{1MeV} = \\ = 5 \cdot 10^{-17} \cdot 7.07 \cdot 175 \cdot 10^{-4} \cdot 3.45 \cdot 10^{14} = 2.13\ mA$$

Expected dark current increase of 1 strip in beam zone: $\Delta I \approx 35$ μA

Expected radiation damage of beam tracker



Dependencies of Neff (black) and Ubias+Ubi (red) from equivalent 1MeV neutron fluence

Expected change of Neff and full depletion voltage (without self annealing):

$$N_{eff} = N_{0eff} \cdot e^{-c \cdot \Phi_{1MeV}} - \beta \cdot \Phi_{1MeV}$$

$$U_{bias} + U_{bi} = \frac{e \cdot |N_{eff}| \cdot d^2}{2 \cdot \varepsilon_0 \cdot \varepsilon}$$

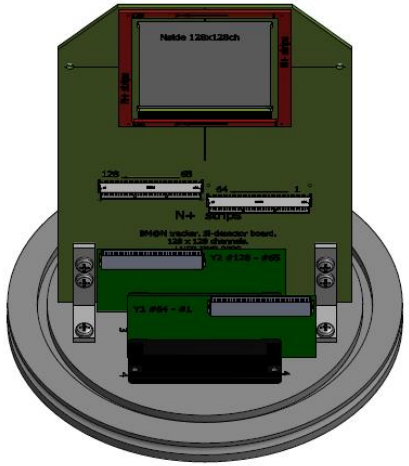
U_{bias} - silicon detector bias voltage;
$U_{bi} \approx 0.65$ V – built-in potential;
c = $5.5 \cdot 10^{-14}$ cm^2 – donor removal coefficient;
$\beta = 0.031$ cm^{-1}– acceptor creation coefficient

$U_{bias} + U_{bi}$ increase up to 72 V
after $\Phi_{1MeV} = 1 \cdot 10^{14}\ cm^{-2}$ (10^6 Au ions/sec [2.5 weeks irrad.])

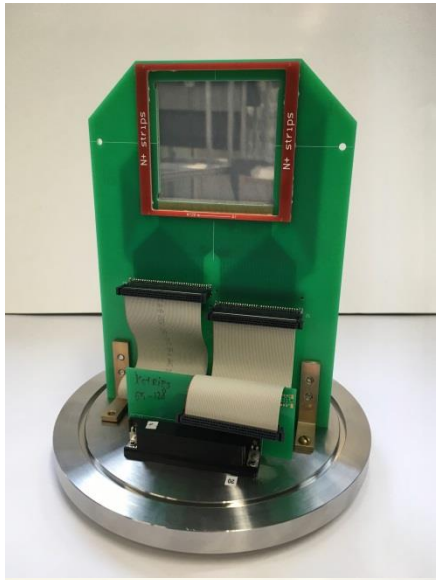
$U_{bias} + U_{bi}$ increase up to 250 V
after $\Phi_{1MeV} = 3.45 \cdot 10^{14}\ cm^{-2}$ (10^6 Au ions/sec [2 months irrad.])

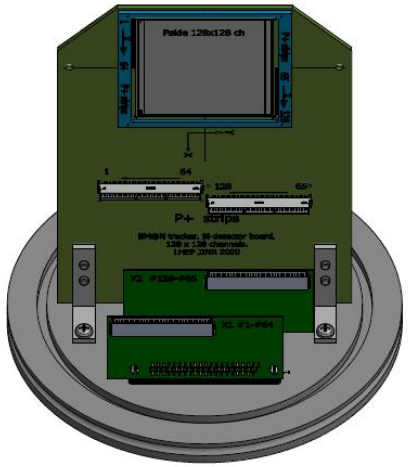
Expected max. power dissipation per 1 strip
at V_{bias}= 250 V : $P \approx 8.75$ mW

Beam tracker

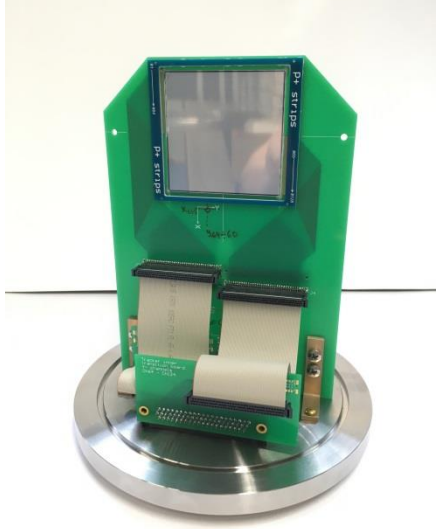


n+ Side



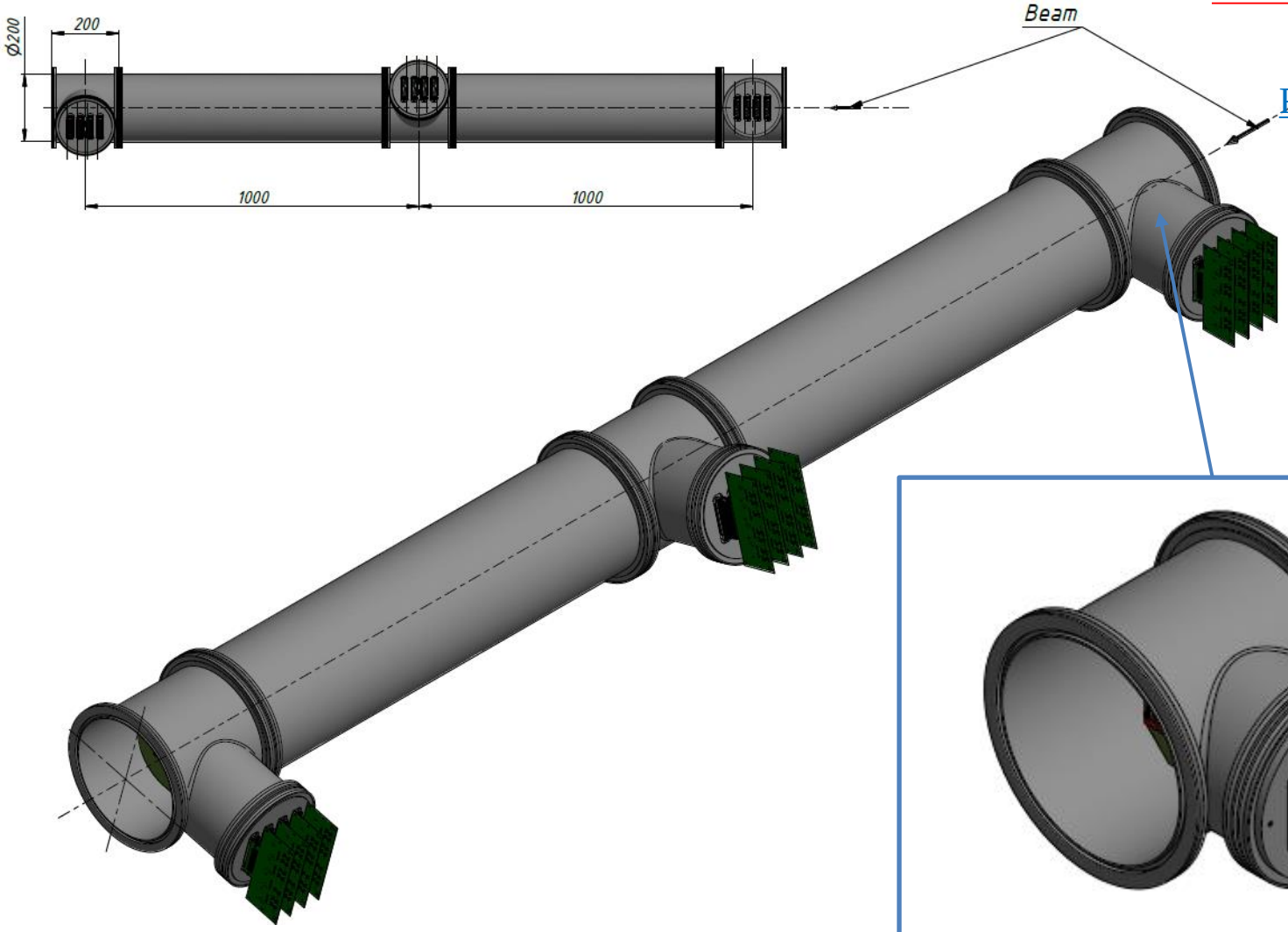


p+ Side



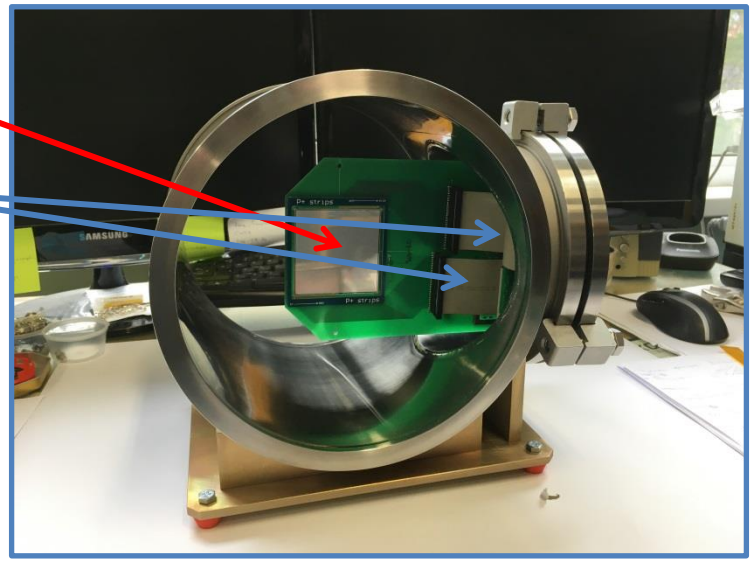
Beam tracker coordinate plane (128x128 strips, thickness 175 um) assembled at vacuum flange.

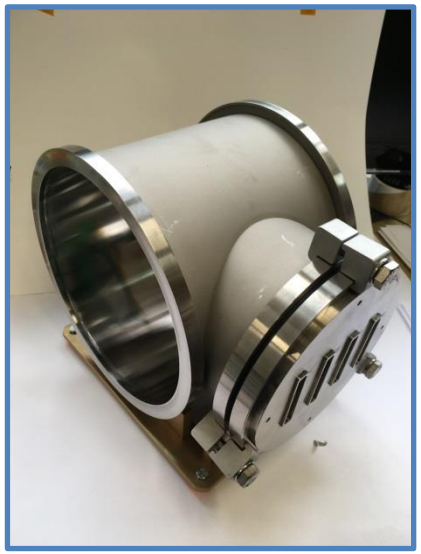
Beam pipe section with beam tracker modules ±15°



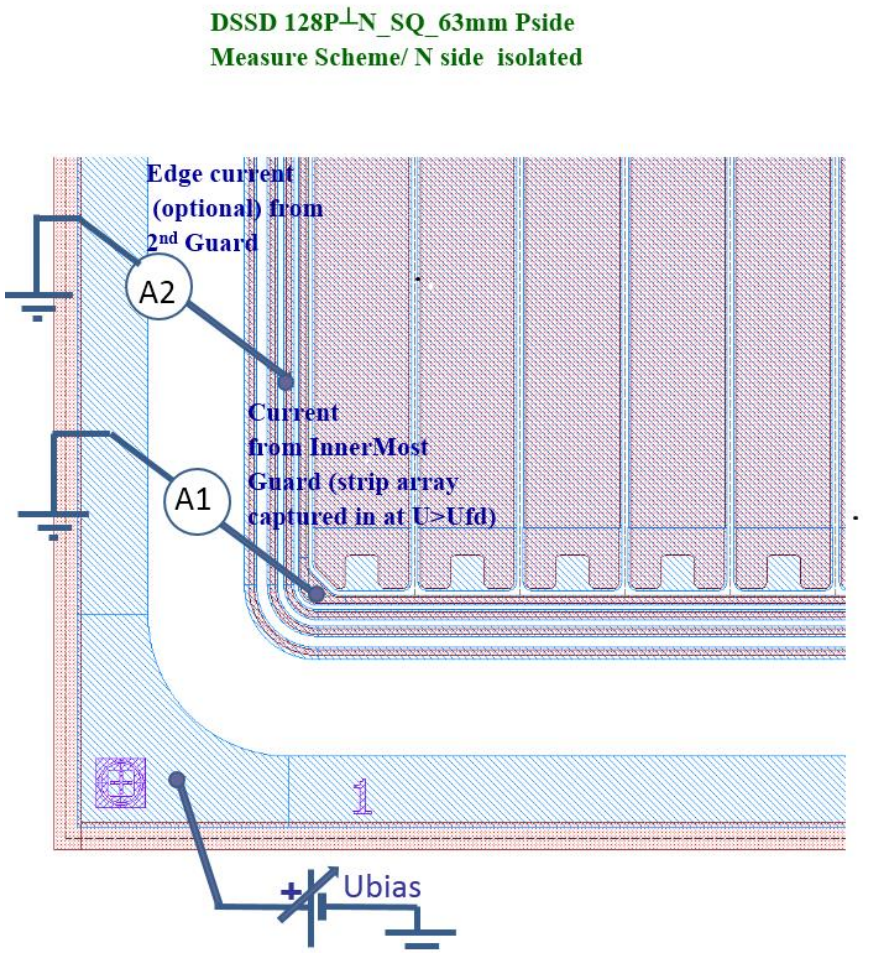
Beam tracker sensor

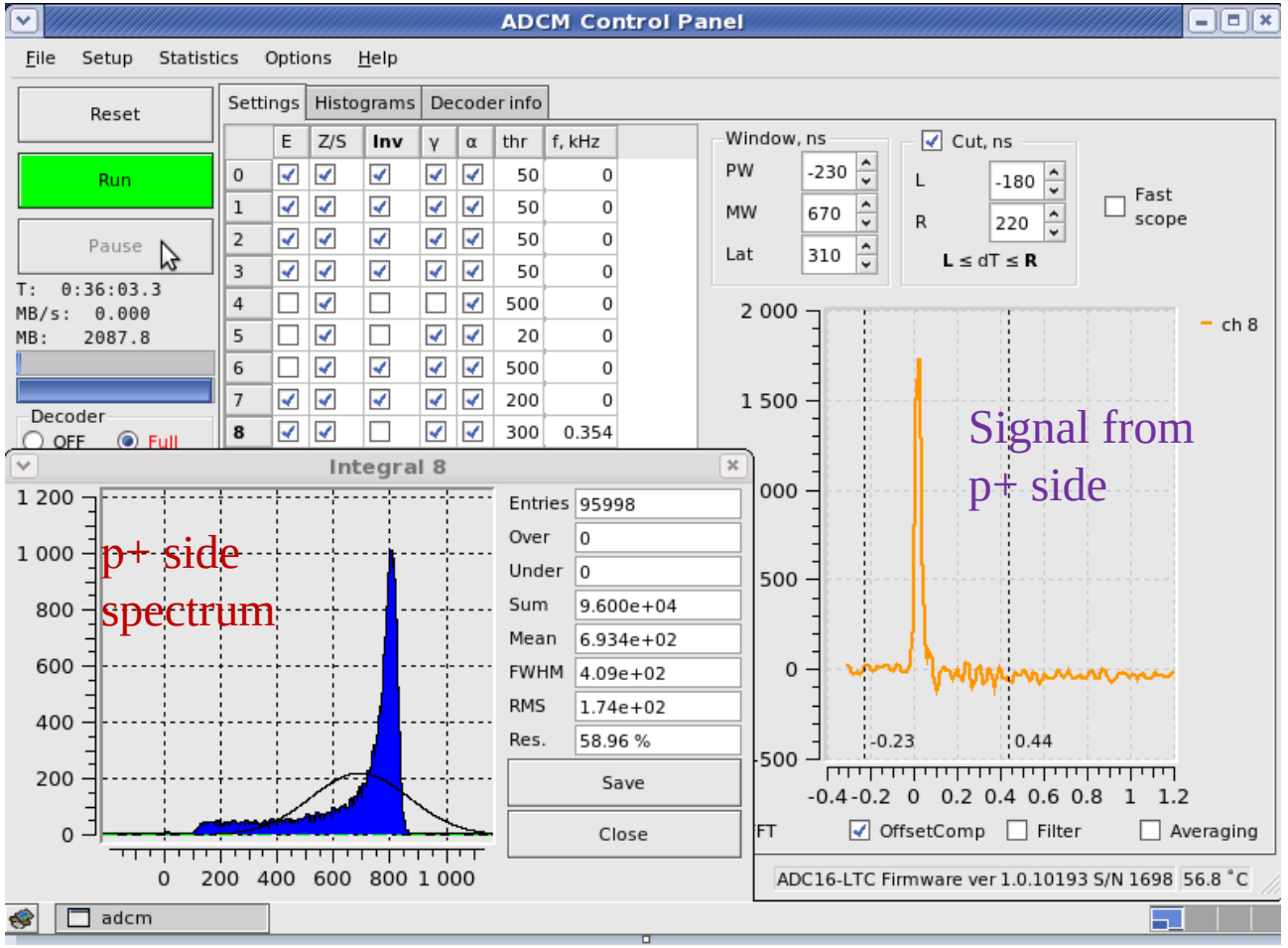
Readout cables





First test of beam tracker Si detector





Beam tracker status summary

Silicon Detectors assembled on PCBs and tested (3 planes);
FEE in progress based on ASICs:

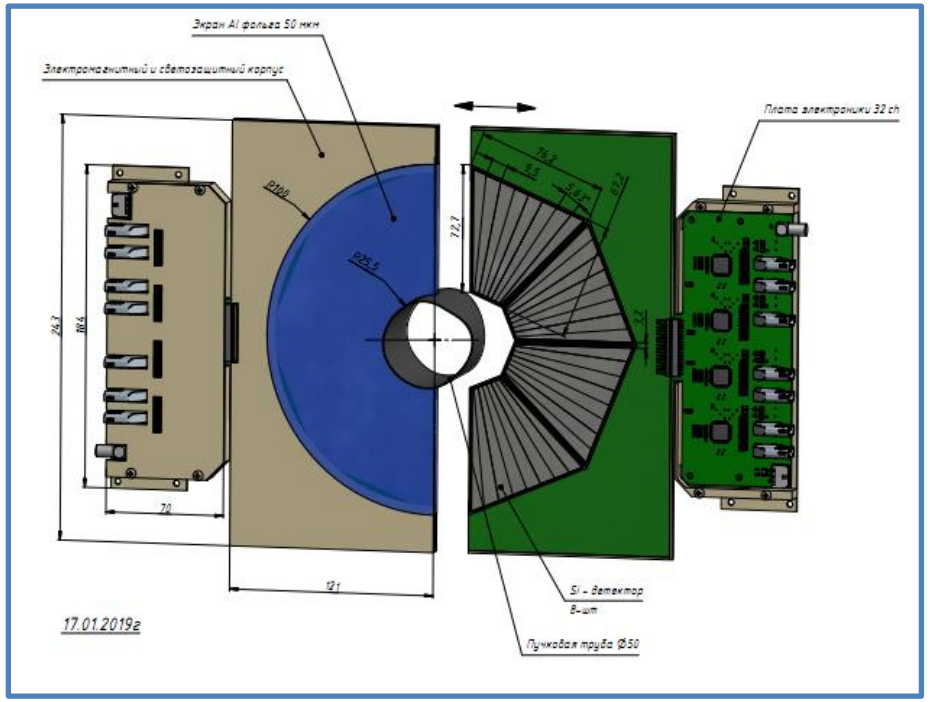
* VATA64HDR16.2 with high Dynamic Range : -20 pC ÷ +50 pC;

FEE design for «light» ions based on VA163+TA32 (Dynamic Range : ± 750fC) – will be started after VATA64HDR16.2 first tests;
Design in progress:

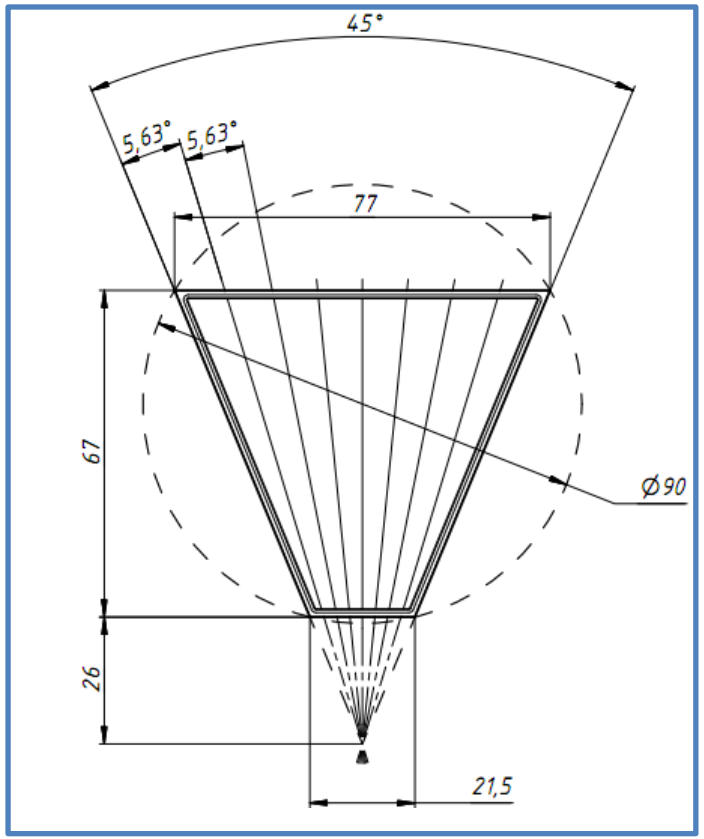
* cross-boards for assembling FEE PCBs on flange;
* mechanical supports/flange+cooling FEE/

Ready to assembly on flange: February – March 2021

First test of beam tracker Si detector



General view of multiplicity trigger which consists of 2 half-planes (8 silicon strip trapezoid detectors, thickness 525 um) and 2 FEE boards.



Multiplicity trigger detector section (8 strips)

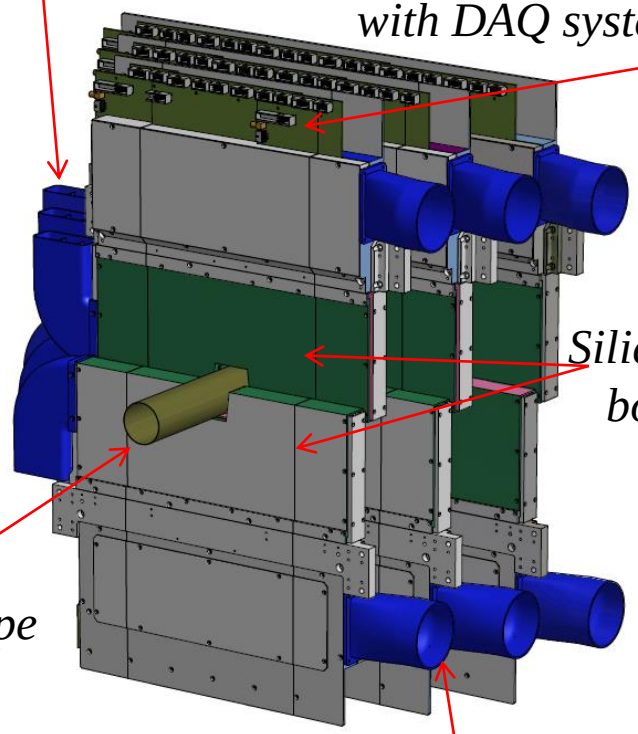
Multiplicity trigger status summary

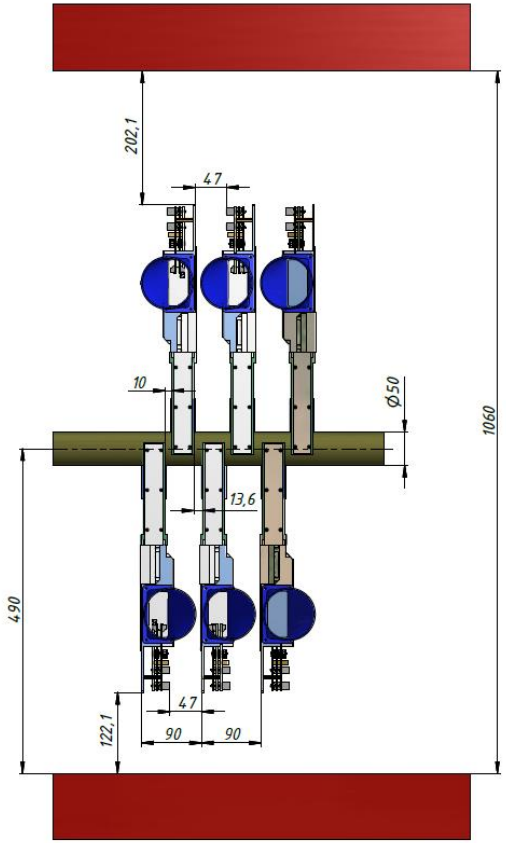
Trapezoid detectors – tested and ready to assembly on detectors PCBs
2 FEE boards with 32 channels (AST1-1) ready to assembly (version-2018)
Design in progress:

* 2 detectors PCB;
* light+EM-shielding for two half-planes;
* mechanical support

Ready to assembly on beam channel: July 2021

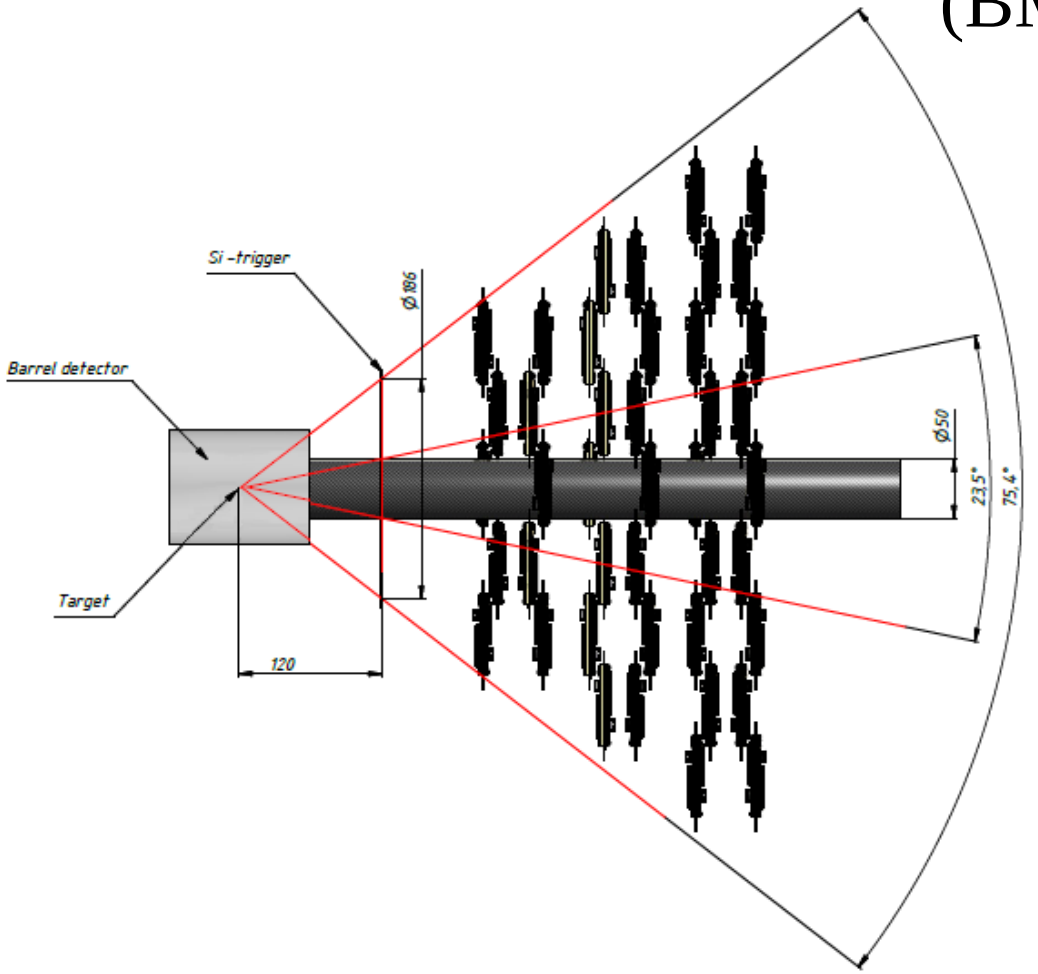
Forward Silicon Detectors Configuration (BM@N – 2020)

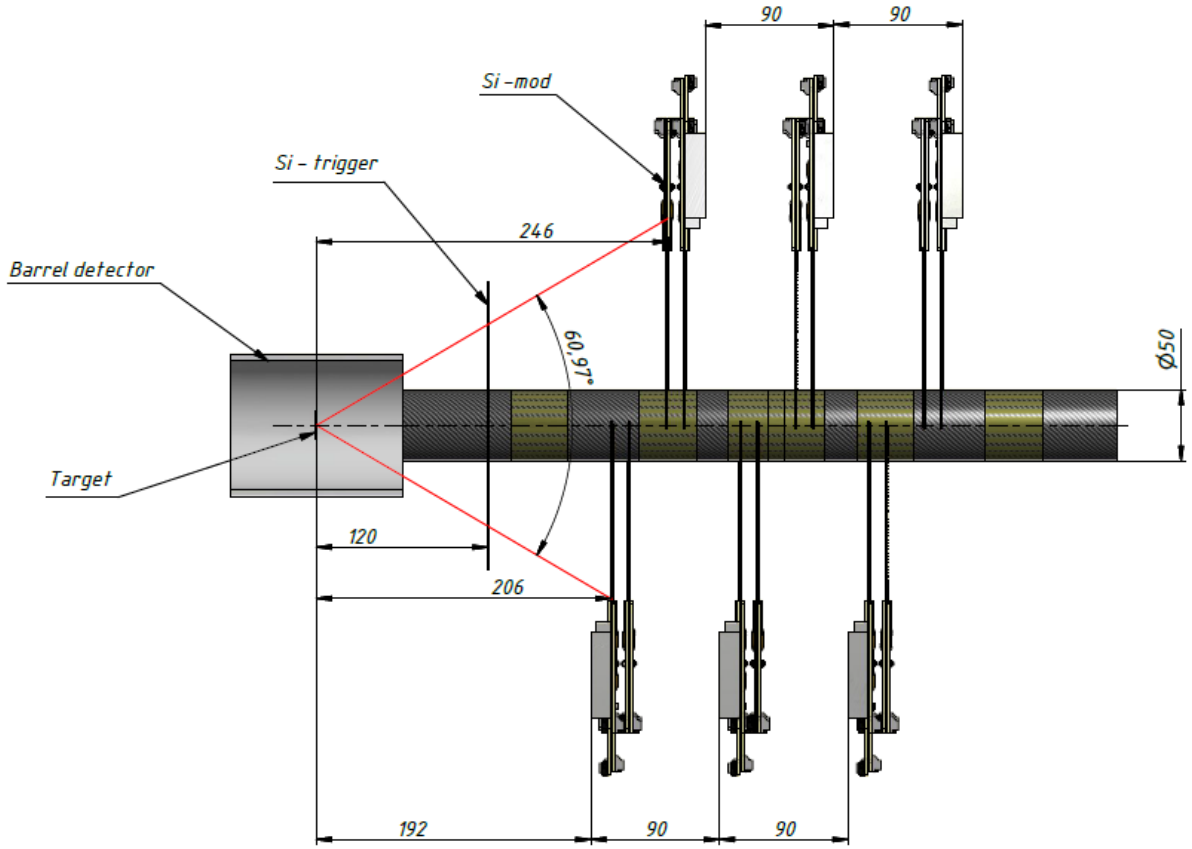




Forward Silicon Detectors in analyzing magnet

Forward Silicon Detectors Configuration (BM@N – 2020)



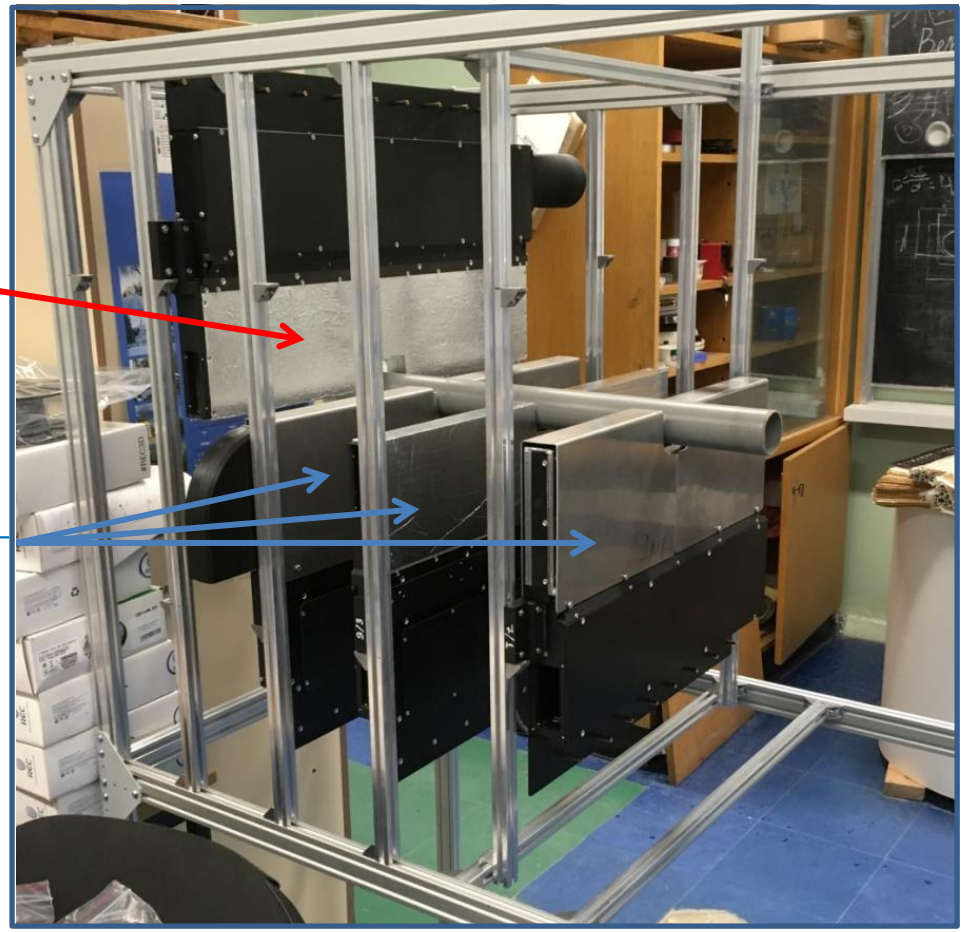


Positions of Si-planes on the beam-channel XZ (left) and YZ (right)

Forward Silicon Detectors Configuration (BM@N – 2020)

Light+EM-shielding

Mechanical protection of detectors during assembling

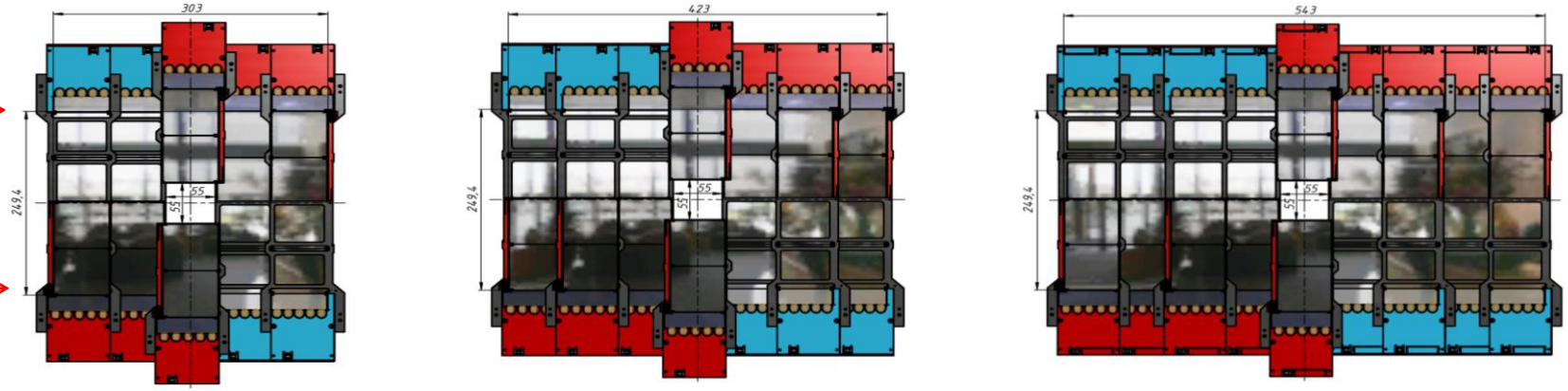


Prototype of mechanical support for Forward Silicon Detectors planes

Forward Silicon Detectors Configuration (BM@N – 2020)

Upper half-planes →

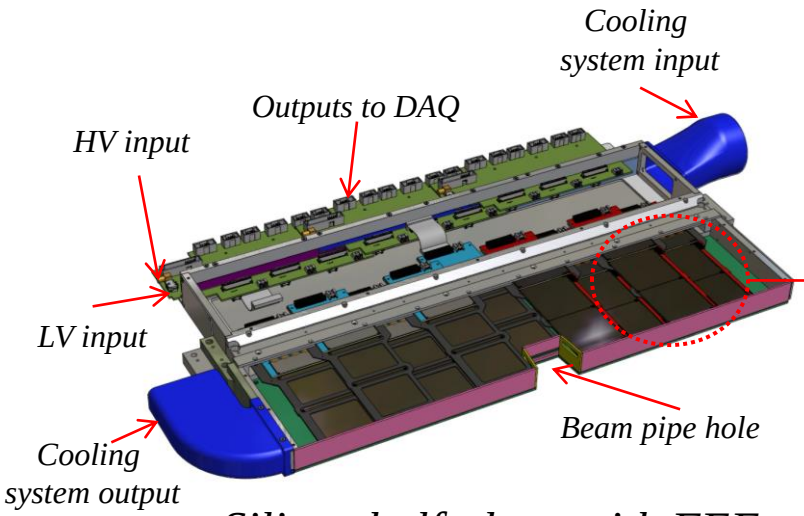
Bottom half-planes →



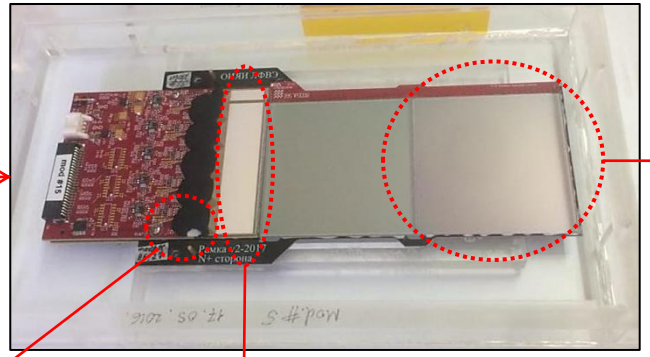
Three tracking silicon planes with FEE boards (using only one type of Silicon Detector Module!)

Number of	First Plane	Second Plane	Third Plane	Total
Si-modules 60x120 mm^2	10	14	18	42
DSSDs	20	28	36	84
ASICs (temp. <= +25 C°)	100	140	180	420
Power dissipation	28,16 W	39,42 W	50,69 W	118,27 W
PAs	20	28	36	84
FEE PCBs	20	28	36	84
Channels	12800	17920	23040	53760
Area, m^2	0.073	0.102	0.132	0.307

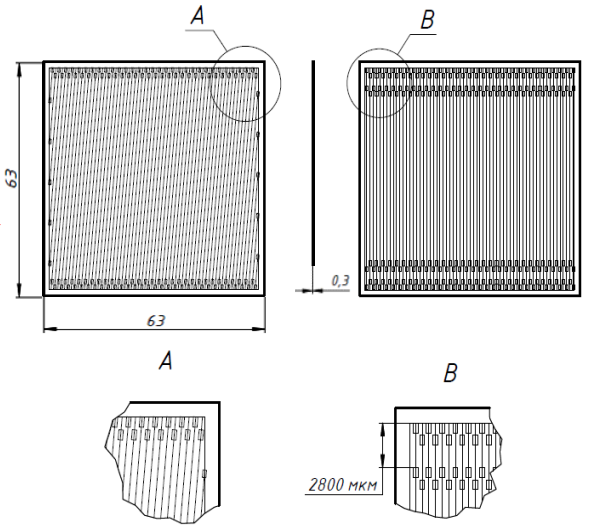
Silicon Detector Module

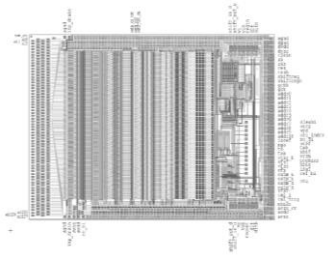


Silicon half-plane with FEE

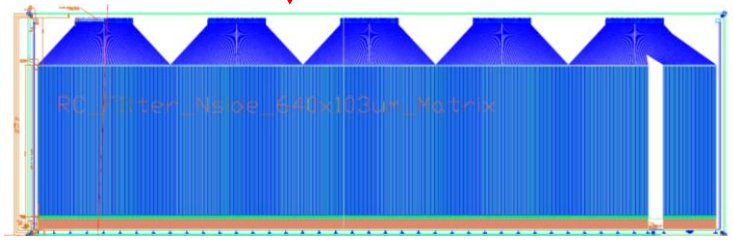


Silicon Detector Module





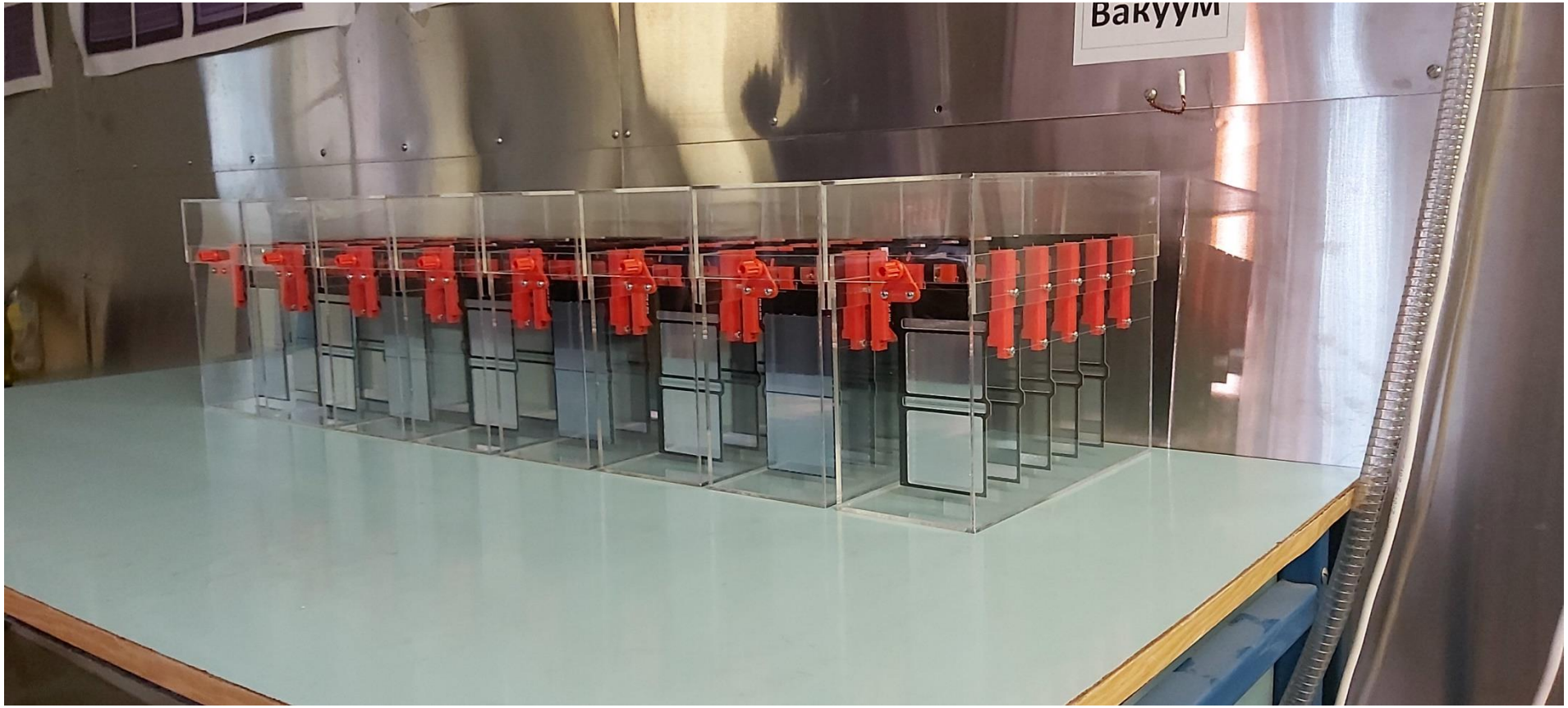
ASIC VATAGP7.1 (5 chips on each side of module)
Number of CSA: 128 channels
Dynamic range: ±30 fC
Peaking time (slow/fast shaper): 500 ns/ 50ns
Noise (ENC): 70e +12e/pF (typ.)
Voltage supply: +1.5 V, -2.0 V
Gain from input to output buffer: 16.5 μA/fC
Output Serial analog multiplexer clock speed: 3.9 MHz
Power dissipation per channel: 2.2 mW



Pitch Adapter (n+) side
sapphire plates with an epitaxial layer of silicon (SOI)
Number of channels: 640
Value of poly-Si resistors: ≈ 1 MΩ
Value of integrated capacitors: ≈ 120 pF
Capacitor working voltage: 100 V
Capacitor breakdown voltage: >150 V

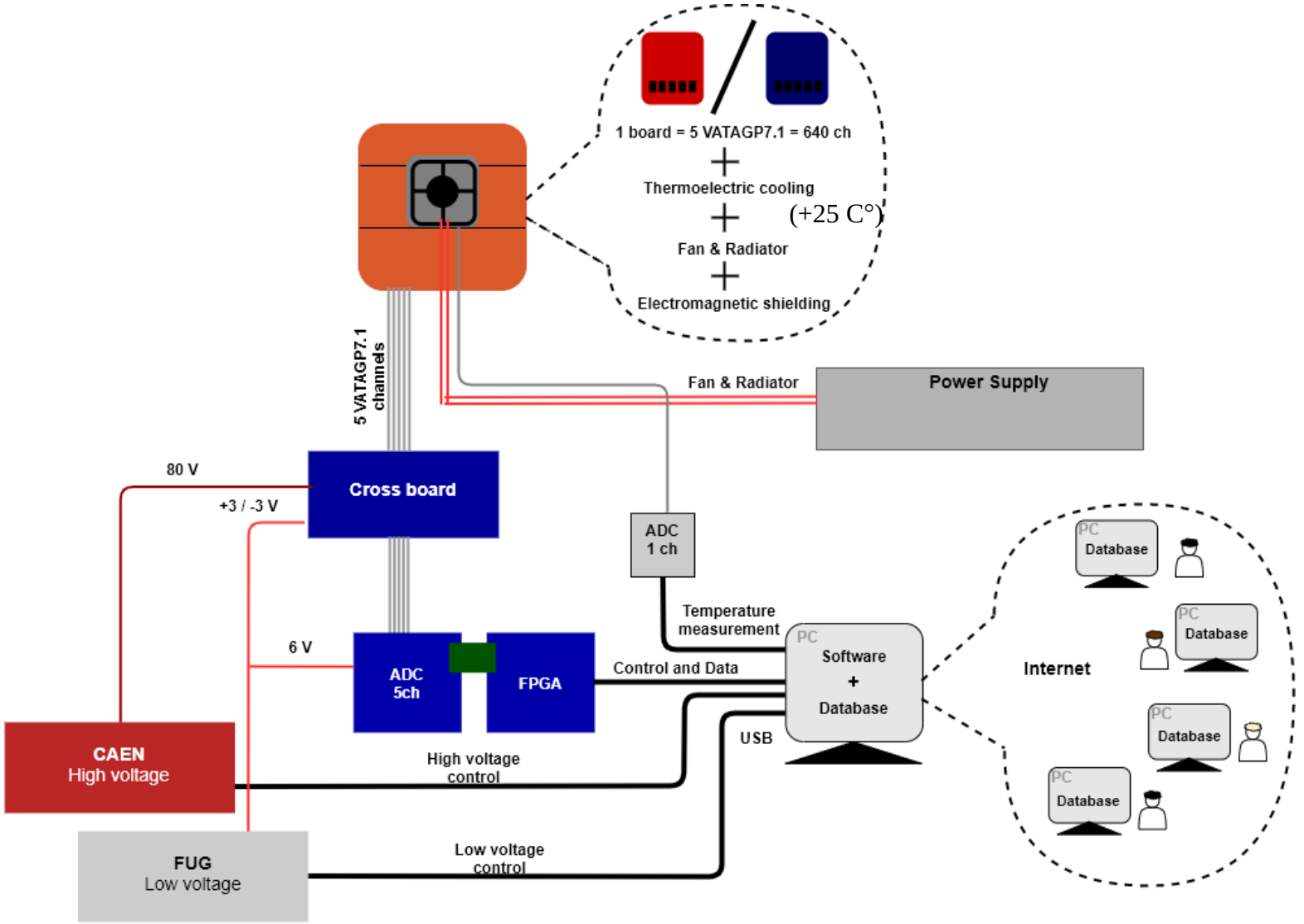
Size: 63x63x0,3 mm^3 (on 4" – FZ-Si wafers)
Topology: double sided microstrip (DSSD)
(DC coupling)
Pitch p^+ strips: 95 μm;
Pitch n^+ strips 103 μm;
Stereo angle between p^+/n^+ strips: 2.5^0
Number of strips/DSSD: 640 (p^+)× 614(n^+)
Number of strips/module: 640 (p^+)× 640(n^+)

Silicon Detector Modules



Silicon Detectors assembled on support frames

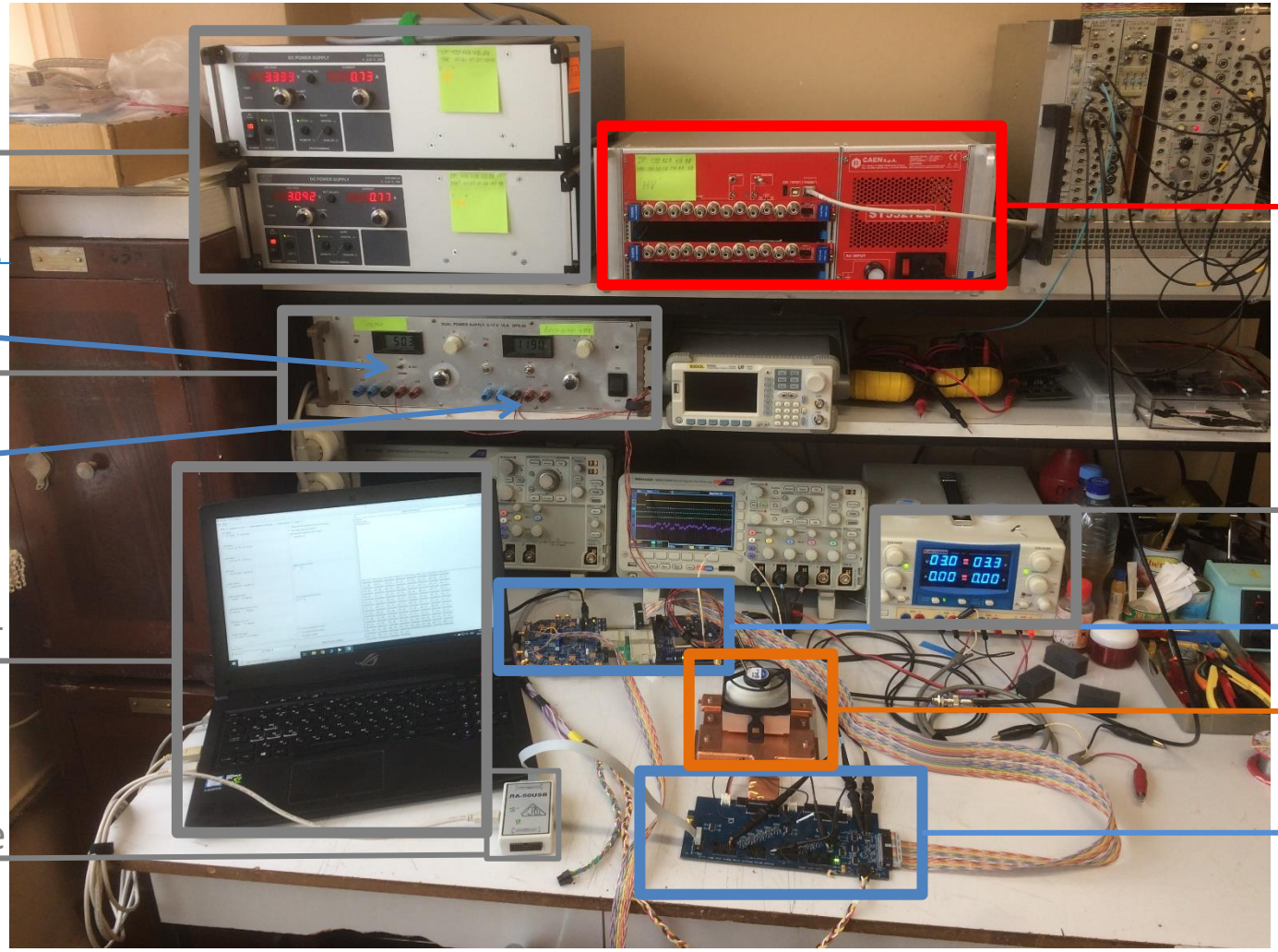
Front-end electronics test stand



Testing scenario:

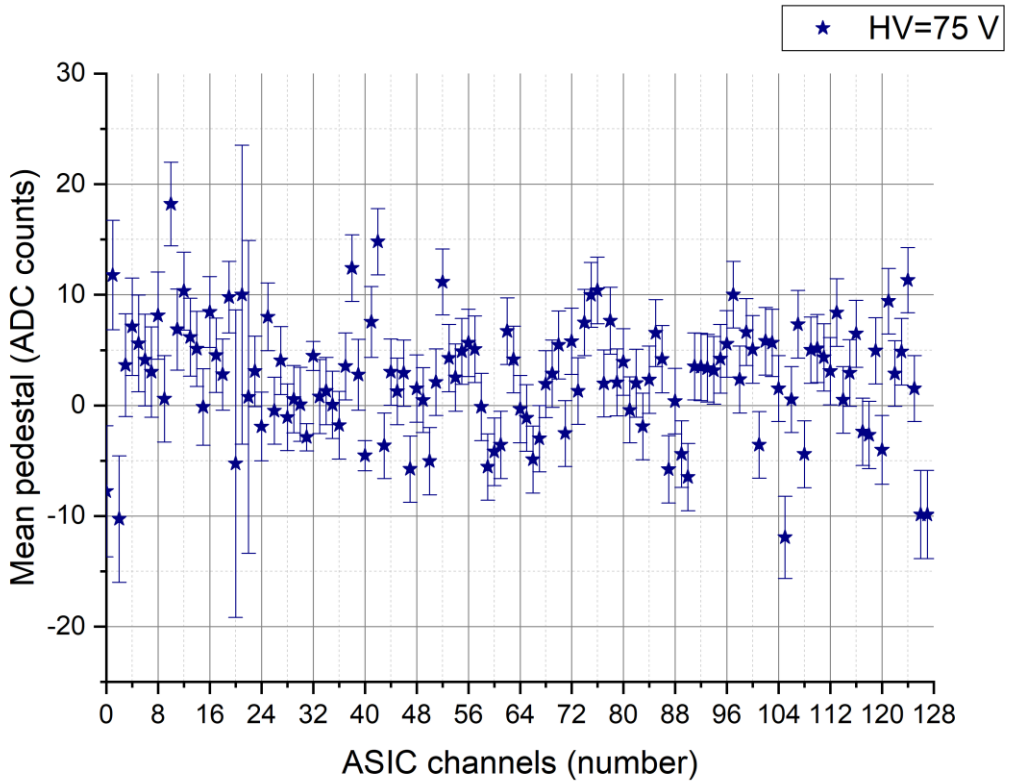
1. Connect PCB to stand (HV, LV and temperature will be measured whole time) in cooling and EM shielding box;
2. Make pedestal run for each chip without HV at pitch-adapter, save raw data;
3. Send configuration data to each chip;
4. Measure crosstalk between neighbor channels (external test signal);
5. Measure I(PA)= f(U_{HV}) leakage current of PA-640n+ (only for n+ PCB);
6. Measure ENC= f(U_{HV}) (only for n+ PCB);
7. Save data to the database.

Front-end electronics test stand

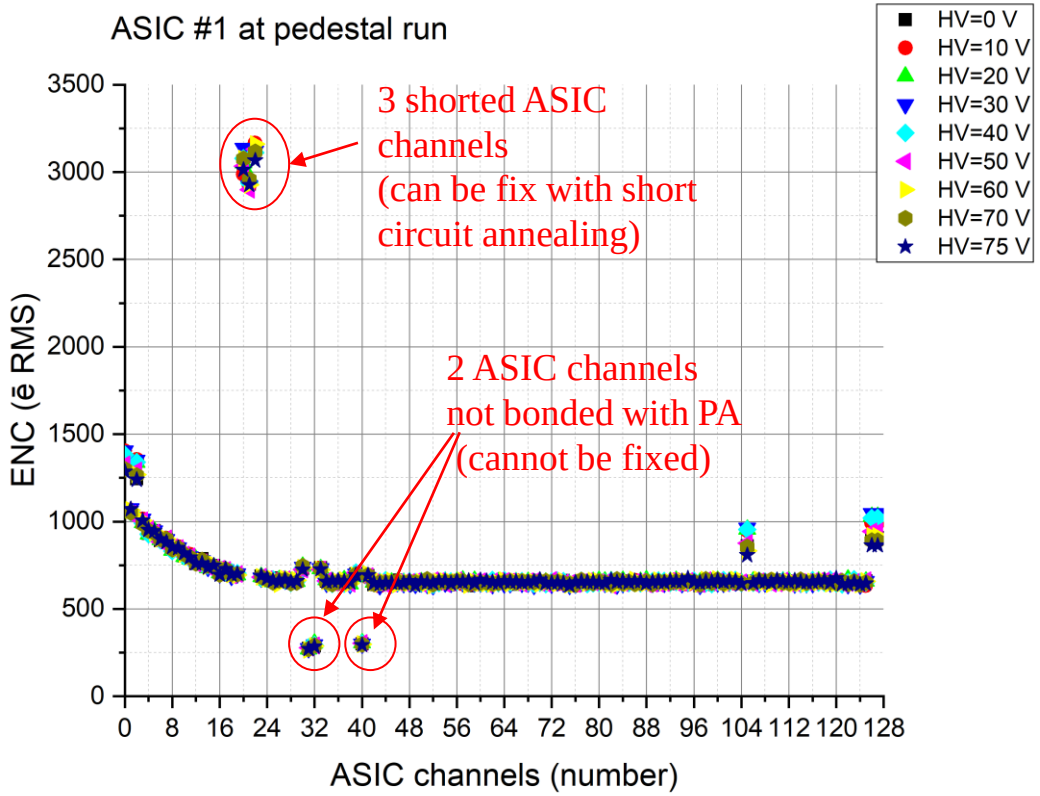


First FEE test results

Pedestal run red ASIC #1 PCB #40 read-out frequency 3.6 MHz
(numeration starts with 0th channel)



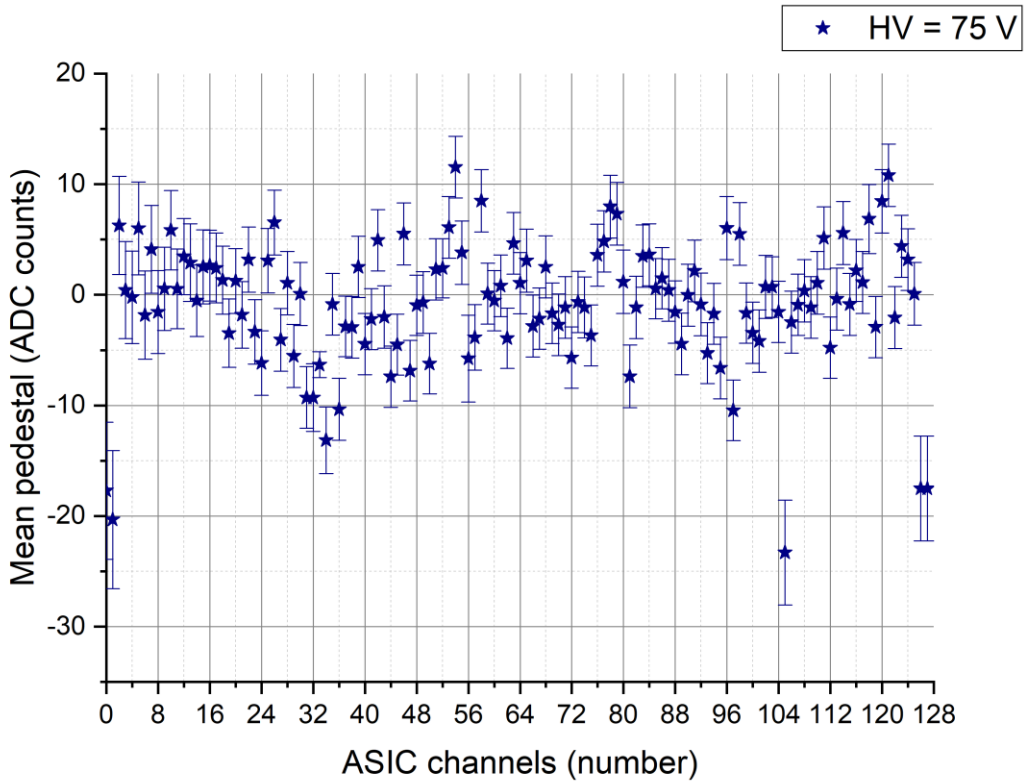
Mean pedestal per ASIC#1 channel



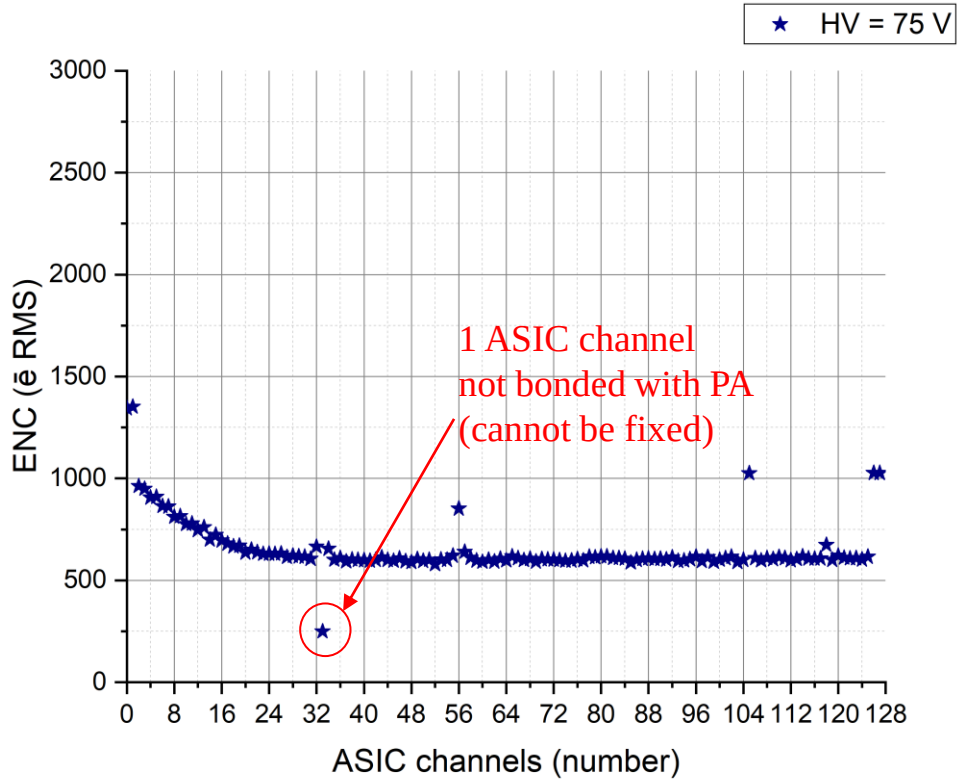
ENC per ASIC #1 channel
<ENC> = 685 ē RMS (without 3 shorted channels)

First FEE test results

Pedestal run red ASIC #2 PCB #40 read-out frequency 3.6 MHz
(numeration starts with 0th channel)



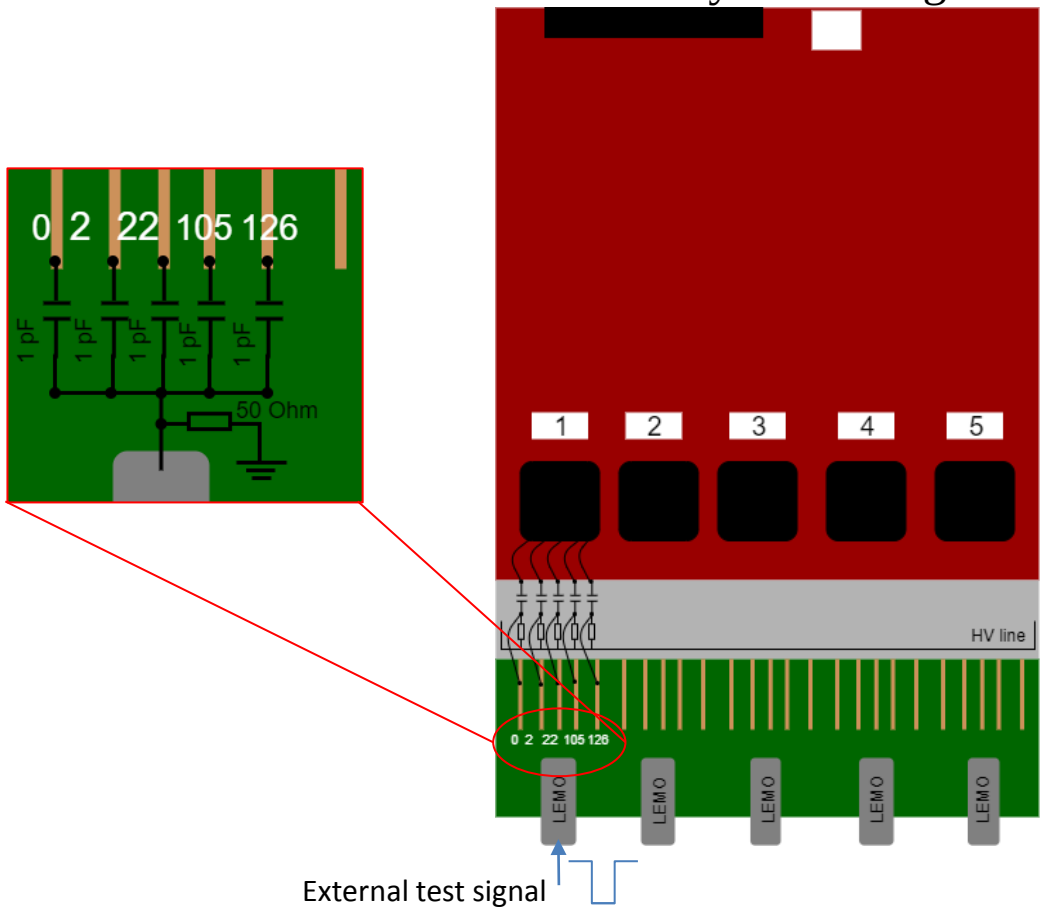
Mean pedestal per ASIC#2 channel



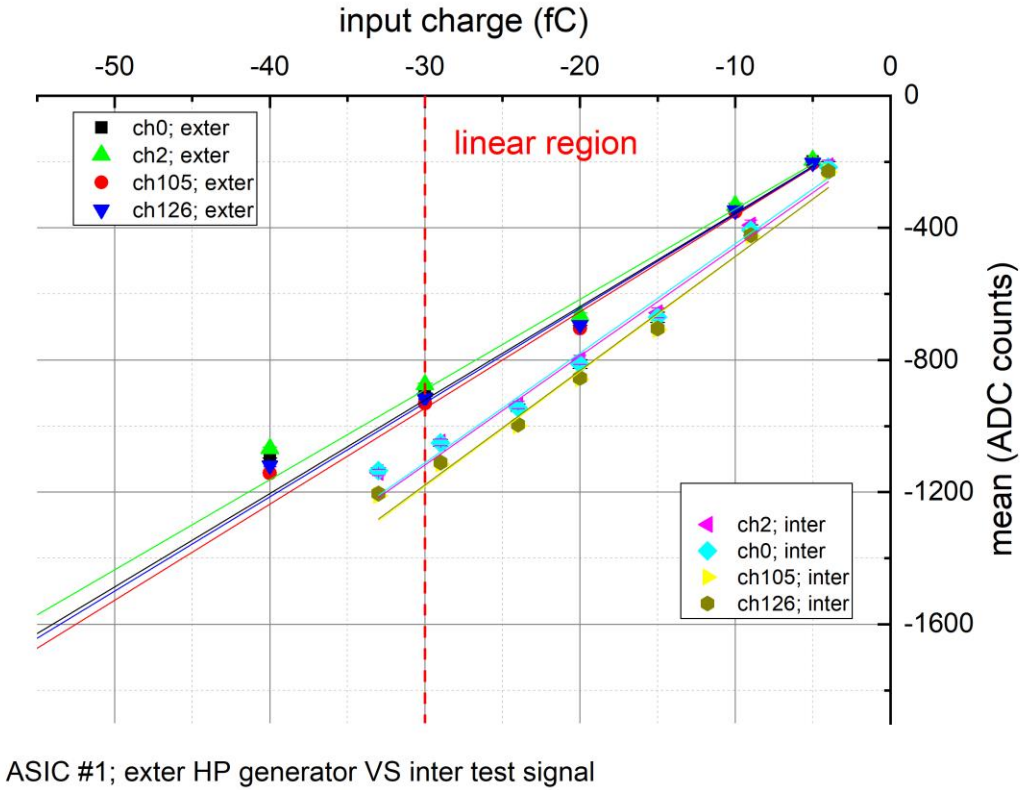
ENC per ASIC #2 channel
<ENC> = 654.9 ē RMS

First FEE test results

Dynamic range red ASIC #1 PCB #40 read-out frequency 3.6 MHz



Test signal connection for ASIC #1



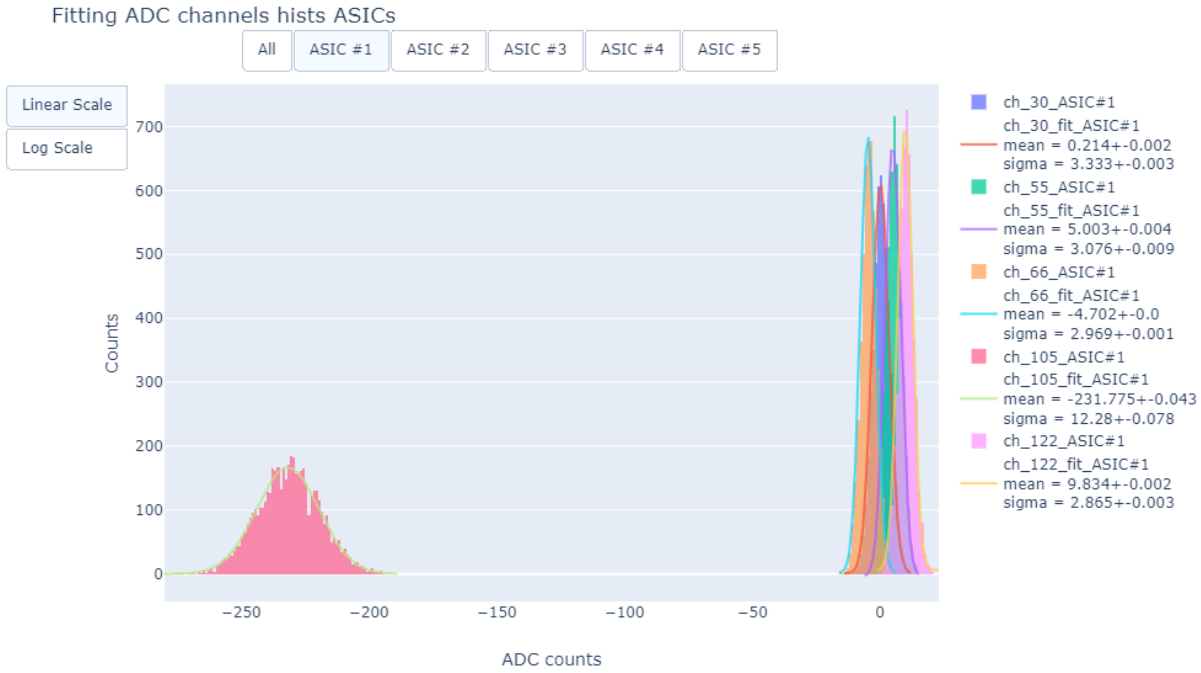
ASIC #1; exter HP generator VS inter test signal

ASIC #1 dynamic range from external and internal test signal in 0^{th} , 2^{nd} , 105^{th} , 126^{th} channels

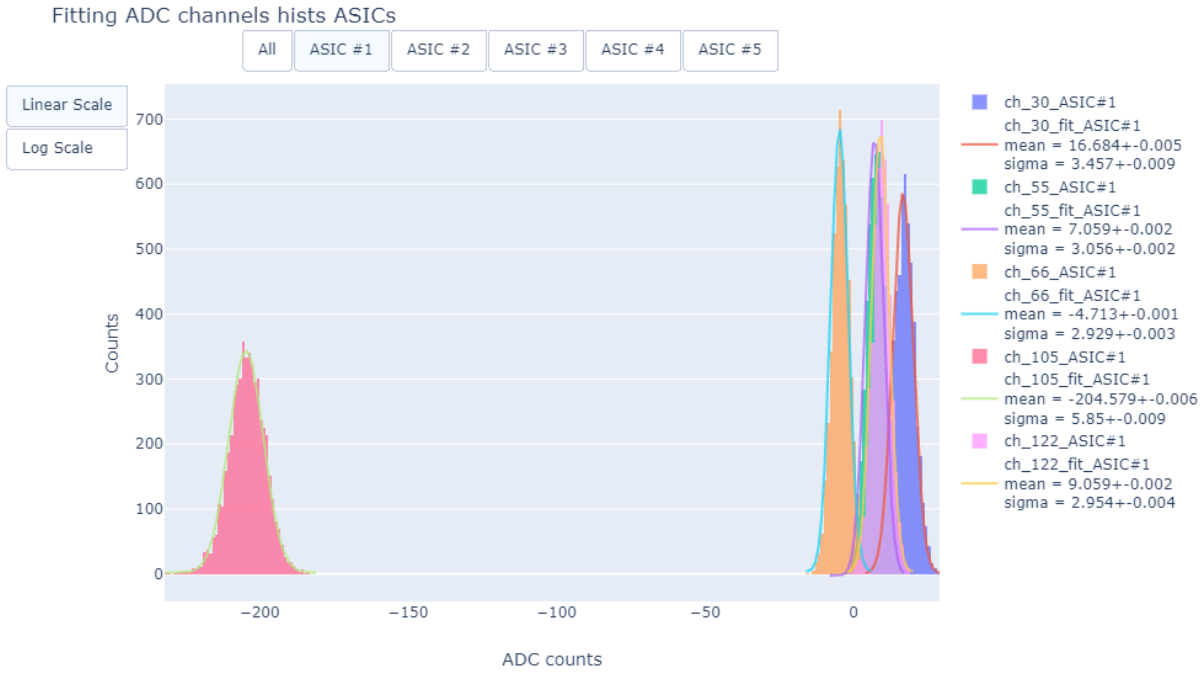
First FEE test results

Test signal -5 fC in 105th channel ASIC #1
red PCB #40 read-out frequency 3.6 MHz, HV = 75 V
(before pedestals subtraction)

Internal ASIC test signal



External test signal



ADC counts histograms
at 30, 55, 66, 122 and 105 ASIC #1 channels

Power supply

Low voltage

4x 

Has slow control soft
0-6.5 V output voltage
0-30 A output current

FUG Electronik NTN 350 – 6.5

High voltage

1x 

CAEN SY5527LC
4 Slot crate

3x 

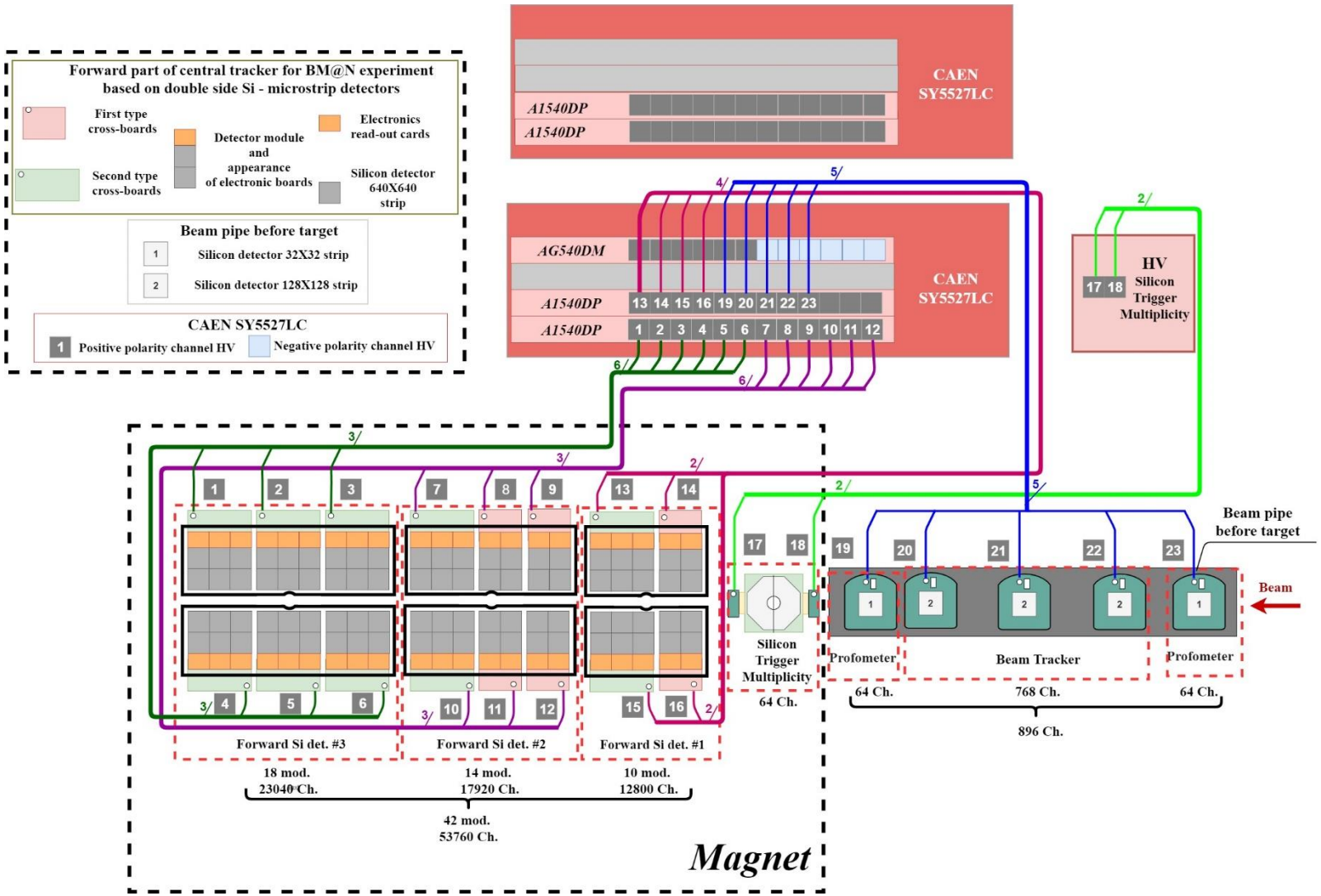
CAEN A1540DP

Slow control soft
12 channels
0-100 V output voltage (+ polarity)
1 mA current full scale
1nA monitor resolution
1mV Voltage Monitor resolution

Cross boards (are being designed now)

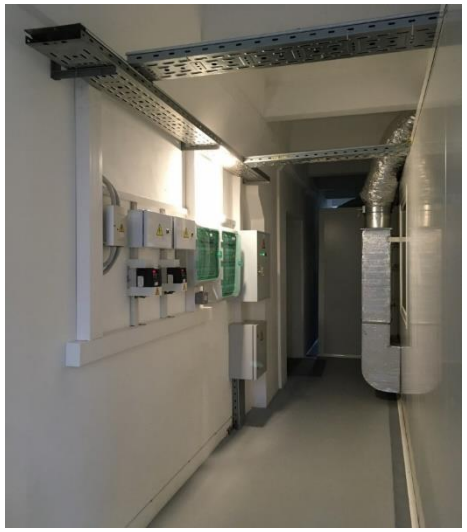
Silicon Detector Module

HV power supply



Assembling clean room

Clean room control board



Entrance

Working area 42 m²
Clean room standard ISO7 (352,000 (≥0.5 μm) Max. Number of Particles Permitted/m³)

Forward Silicon Detectors status summary

- Si – detectors and PA-640 tested and ready to assembly;
- All 90 Silicon detectors assembled on support frames and wait assembling with FEE;
- Test stand for FSD FEE electronics are done;
- FEE boards assembling and testing in progress;
- First FSD module should be assembled and tested during Fall 2020;
- Test stand for FSD module (with 106Ru + cosmic) design in progress;
- All HV и LV modules are procured and delivered;
- Assembling clean room is done;
- Wire bonder Delvotec set-up and tested (with supplier representative);
- Forward Silicon Detectors mechanical supports design in progress.

Backup slides

Forward Silicon Detectors + GEMs configuration

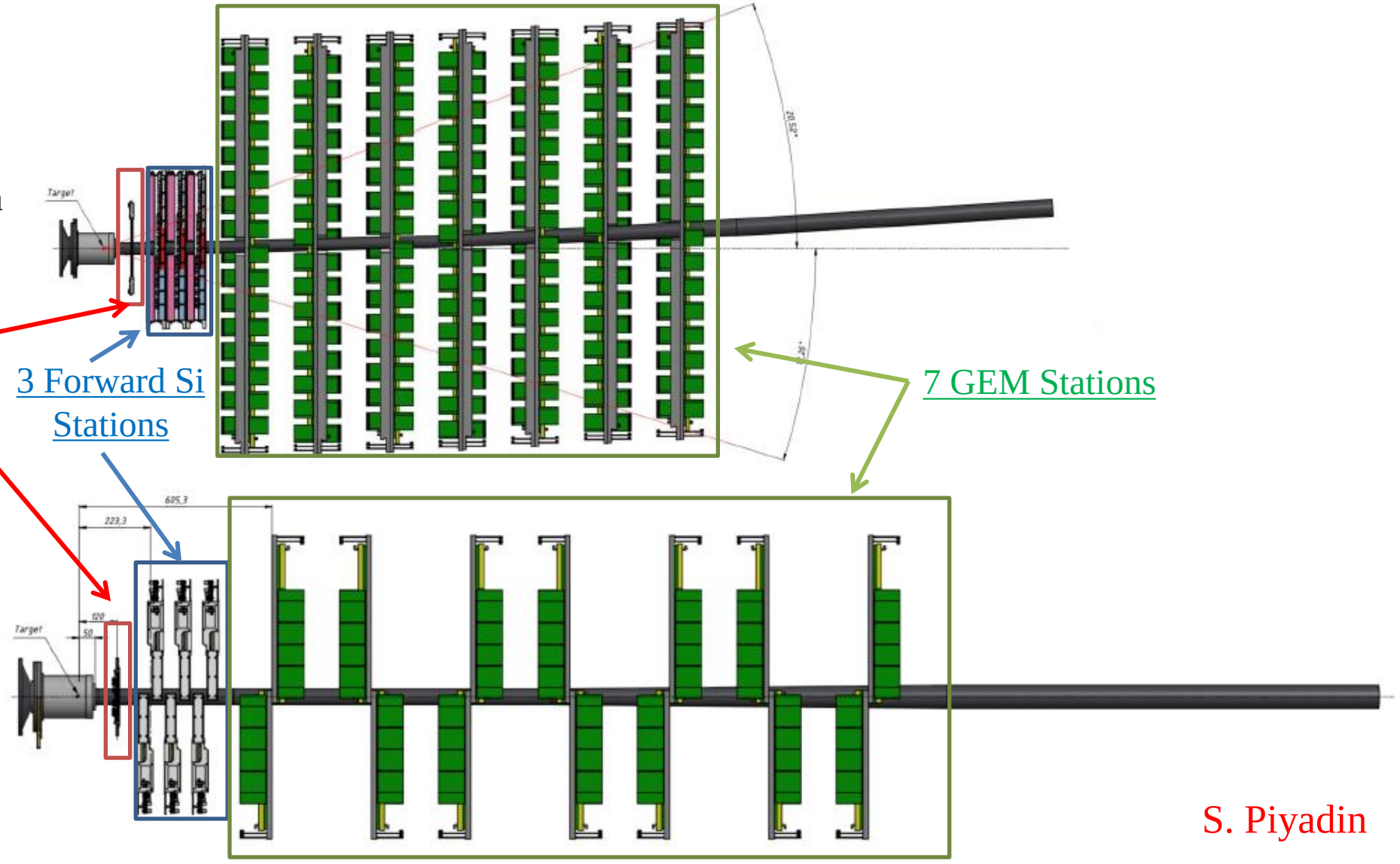
XZ – projection

Si multiplicity trigger

3 Forward Si Stations

7 GEM Stations

YZ – projection



S. Piyadin