



РОССИЙСКИЙ ФОНД ФУНДАМЕНТАЛЬНЫХ ИССЛЕДОВАНИЙ



BANGE OF NUCLEAR

# Progress in development of technology for series STS module assembly at JINR

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for the CBM-BM@N STS Collaboration



### Outline

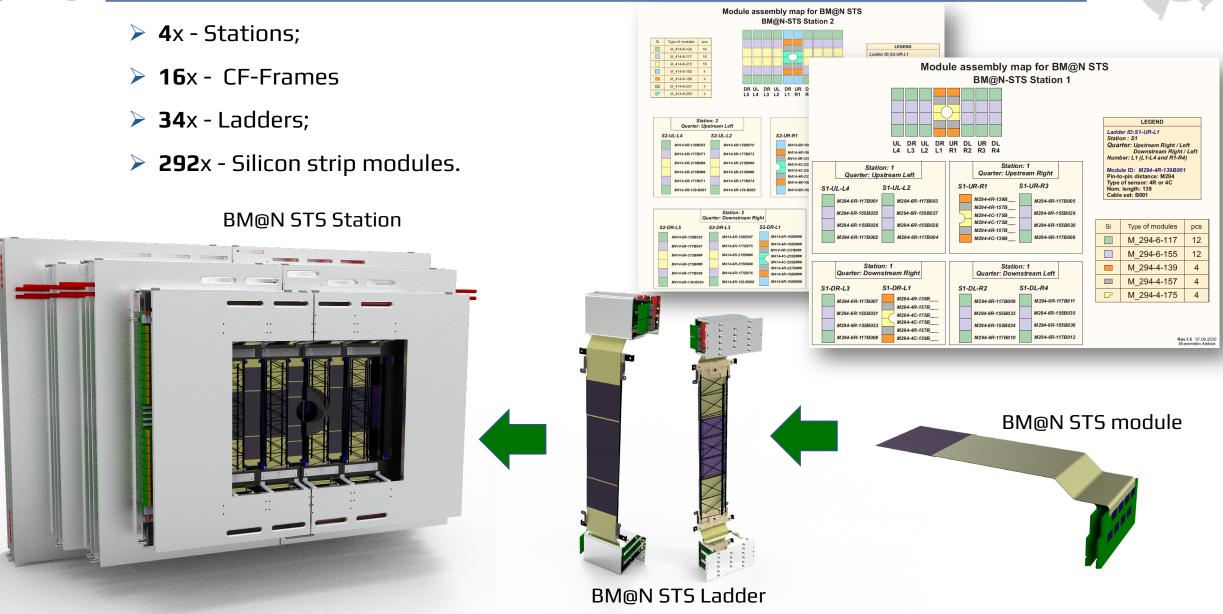


- Structure of BM@N STS Stations
- Module components for assembly
  - Silicon microstrip sensor
  - Flexible Capton-Aluminum cable
  - Front-end Board
  - Readout chip and LDO
- Cross section of module
- Technological processes of assembling modules for the BM@N STS
  - Assembly of the ASIC with flexible AI microcables
  - Assembly of the Si- sensor with flexible AI microcables
  - QA of assembly process
  - Wire bonding process ASIC and LDO to PCB
- Test of STS module
- Conclusions



## **BM@N STS Stations**

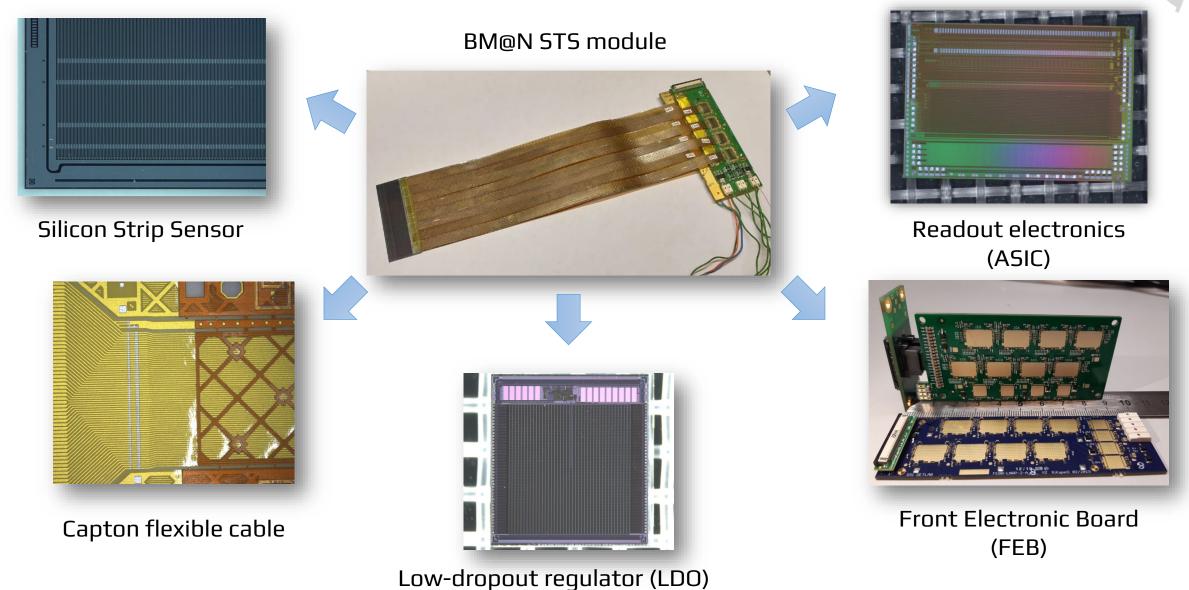
BRM @N





# Module components for assembly

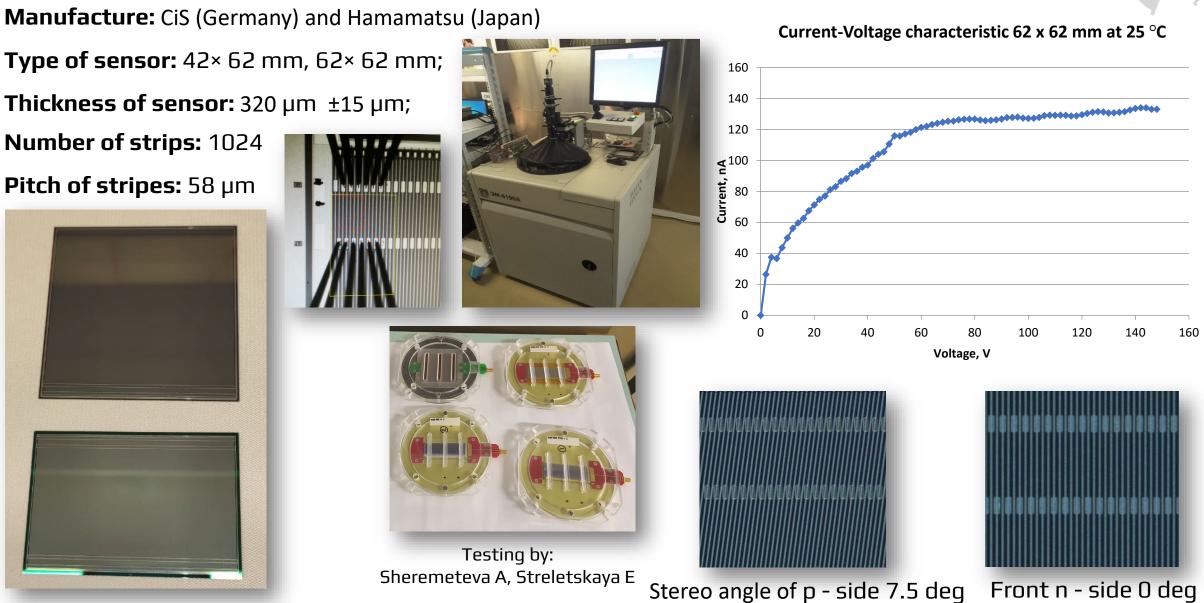






### Silicon microstrip sensor







# Flexible Capton-Aluminum cable



Number of signal traces - 64;

Width of trace in long work area - 30 um;

Pitch of trace of long work area - 112 um;

Width of trace in bond area - 45 um;

Pitch of trace in bond area - 116 um;

Width of windows of bond area - 165 um

Trace capacitance - 0.45 pF/cm

Trace lengths 11 - 30 cm



One set of components for assembly module





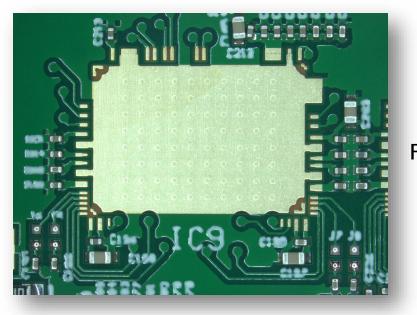
# **Front-end Board**



- Manufacture by Maraphon Ltd.
- Size of the PCB:  $87 \times 40$  mm;
- Thickness with components: 3 mm;
- 1 Uplink 80 Mb/s per one ASIC
- 1x Downlink 40 Mb/s
- 1x Clock 40 MHz

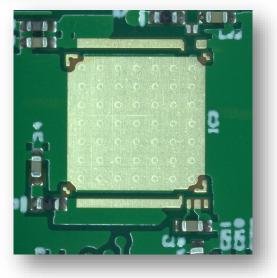


#### BM@N STS FEB with 8 ASIC



Footprint of ASIC

Footprint of LDO



LXX International conference "NUCLEUS – 2020. Nuclear physics and elementary particle physics. Nuclear physics technologies" 13.10.2020

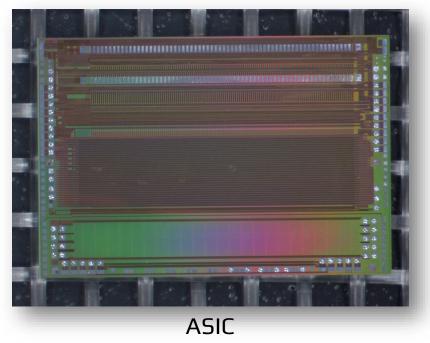


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# Readout chip ASIC v2.1 and LDO v.1



- 128 readout channels
- Flash ADC: 5 bit
- Data driven mode of operation
- Clock frequency 40 MHz
- Pitch of analog pads: 116 µm



Manufacture: Semiconductor Laboratory

V<sub>in</sub>: 2.4 – 3.3 V

 $V_{\text{out}}$ : 1.8 V and 1.2 V

Size of chip: 5415  $\times$  5775  $\mu m.$ 

Thickness 600 µm.

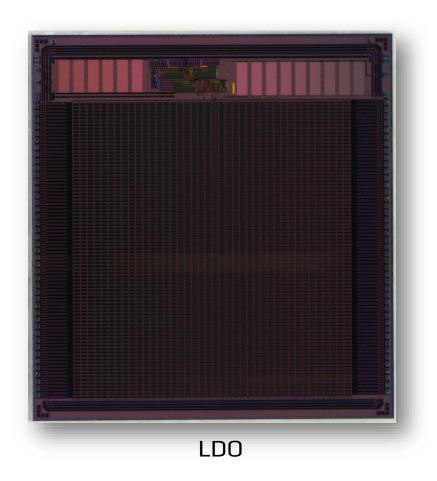
Size of bond pads: 50  $\times$  50  $\mu m$ 

Pads: 45 input power pads;

44 output power pads;

5 control pads;

4 GND pads.



BM



### **Cross section of module**



#### **Module material**

**Cable:** TDA-24 (Aluminum 14 μm + Capton 10 μm) **Pi-mesh of cable:** Capton 75 μm **Pi-mesh of shielding:** Foamtak II 165 μm



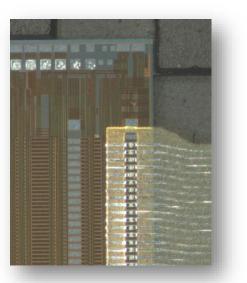


## Assembly of the ASIC with flexible AI - microcables

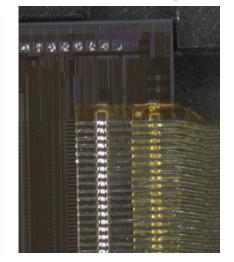




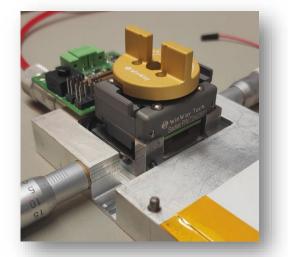
Ultrasonic assembly process on TAB-bonding machine



TAB - Bonding result of 1-st row of contacts Encapsulation of 1-st row of contacts



TAB - Bonding result of 2nd row of contacts





Aleksei Sheremetiev



### **QA of assembly process**

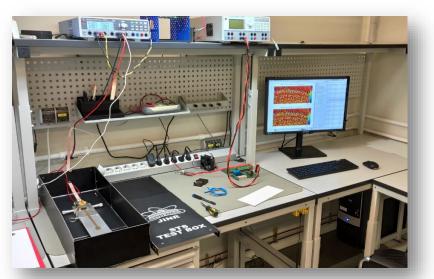


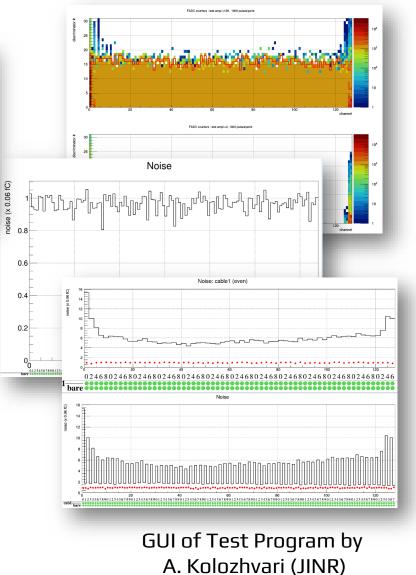


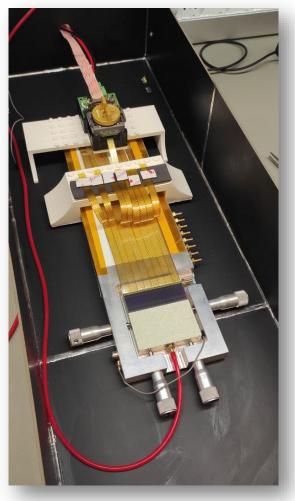
AFCK board v.1.1 and FMC board



Winway socket PogoPin device (GSI)





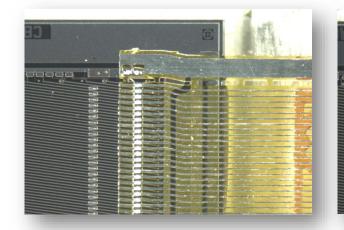


Bonding QA tests of 1<sup>st</sup> row on sensor



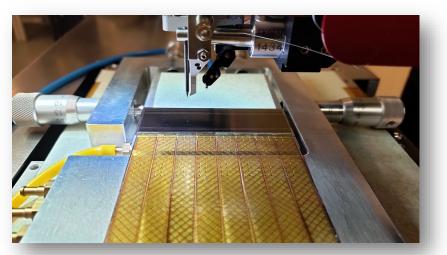
# Assembly of the Si- sensor with flexible AI - microcables BM@N



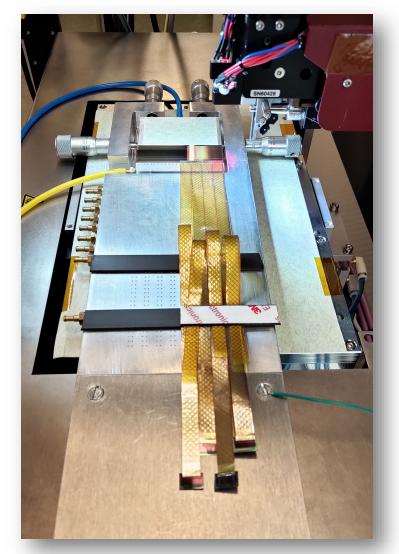


Bonding result of 1<sup>st</sup> row of contacts on sensor

Bonding result of two rows of contacts on sensor



The result of bonding 1<sup>st</sup> row cables on Si -sensor



Jig of bonding 1<sup>st</sup> row cables on Si -sensor

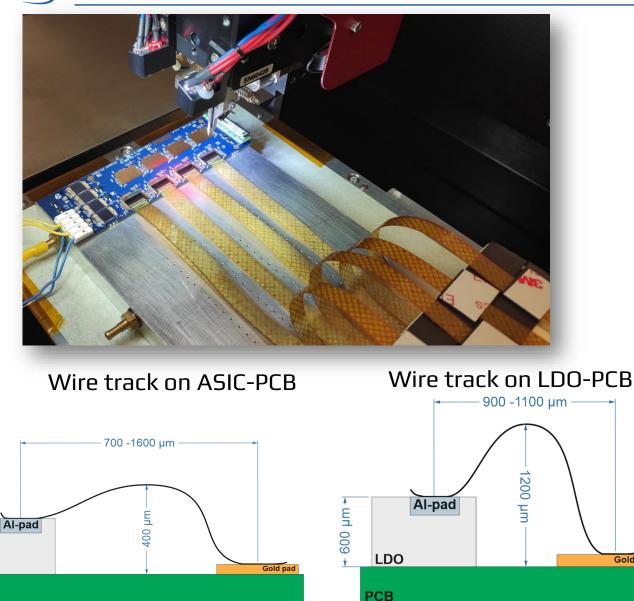


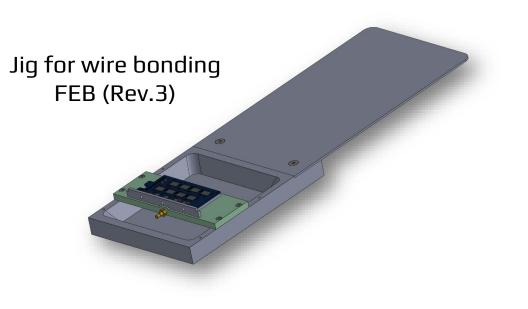
200 µm

ASIC

### Wire bonding process ASIC and LDO to PCB







- Two types of wire bonding process; ٠
- 25 μm Aluminum wire; ٠
- Special ultrasonic needle with small ٠ pitch;

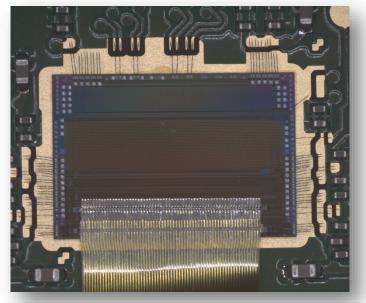
Gold pad



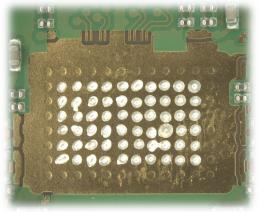
# Wire bonding process ASIC and LDO to PCB



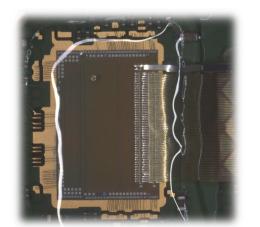
#### Wire bonding process of ASIC



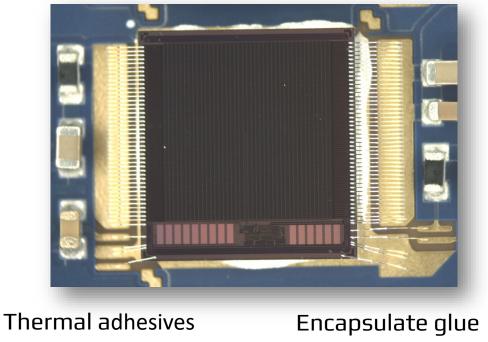
Thermal adhesives

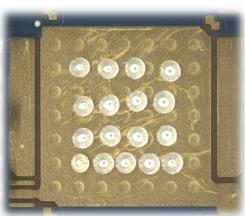


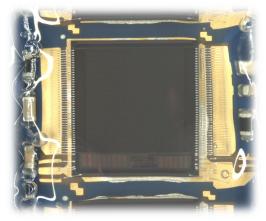




#### Wire bonding process of LDO



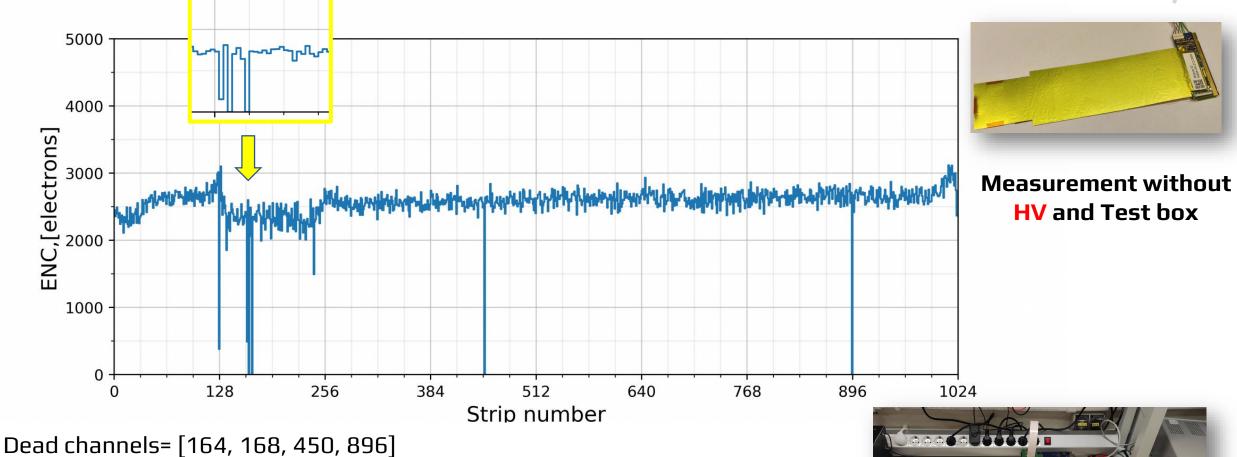






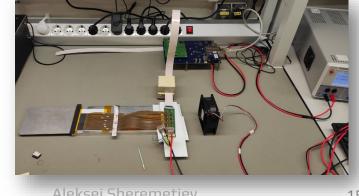
### **Electrical test of half-module**





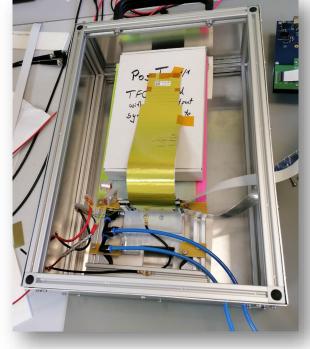
Not bonding channels = [128, 162, 235]

Not working channels on N-side of sensor: 7 Ch. [0.7%] Test by: D. Dementev, M. Shitenkow,





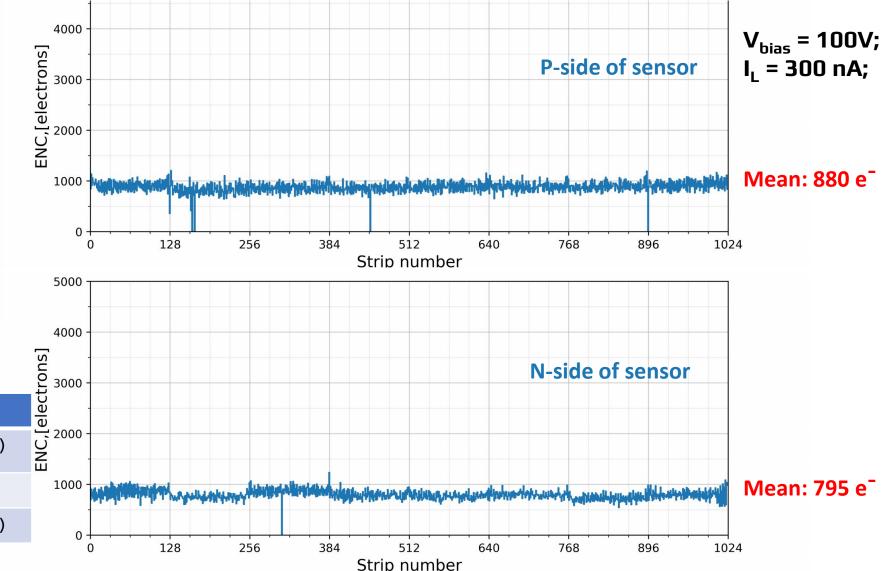
#### Test of STS module



# Result of dead channels at assembled modules

			_ <del></del>
Module	N-side	P-side	elec
M294-6R-212-D001	40 (4%)	23 (2,3%)	ENC,[
M294-2R-212-D003	5 (0.5%)	10 (1%)	
M294-2R-212-D004	7 (0.7%)	11 (1.1%)	

#### Test by: D. Dementev, M. Shitenkow.



6<sup>th</sup> Collaboration Meeting of the BM@N Experiment at the NICA Facility 26.10.2020

BM@N





- Assembly workflow has been developed and tested
- Workplaces and test benches for key technological operations has been prepared
- Set of bonding tools for assembly was designed and manufactured
- OA procedures for all components and steps of the assembly has been developed
- Technological documentation and Electronic logbook customize design has been

development to store ELOG data during assembly modules

• Five modules have been assembled at JINR lab, still more components for assembly of

20 modules are required to estimate production yields for mass production

# Thank you for attention!

