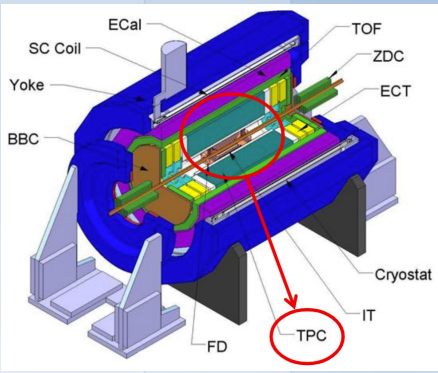


Status of the activity on development of Data Concentrator Chip

Eduard ATKIN, evatkin@mephi.ru
on behalf of ASIC lab at NRNU MEPhI

D. Azarov, P. Ivanov, D. Normanov,
V. Samsonov, A. Serazetdinov, V. Shumikhin

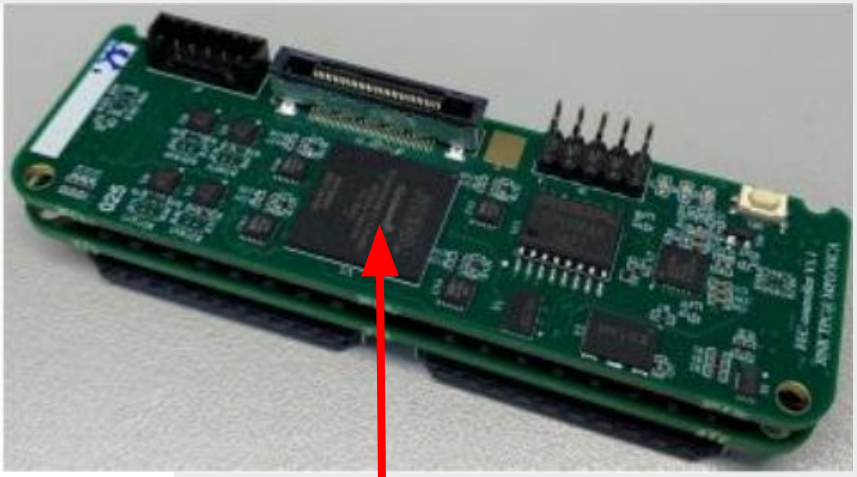
VI-th Collaboration Meeting of the MPD Experiment
October 28, 2020

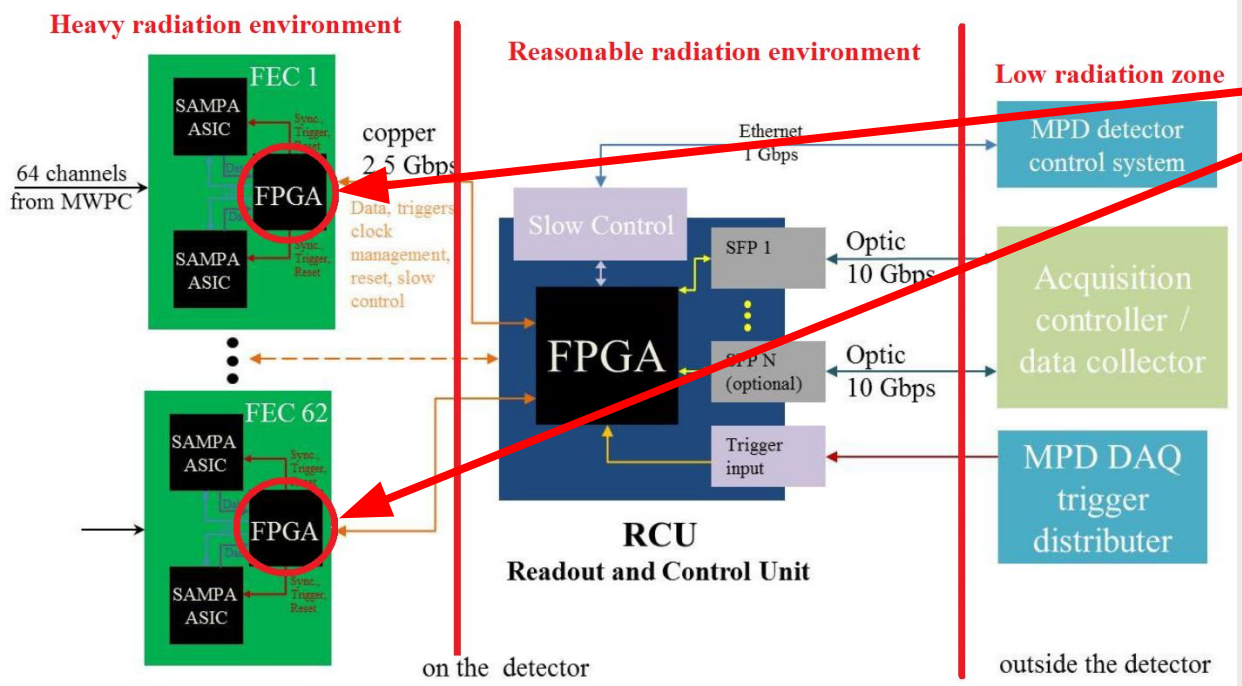
Outline

- Starting point
- Chip designation & environment
- Design routes
- Specifications
- Features & building blocks
- ASIC block diagram
- External interfaces and protocols
- Process & Layout & Pinout & Bonding
- Radiation tolerance issue
- Further plans & conclusions

TPC FEE* as a starting point

2 PCBs
28*91 mm^2

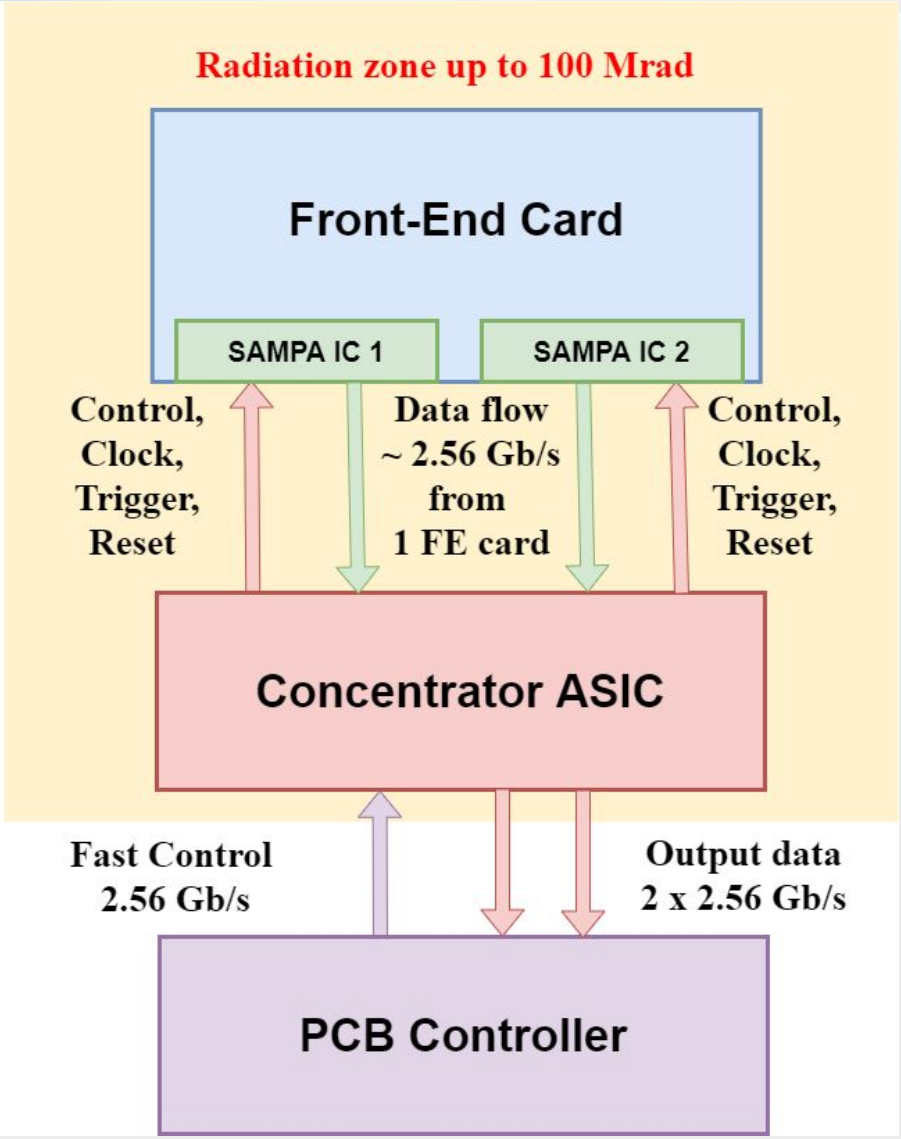




Non-radiation tolerant FPGAs to be replaced by rad-tolerant ASIC

* – A. Averyanov et al MPD TPC status, 2020 JINST 15 C07017
– S. Vereschagin et al Time-projection chamber for Multi-Purpose Detector, 2020 NIMA vol. 958, 162793

The prototype chip features



- almost double redundancy for data flow: 2.56 Gb/s one totally at SAMPA outputs goes via two CML interfaces at the same speed each
- radiation tolerance fits the most heavy radiation zone
- compensation of the used cable losses as well as PCB and package parasitics
- programmable built-in chip 50 Ohm matching for cables

Why does the concentrator ASIC necessary for TPC FEE?

- The TPC setup contains about 10^5 detector channels, based on SAMPA chips, ended by high-speed (~10 Mb/s) high-resolution (10 bit) ADCs, generates a large **amount of** digital **data** and thus require a high integration, based on ASIC technology
- Data should proceed via a synchronized deserialization, sequencing, noise-free and fault-free encoding, output serialization
- Needs to use a very limited number but **high-speed links** both for data transfer out and control. All possible RF losses should be mitigated
- Needs to process the data on-detector in a non-friendly **radiation environment**
- Non-availability of COT components ready to use

Hub ASIC shortly

- **Transceiver** chip (called as “hub v.1”) for FEE communication to/from counting room
- 1 downlink + 2 uplinks, both working at **2.56 Gb/s** via electrical cables
- **Radiation tolerant** by design (up to 100 MRad)
- Functionality: detector data readout, triggers, clocks, control and calibration

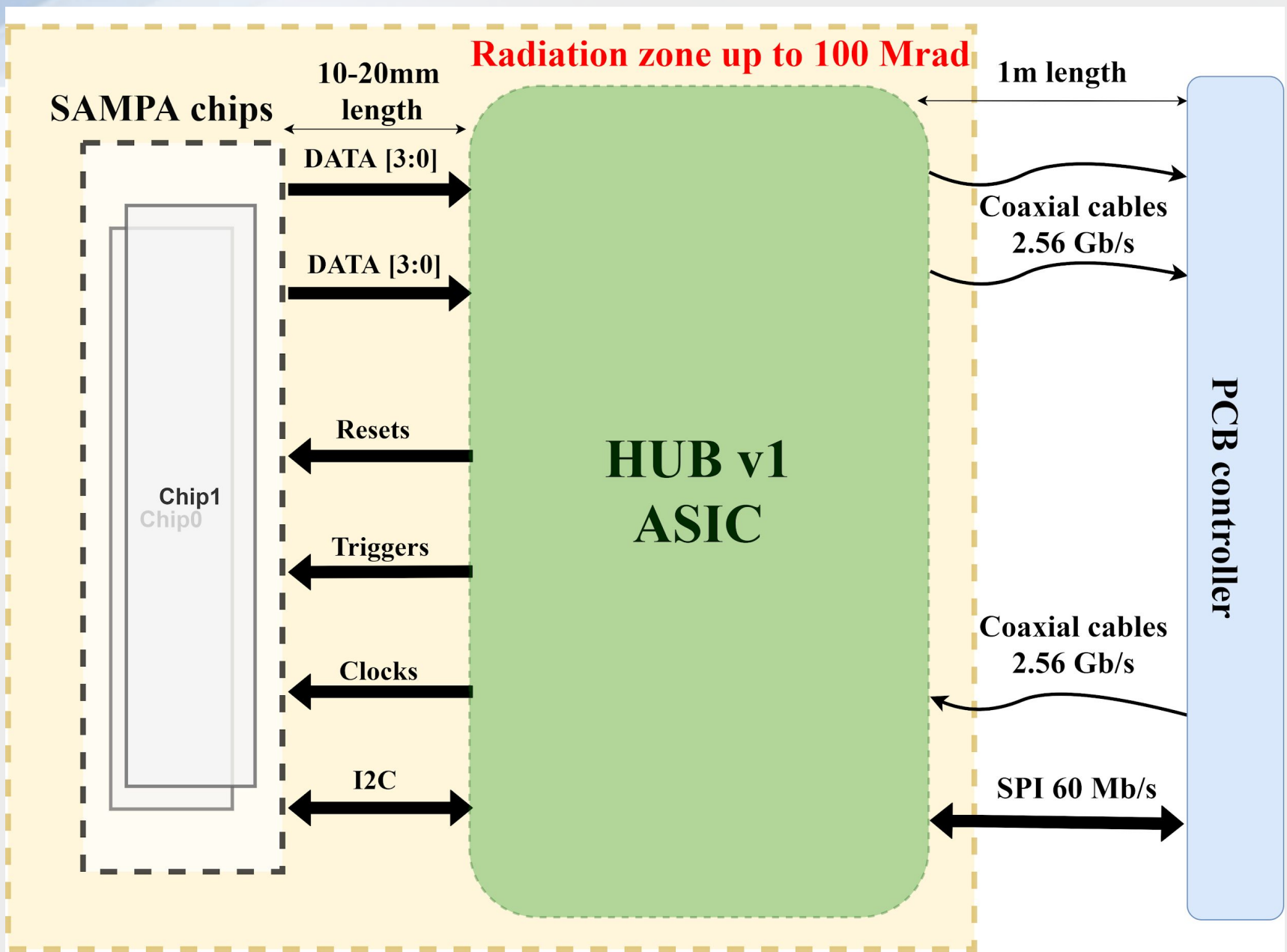
ASIC designation

- HUB v1 is a radiation tolerant prototype ASIC that can be used to implement multi purpose high speed bidirectional links for TPC FEE
- ASIC supports one or two 1m length 2.56 Gb/s links in the direction from detectors to the counting room (Uplink) and one 1m 2.56 Gb/s link in the direction from counting room to the detectors (Downlink)

Interfaces:

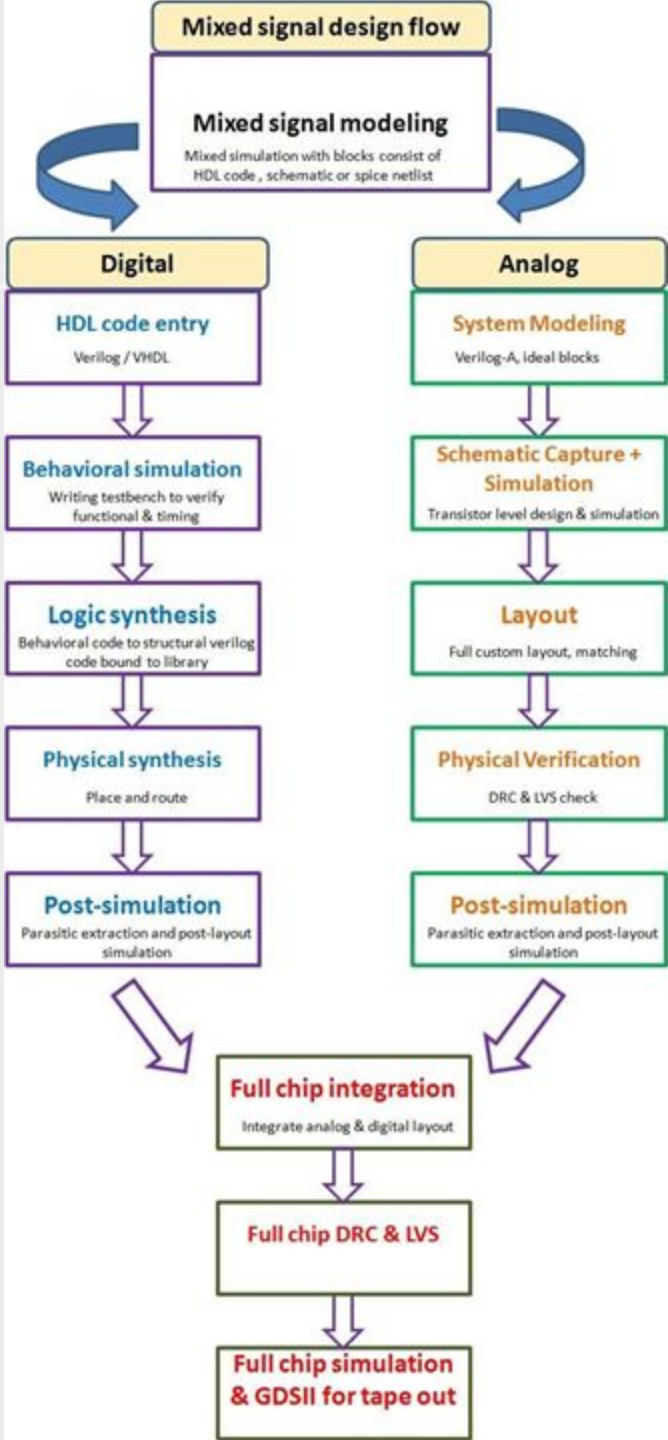
- 2x4 ports SAMPA data
- 2x ports SAMPA Reset
- 2x3 ports SAMPA Trigger
- 2x3 ports SAMPA Clock
- 2x CML Tx
- CML Rx
- SPI (slow control)
- I2C

Environment



Standard mixed-mode design route

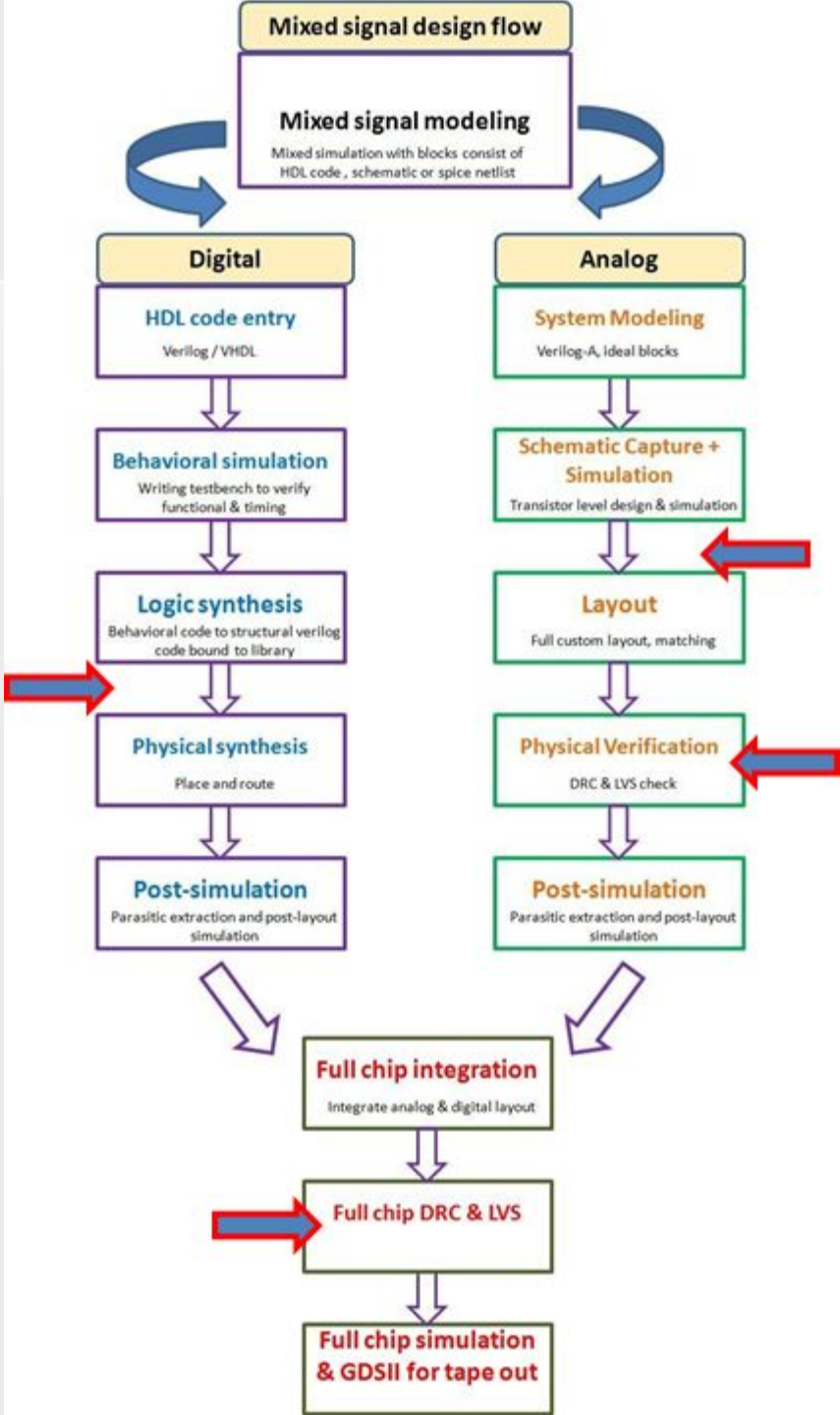
- Cadence CAD tools for start-to-finish design flow
- Top-to-bottom design
- TSMC DKs for the 65 nm process
- Powerful servers (DELL, INTEL) + client workstations
- Digital on top and mostly digital flow



Radiation tolerance aspects in design

Legend 

- Digital part uses: 12T standard cell library of TSMC 65 nm process and triplication logic
- Analog part uses different known tips and tricks to provide radiation hardness by:
  - process
  - design
  - schematics implementation



Specifications (1)

Specifications	Value
Technology node	65 nm
I/O voltage	2,5 V
CORE voltage	1,2 V
Temperature	0 - 85 °C
Power consumption	< 1 W
Radiation tolerance	< 100 Mrad
Serial interface with SAMPA	
Number of input channels	8 channel (16 pins)
Maximum input frequency	320 MHz
Physical level	SLVS

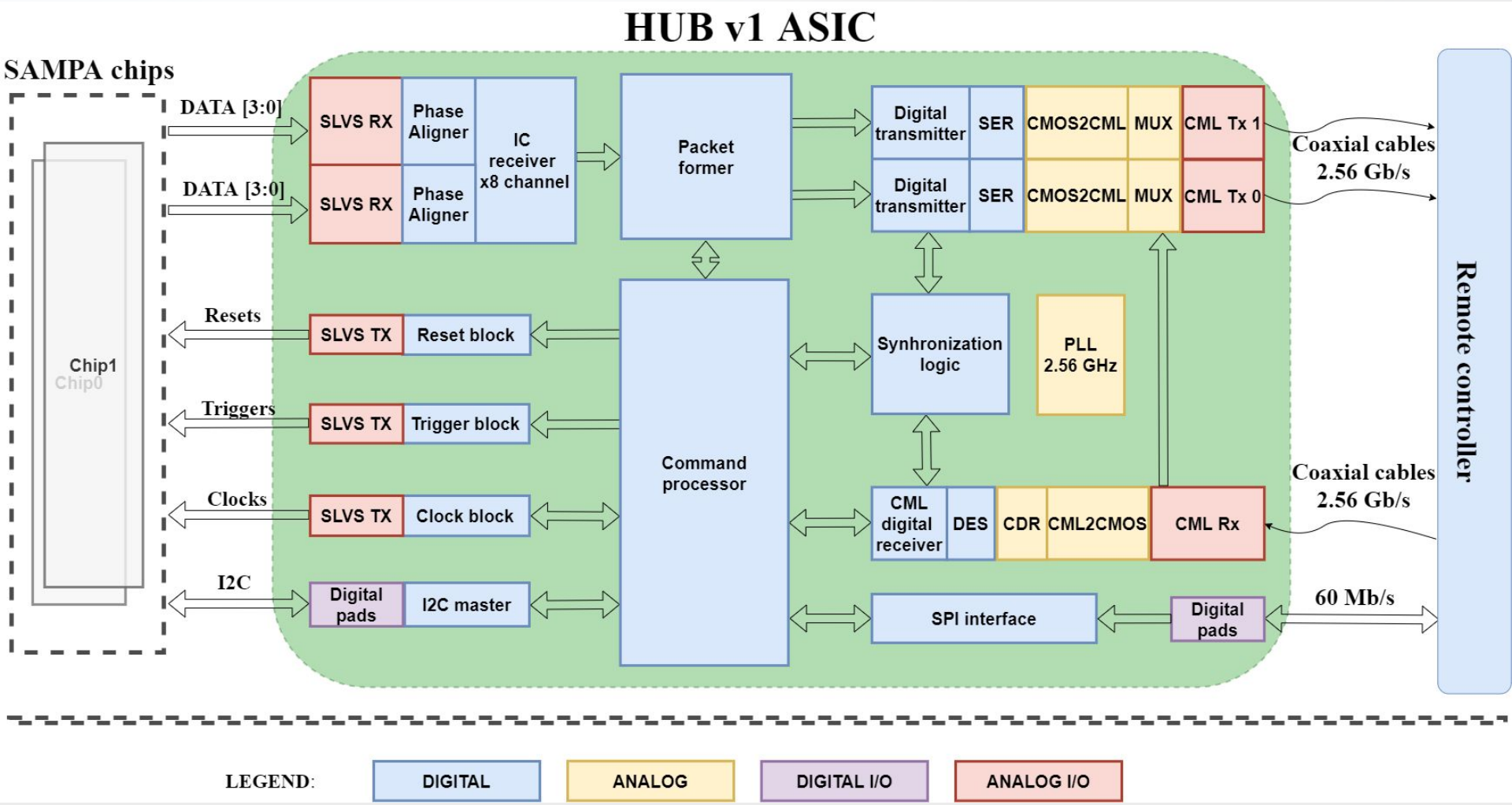
Specifications (2)

High speed Interface to counting room		
Number of channels	Input	1
	Outputs	2
Frequency	2.56 GHz	
Physical level	CML	
Transmission distance	< 1 meter	
I2C Interface		
Operating mode	10 bit addressing	
Frequency	100 kHz - 5 MHz	
Physical level	LVCMOS 1.2 V	
Synchronization Interface		
Number of channels	6 channel	
Frequencies	20/40/80/160/320 MHz	
Physical level	SLVS	

Specifications (3)

Output trigger links	
Number of links	6
Physical level	SLVS
Output reset links	
Number of links	2
Physical level	SLVS
Hardware address	
Number of links	4
Physical level	LVCMOS 1.2 V
External LDO control	
Number of links	2
Physical level	LVCMOS 1.2 V

Prototype ASIC block diagram



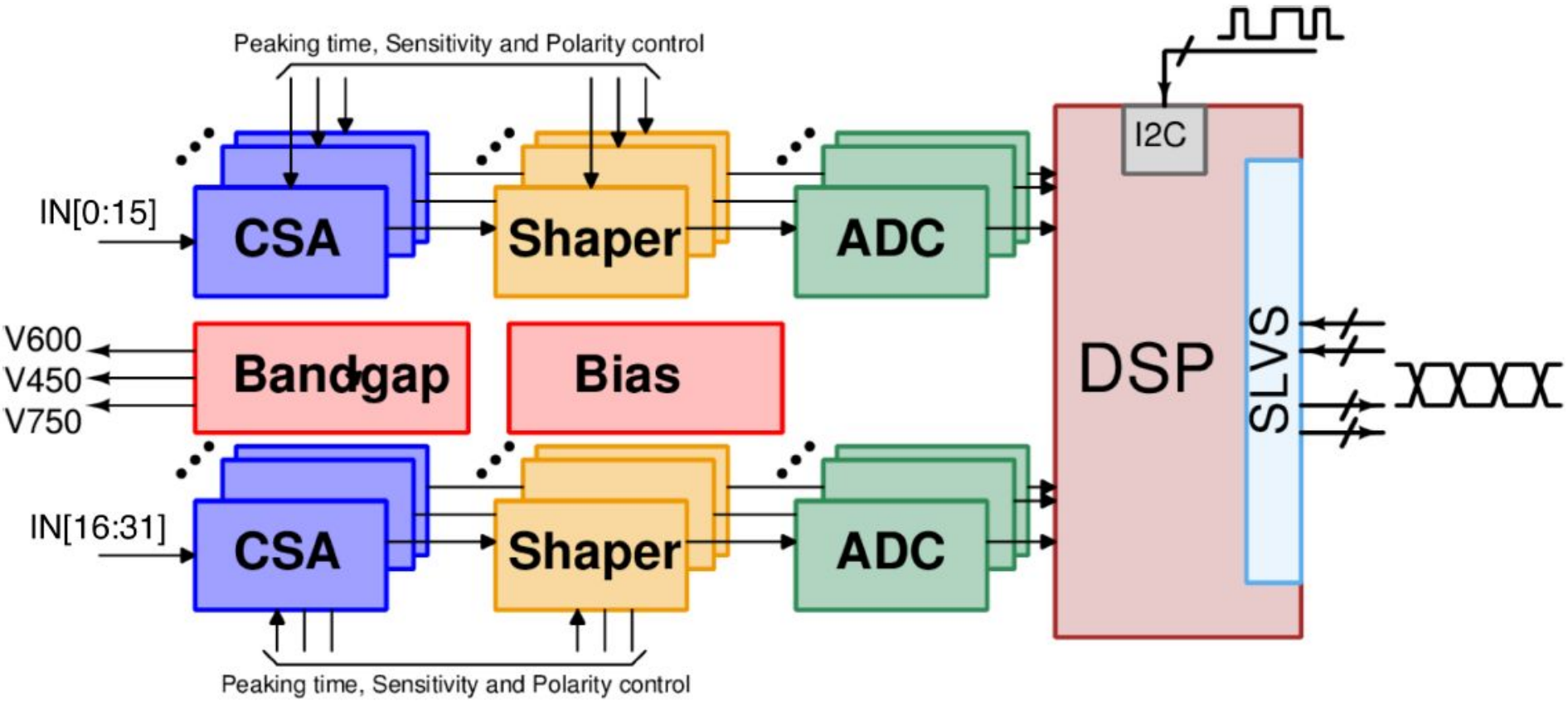
Mixed-mode (mostly digital (~70%)) design

Building blocks

Analog blocks	***Digital blocks***	
SLVS Rx	IC receiver channel	I2C master
SLVS Tx	Phase Aligner	DES
CML_RX	Packet former	Reset
CML_TX	Digital Transmitter	Trigger
PLL	SER	Clock
CDR	Synhronization Logic	
POR	SPI Interface	
CMOS2CML	Command processor	

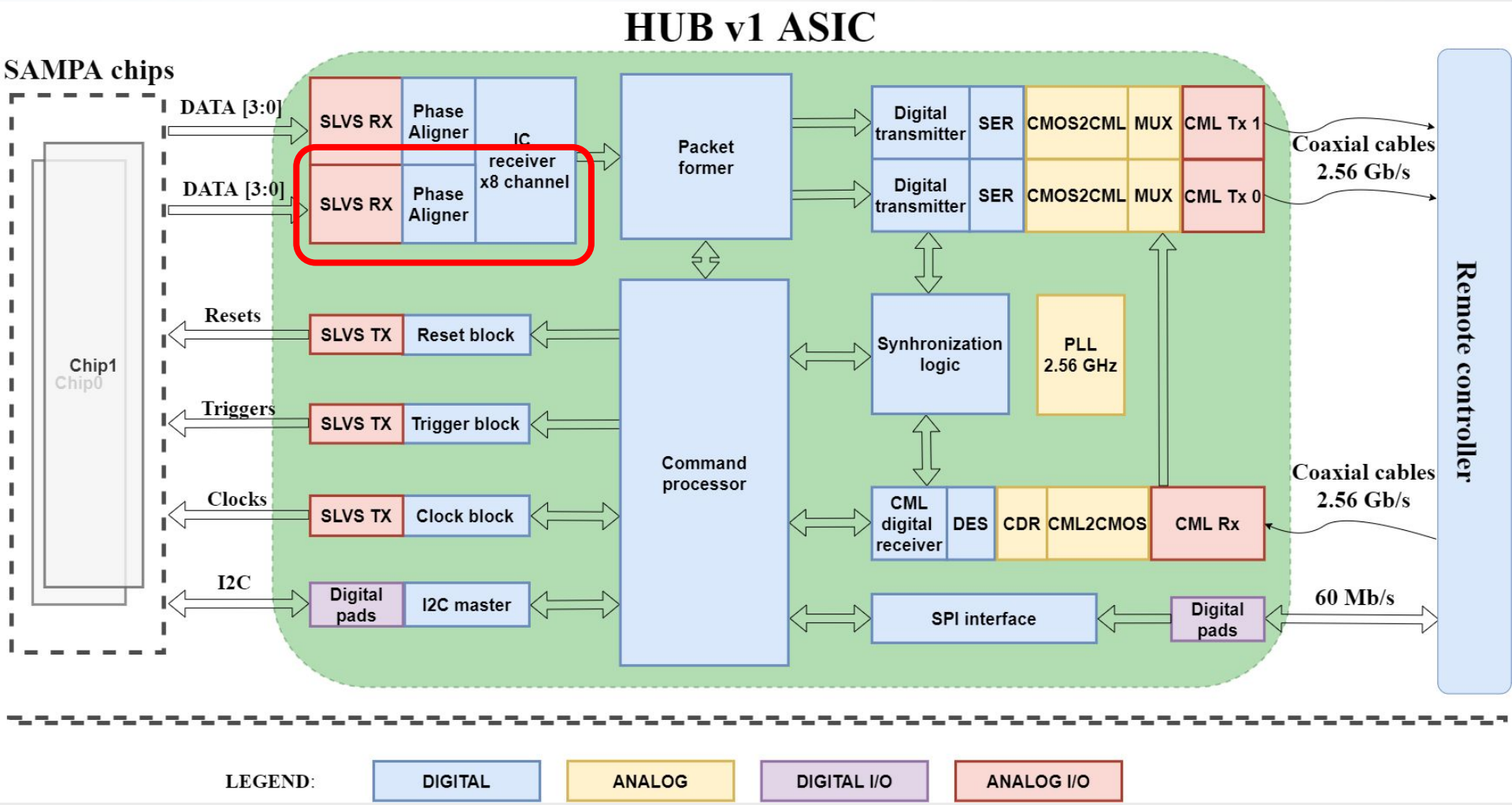
Getting data from SAMPA*

(SAMPA itself)



* – J. Adolfsson, et al. SAMPA chip: the new 32 channels ASIC for the ALICE TPC and MCH upgrades, 2017 JINST 12 (04) C04008

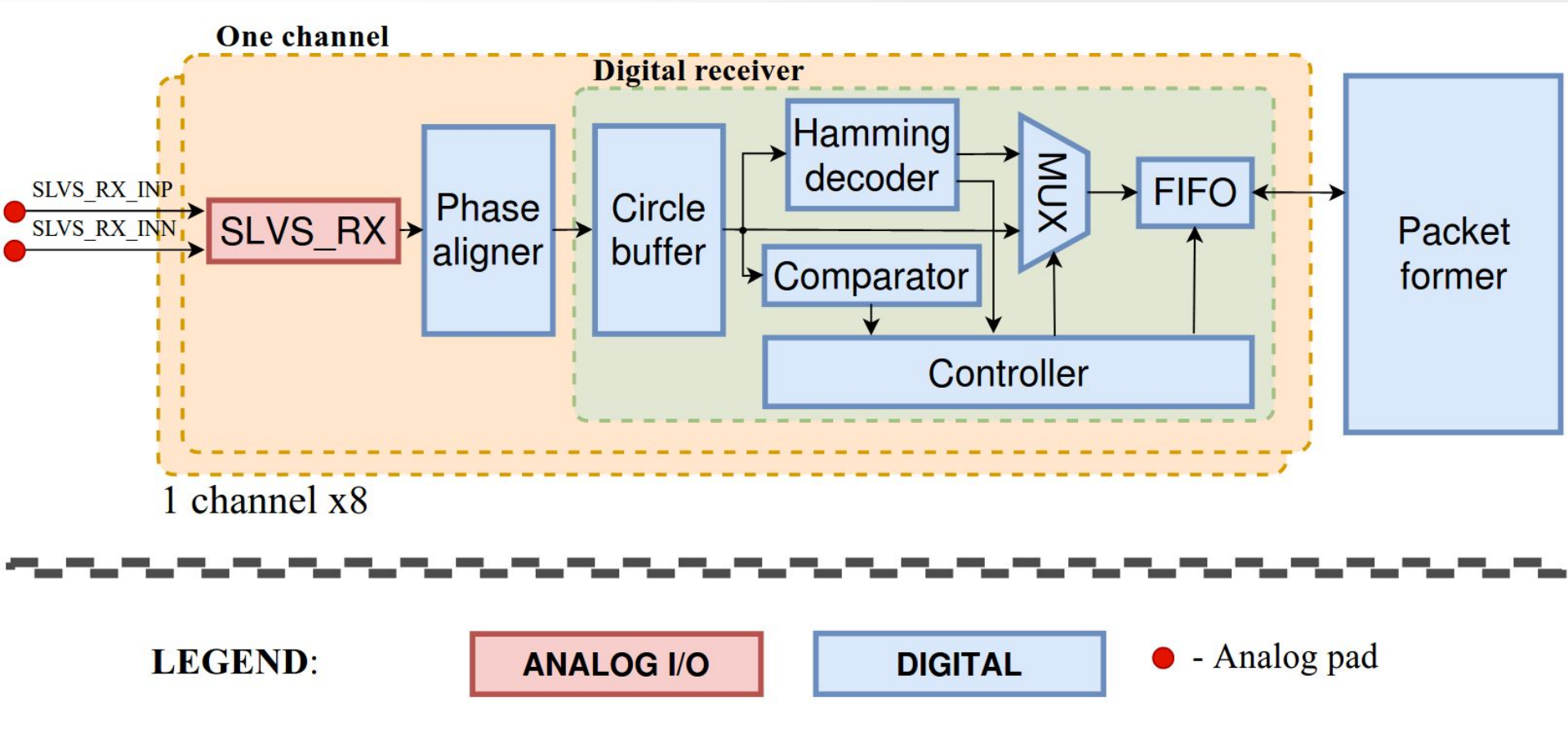
Getting data from SAMPA
(HUB Digital receiver block)



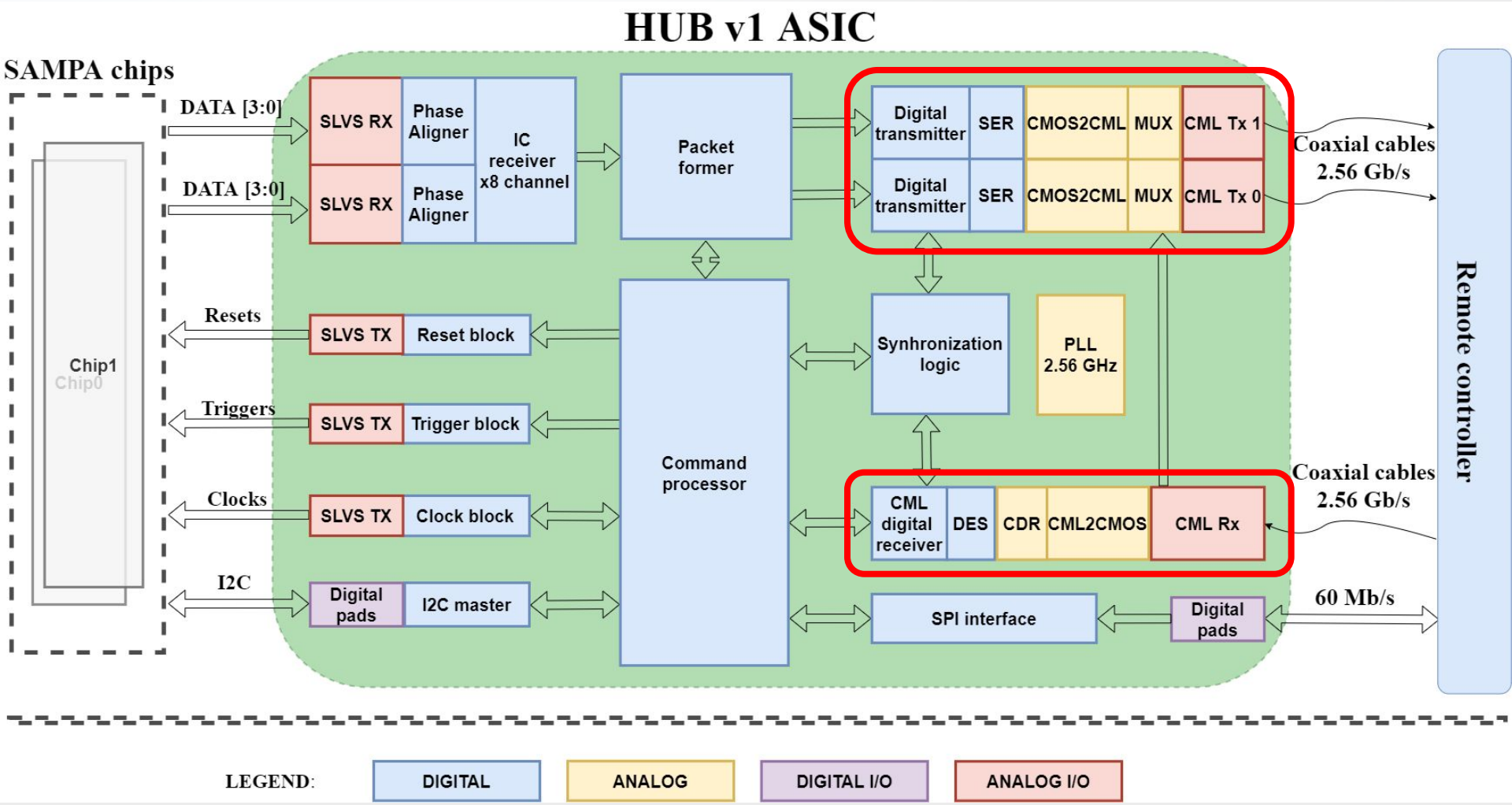
Mixed-mode (mostly digital (~70%)) design

Getting data from SAMPA

(Digital receiver structure)



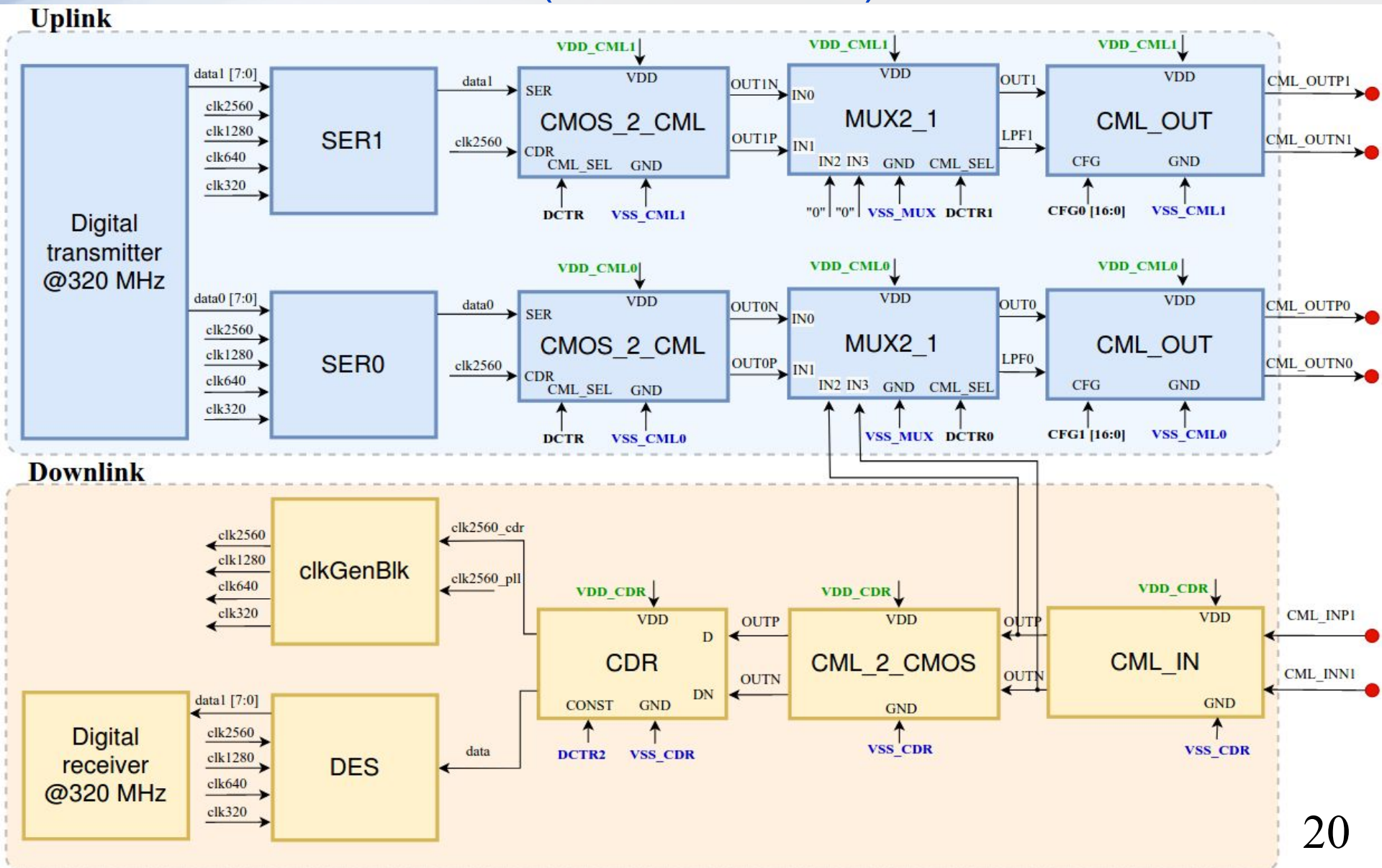
High speed interface to counting room



Mixed-mode (mostly digital (~70%)) design

High speed interface to counting room

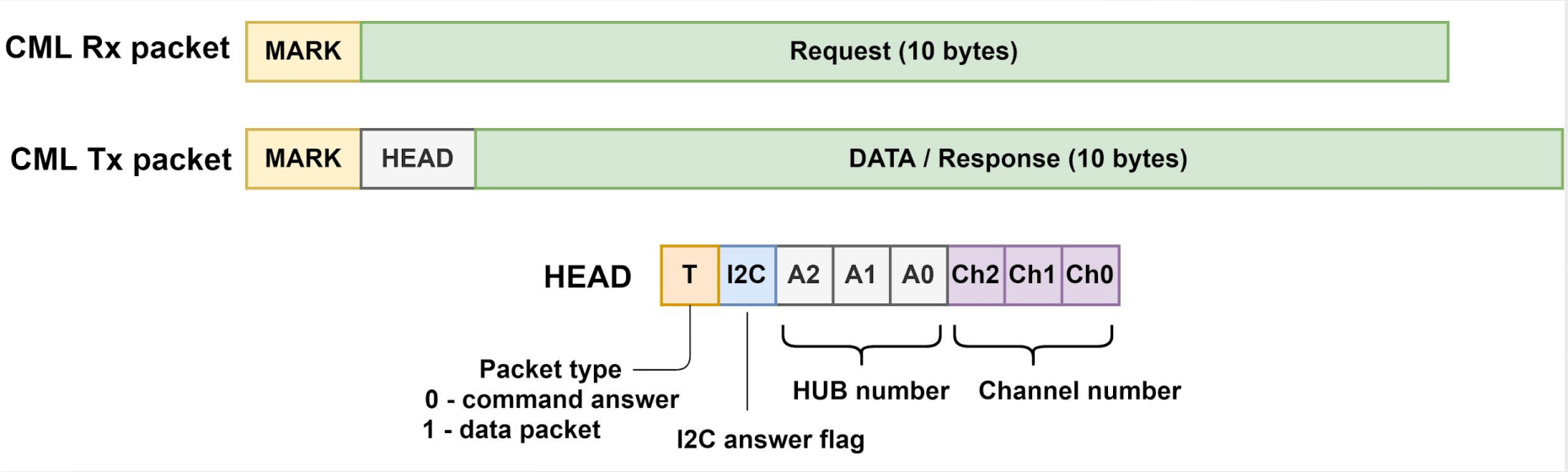
(Tx & Rx details)



High speed interface to counting room
(main CML interface features)

- CML data are encoded by 8b/10b
- CML Rx receives command request
- Supported modes are: one or two CML
- CML Tx 0 translates command response and SAMPA data (commands have higher priority than data)
- CML Tx 1 translates SAMPA data if CML Tx 0 is busy and two CML Tx are used

CML protocol
(Rx & Tx packets)



At T=0 packet contains command Response

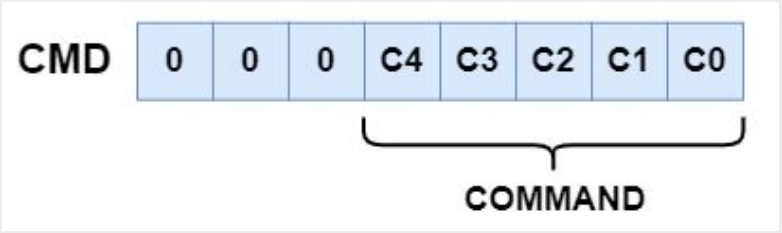
At T=1 packet contains 10 bytes DATA

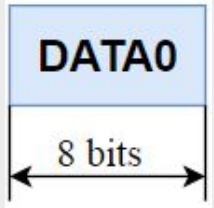
CML protocol
(format of commands)

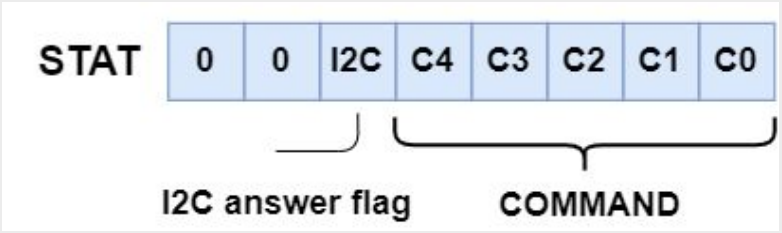
Request	CMD	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
Response	STAT	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Commands:

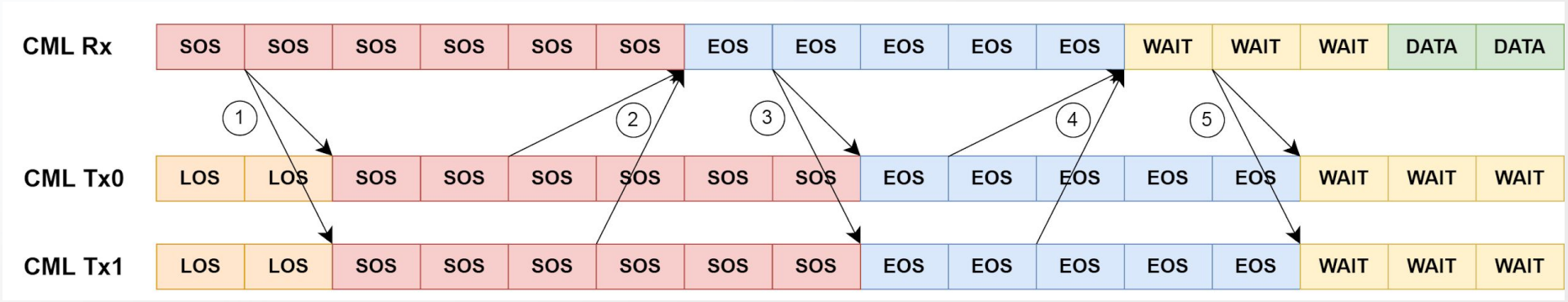
- Config load
- Config read
- ASIC Soft Reset
- SAMPA Trigger out
- SAMPA reset
- I2C read
- I2C write
- Debug commands







CML protocol
(synchronization procedure)



Steps:

1) ASIC starts of synchronization
2) Controller synchronize both channels
3) ASIC sends EOS
4) Controller finalize synchronization
5) ASIC finalize synchronization

CML modes:

- LOS (lost of sync) - K28.4
- SOS (start of sync) - K28.1
- EOS (end of sync) - K28.3
- WAIT - K28.5
- Data packet
- Command packet

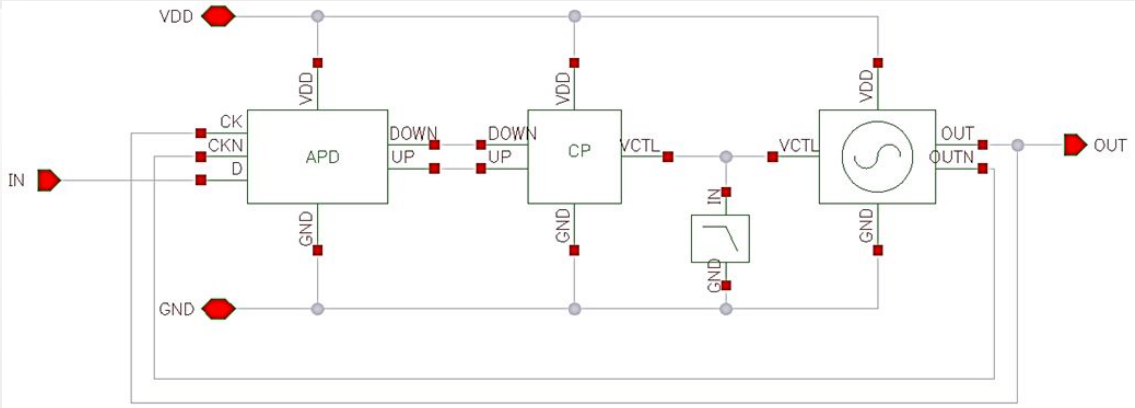
Building blocks

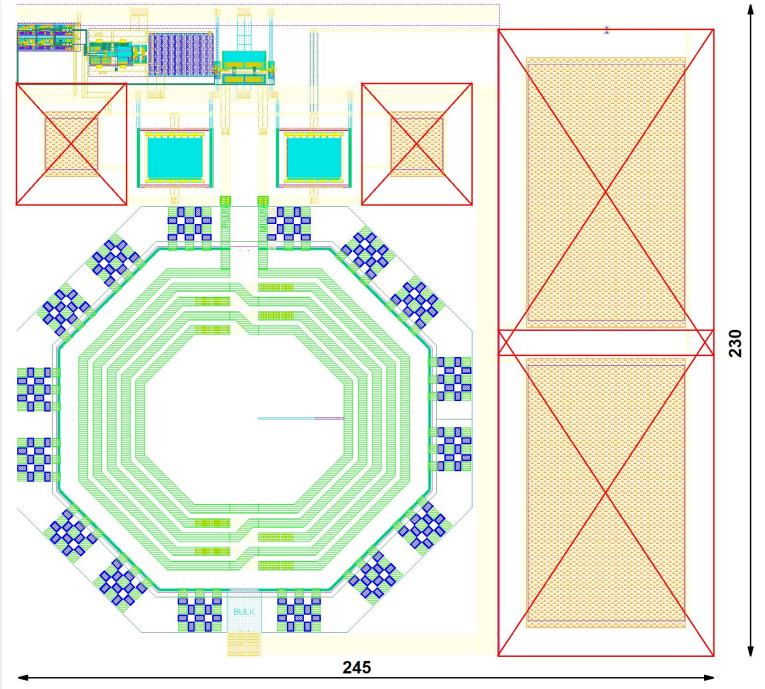
Analog blocks	***Digital blocks***	
SLVS Rx	IC receiver channel	I2C master
SLVS Tx	Phase Aligner	DES
CML_RX	Packet former	Reset
CML_TX	Digital Transmitter	Trigger
PLL	SER	Clock
CDR	Synhronization Logic	
POR	SPI Interface	
CMOS2CML	Command processor	

Clock Data Recovery

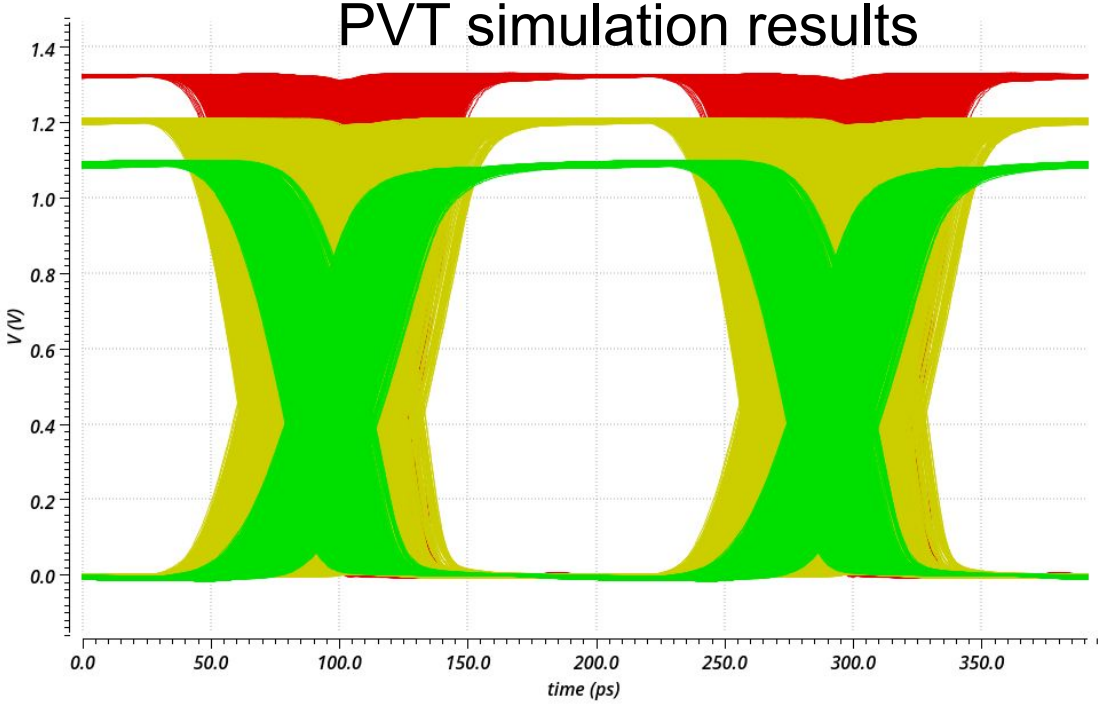
Alexander phase detector scheme

- frequency setting < 1 µs
- jitter about 70 ps
- duty cycle 48.5 %
- power consumption: 6 mW





PVT simulation results



Process & Layout block placement

Chip size: 2 x 2 mm

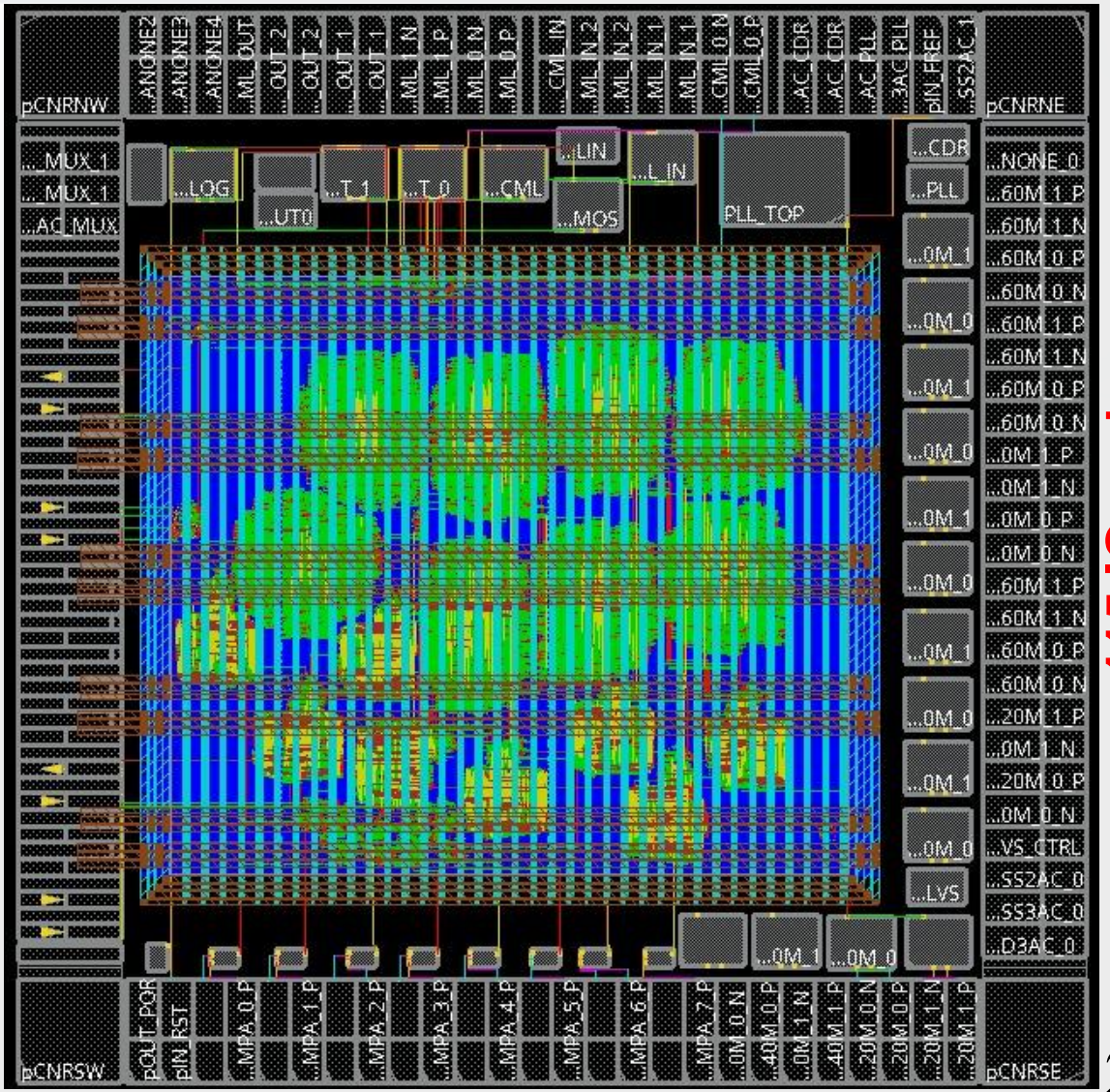
TSMC 65nm CMOS

Mixed-Signal/RF, Low Power

Core : 1.2 V, IO : 2.5 V

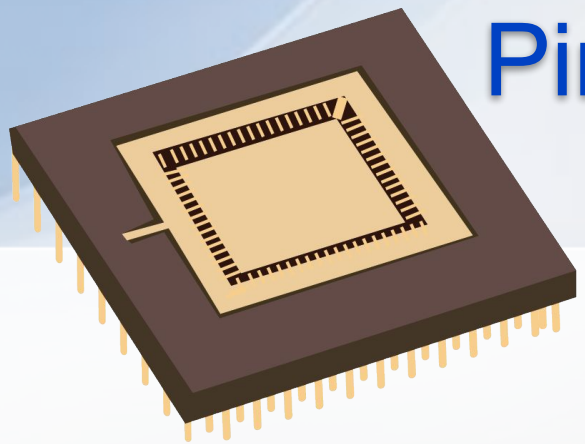
Metal scheme: 1P9M_6X1Z1U

12T standard cells for digital part



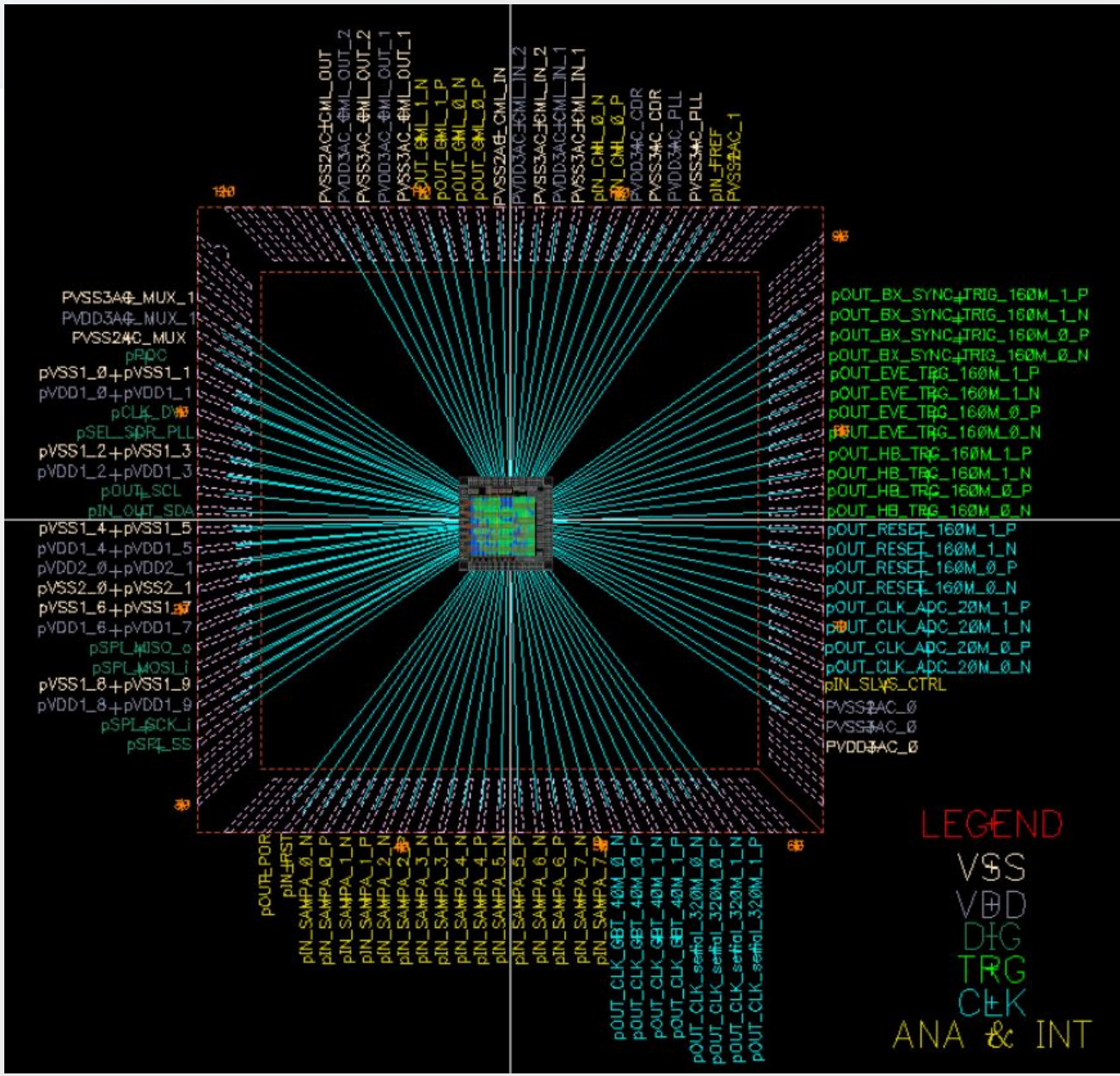
115 IO pads

Pinout & Bonding & Packaging



CPGA 120

Such a packaging produces parasitics, resulting in needs to perform accurate RF simulations



Transmission line attenuation

AlphaWire 9436

coax cable

Specifications (1 m)

Wave impedance – **50 ± 5 Ω**

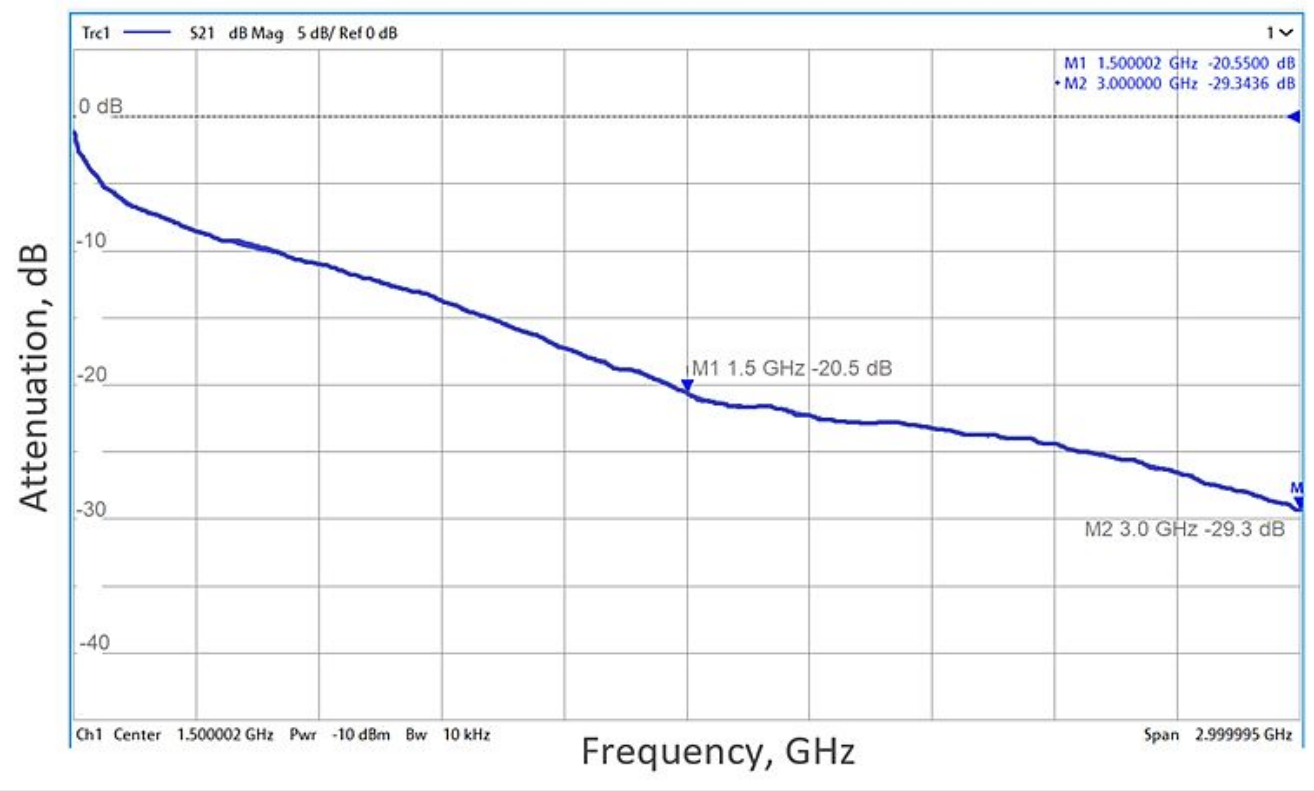
Insulator – **PFA**

Dissipation factor – **0.0008 @ 1 GHz**

Dielectric constant – **2.11**

DCR – **1.57 Ω/m**

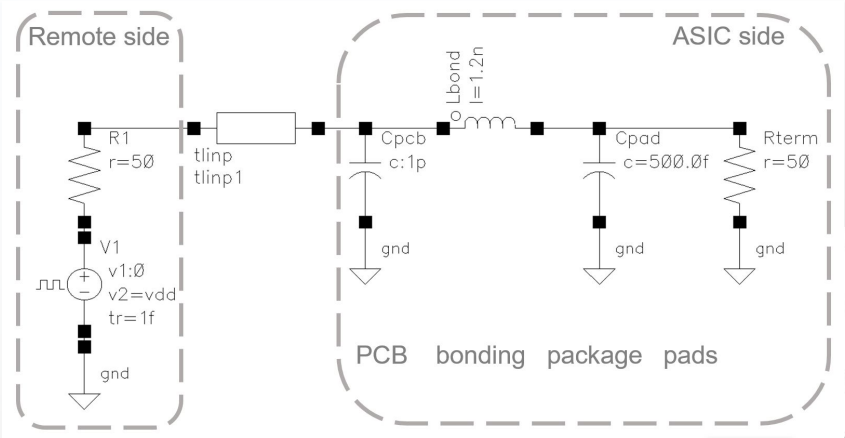
Attenuation, dB/m – **-0.25 @ 10 MHz**



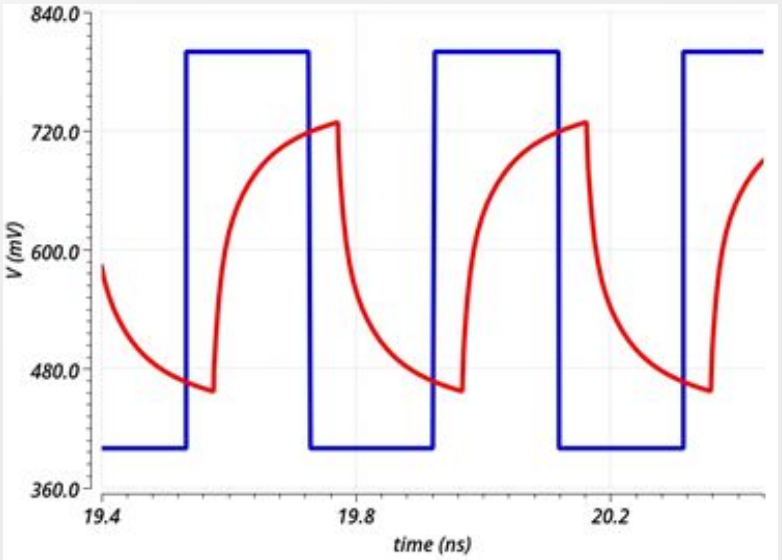
Attenuation of 5 m AWG36 cable,
measured by TPC team (JINR) on 20.10.2020

Transmission line model

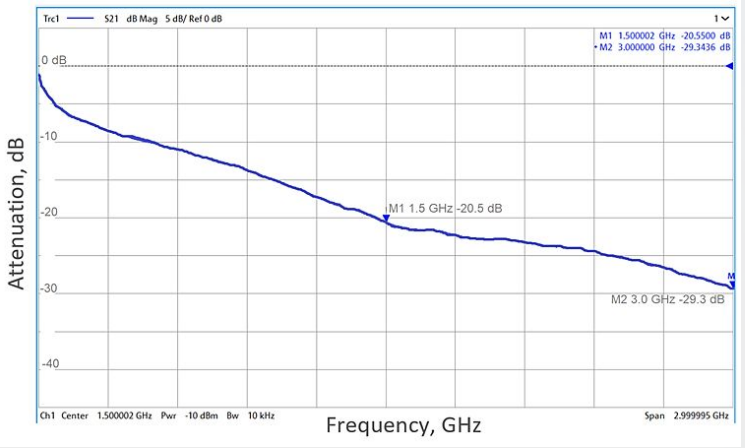
(measurement versus simulation)



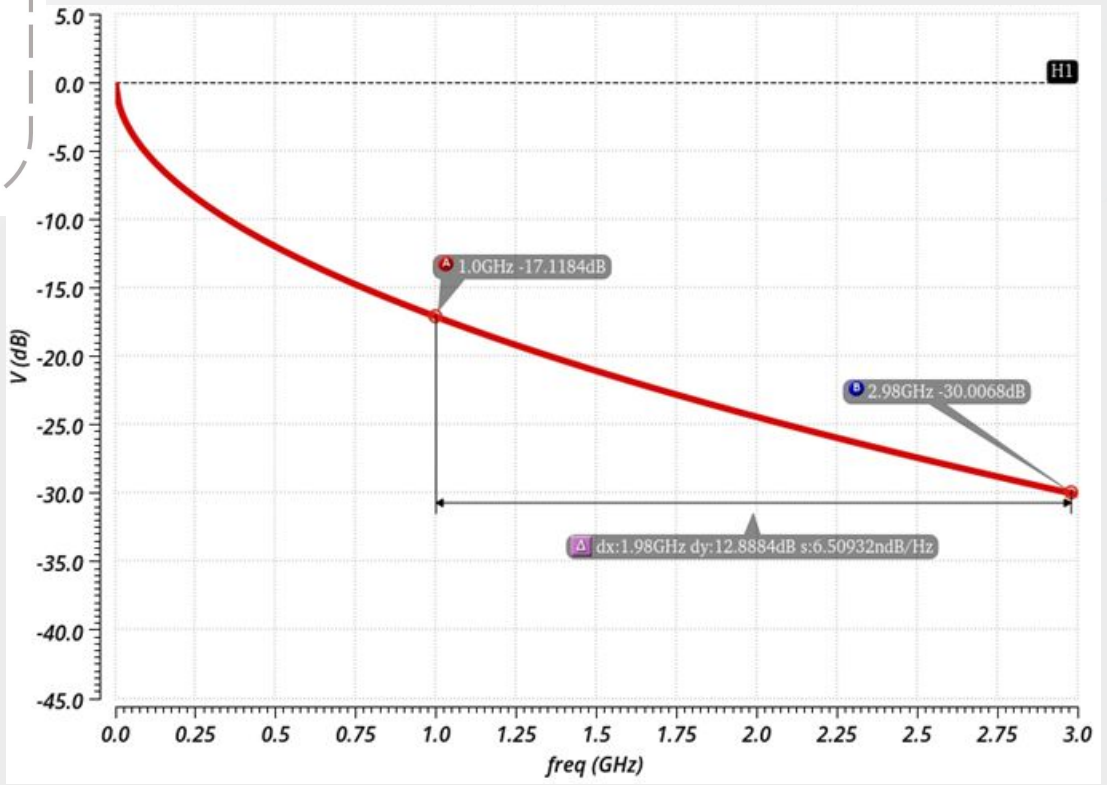
CML interface parasitics (LPF)



1 m cable losses at 2.56 Gb/s



5m cable attenuation vs frequency (measurement)



5m cable attenuation vs frequency (simulation)

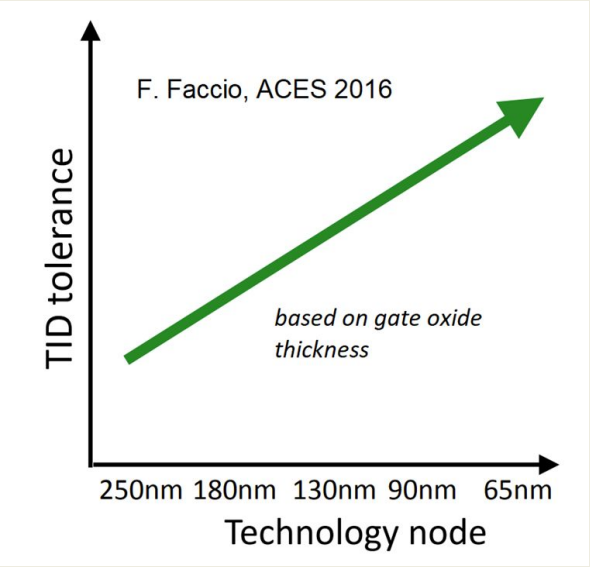
Radiation tolerance by ...

*(used tips and tricks)**

Process

- valuable trade-offs on performance and radiation tolerance at a reasonable cost

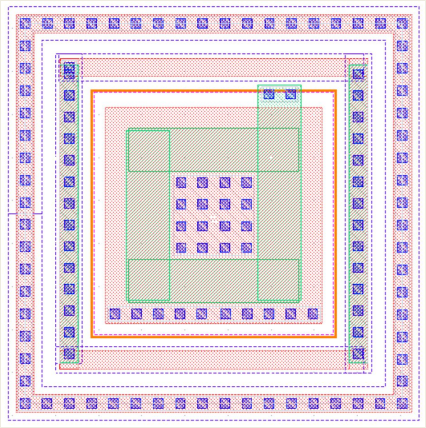
- thin gate oxide provides improved TID tolerance



Design

- ELT NMOS transistors have been used to reduce leakage due to TID

- double guard rings around p-wells and n-wells, biased to constant voltages, have been used to prevent single event latch-ups



Schematics

- high-impedance nodes have been low pass filtered to suppress single event upsets

- short channel (<120 nm) transistors have been avoided to prevent RISCE effect

- triple modular redundancy have been used for the most critical digital blocks

- 12T instead of 7T or 9T standard cells were employed

*see References

Nearest plans

TSMC

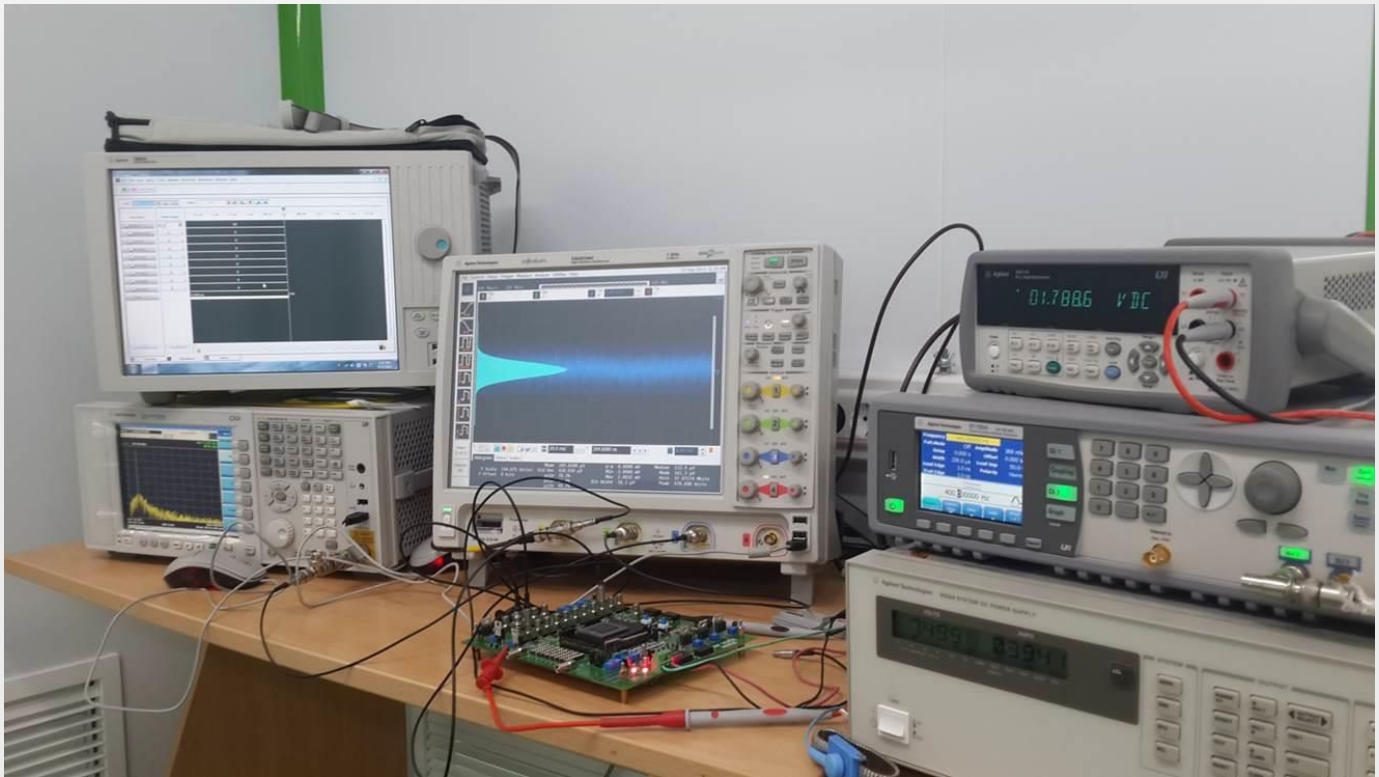
Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
TSMC 65nm CMOS Logic or Mixed-Signal/RF, Low Power*		19			13			19			18	

Nov. 18, 2020 – deadline for ASIC GDSII submission for prototyping via Europractice miniasic program

Sponsorship for fabrication is a responsibility of MPD team from JINR

Further plans (2021)

- Design of breadboard (PCB) & measurement technique
- Lab functional tests of prototyped ASICs
- Study of ASIC radiation tolerance at PNPI, Gatchina



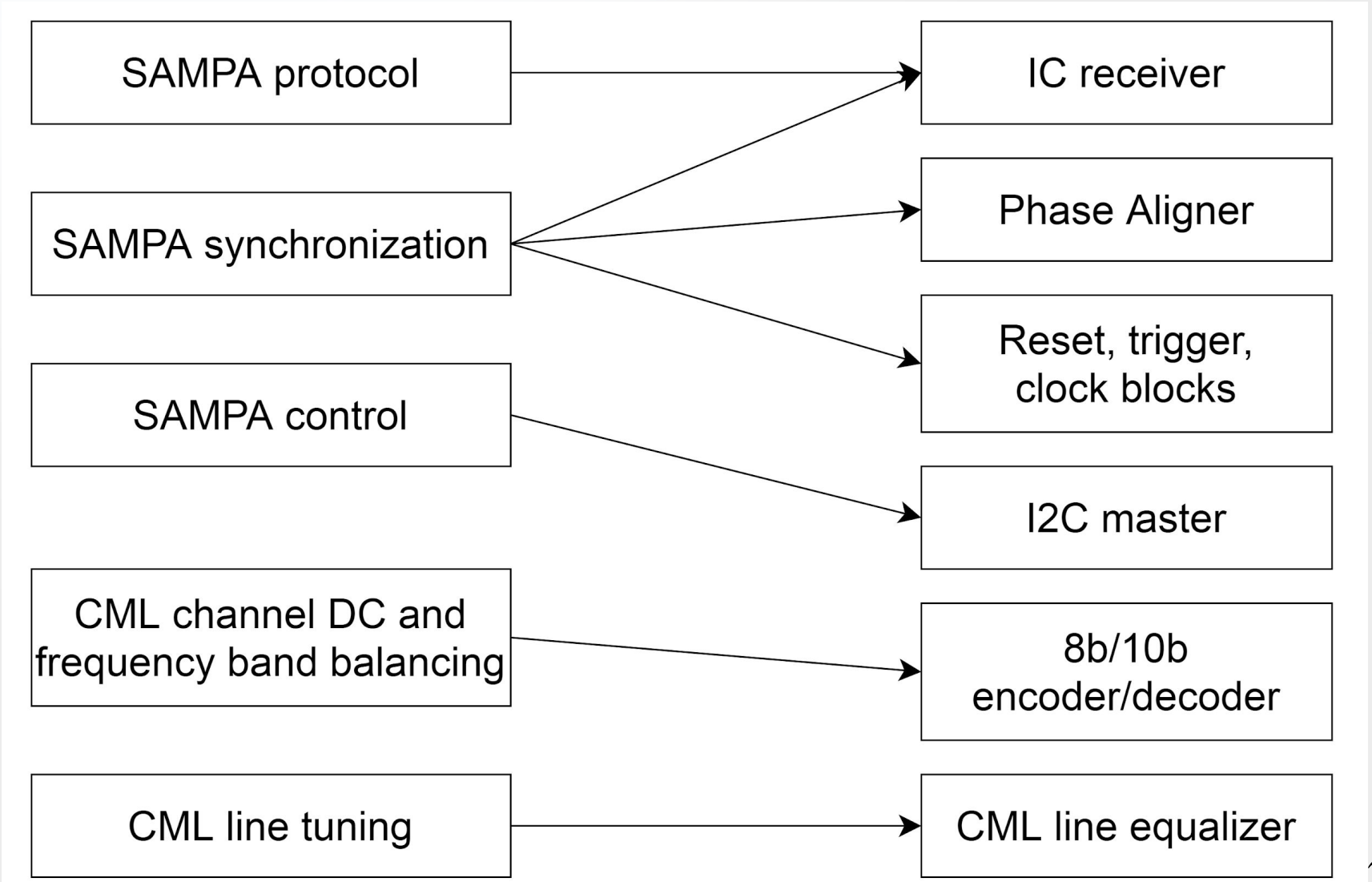
Conclusions

- Method for front-end (on-detector) data concentration has been developed
- It has been implemented in the prototype radiation tolerant CMOS ASIC, intended for the TPC FEE
- Prototype ASIC will be submitted for fabrication via Europractice soon (on Nov. 18)
- Lab functional tests of ASICs as well as their radiation tolerance tests are expected as next steps

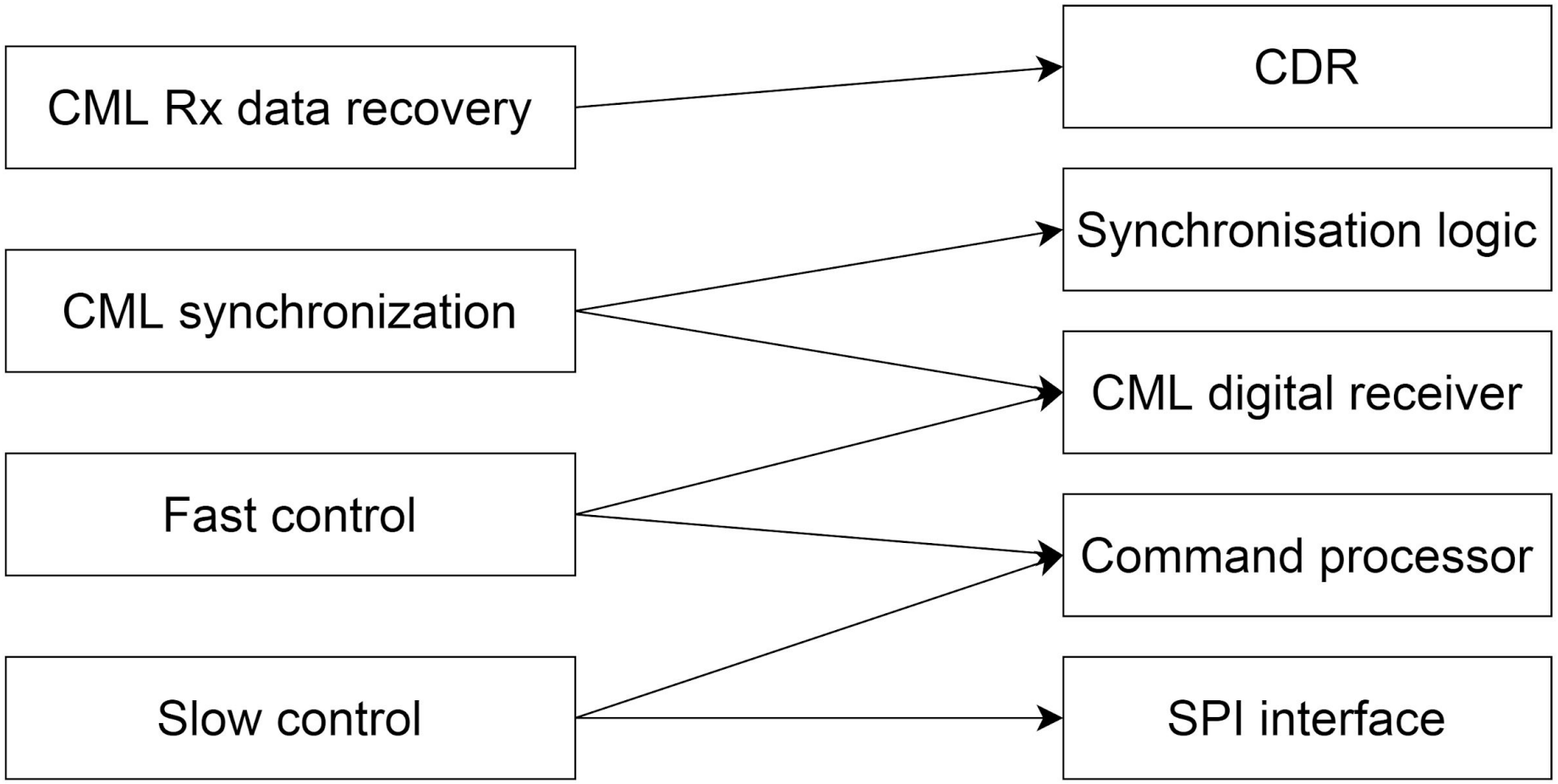
Thank you
for attention

Back up slides

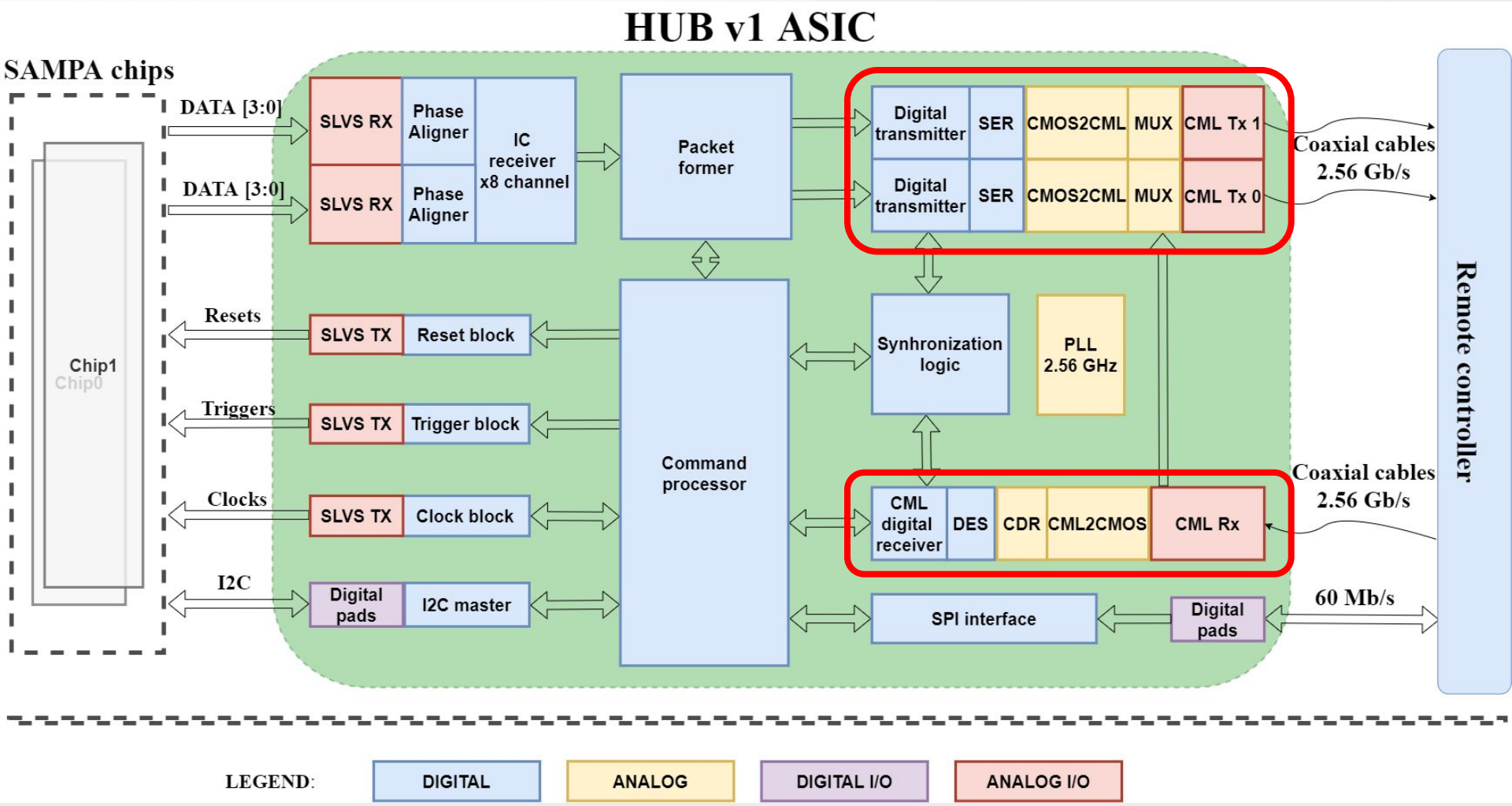
Features & blocks (1)



Features & blocks (2)

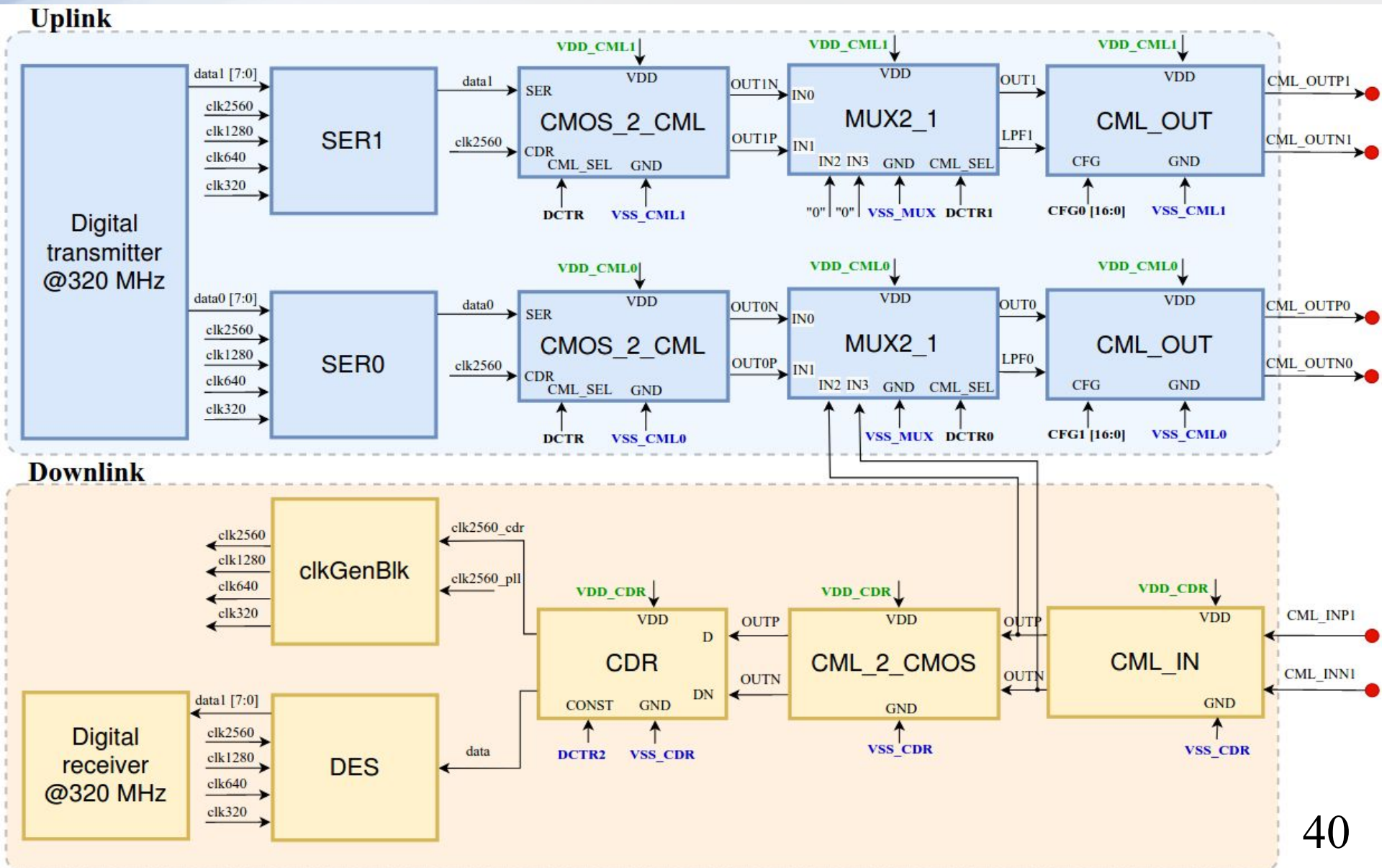


High speed interface to counting room (1)

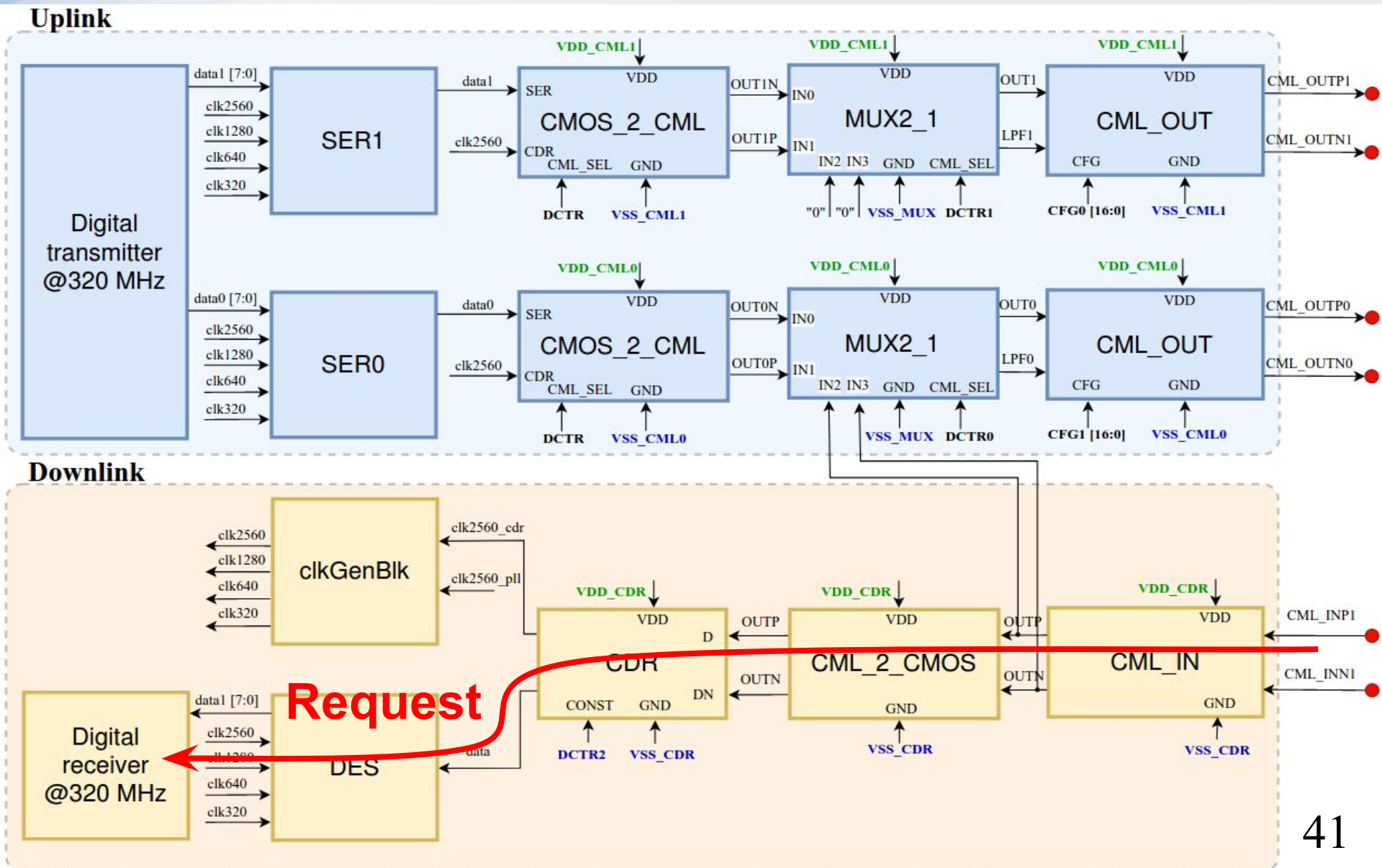


Mixed-mode (mostly digital (~70%)) design

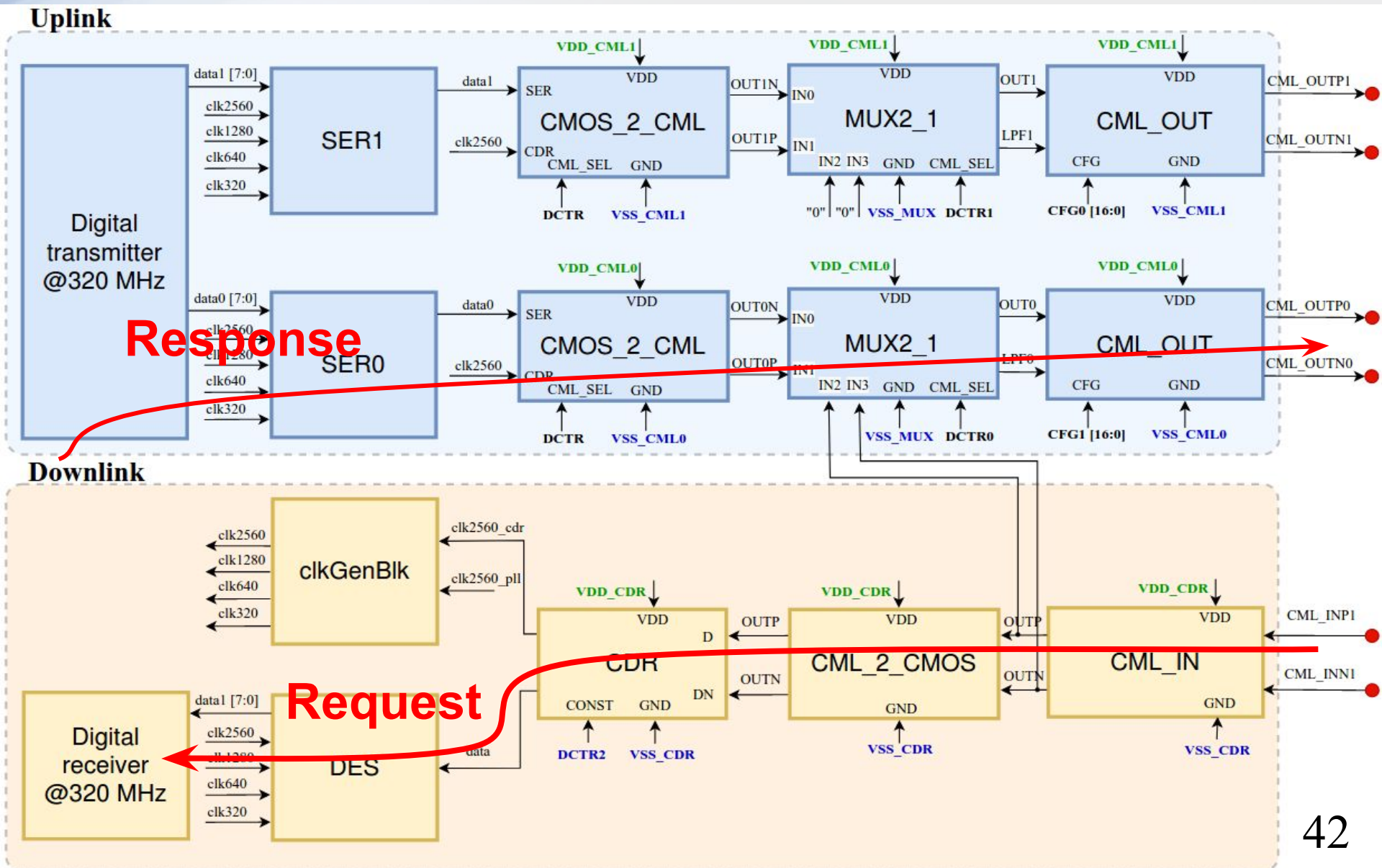
High speed interface to counting room (2)



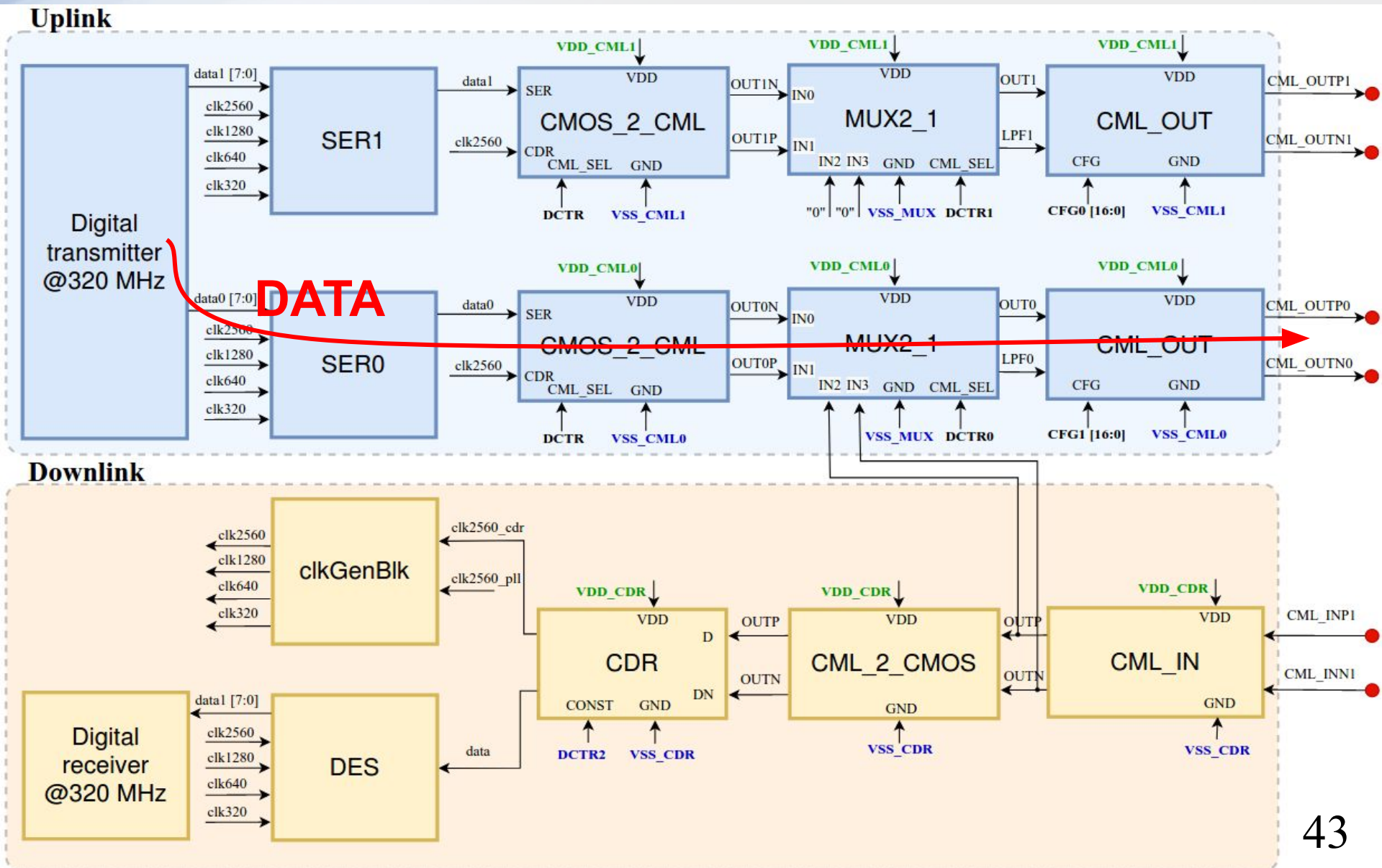
High speed interface to counting room (2)



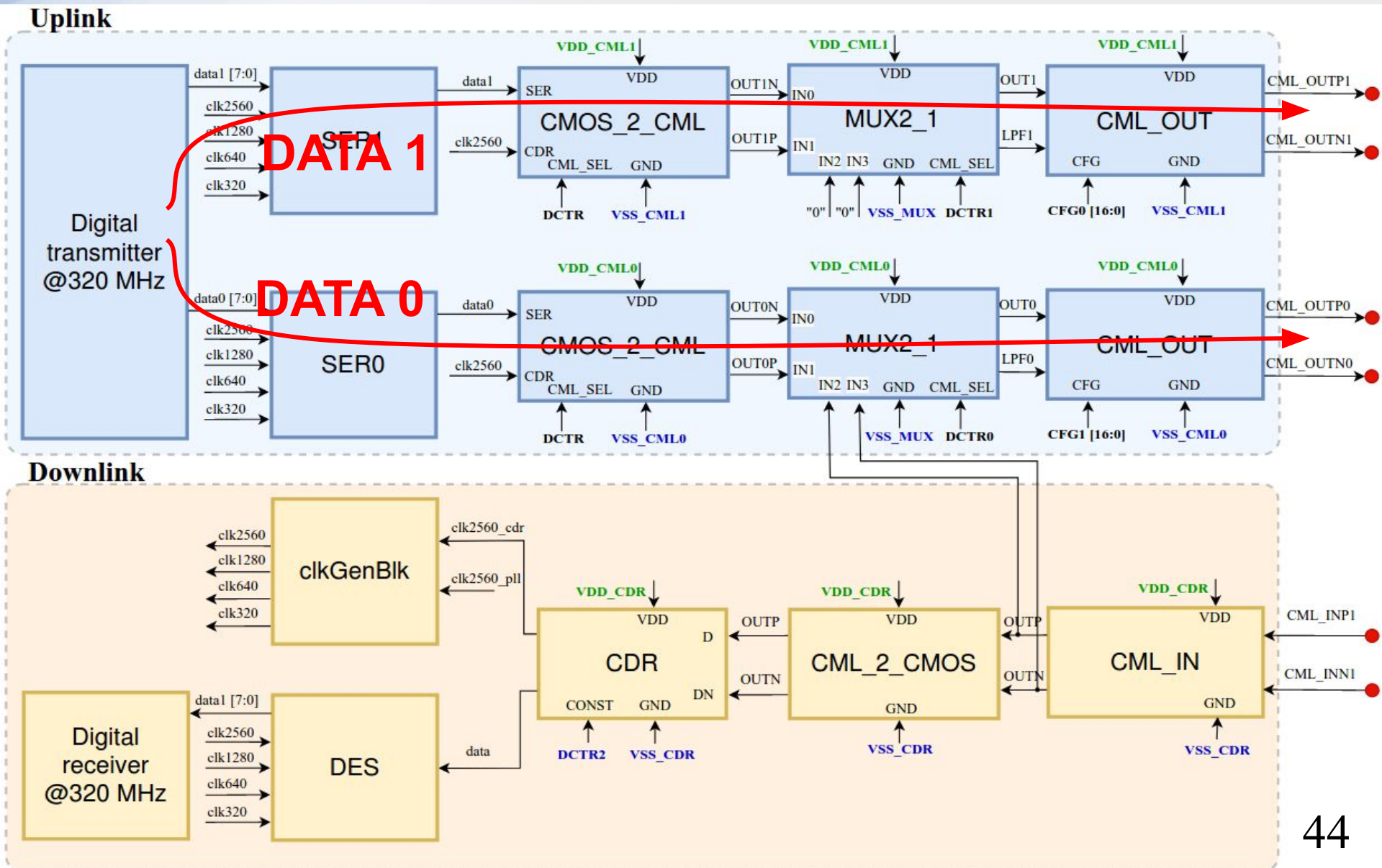
High speed interface to counting room (2)



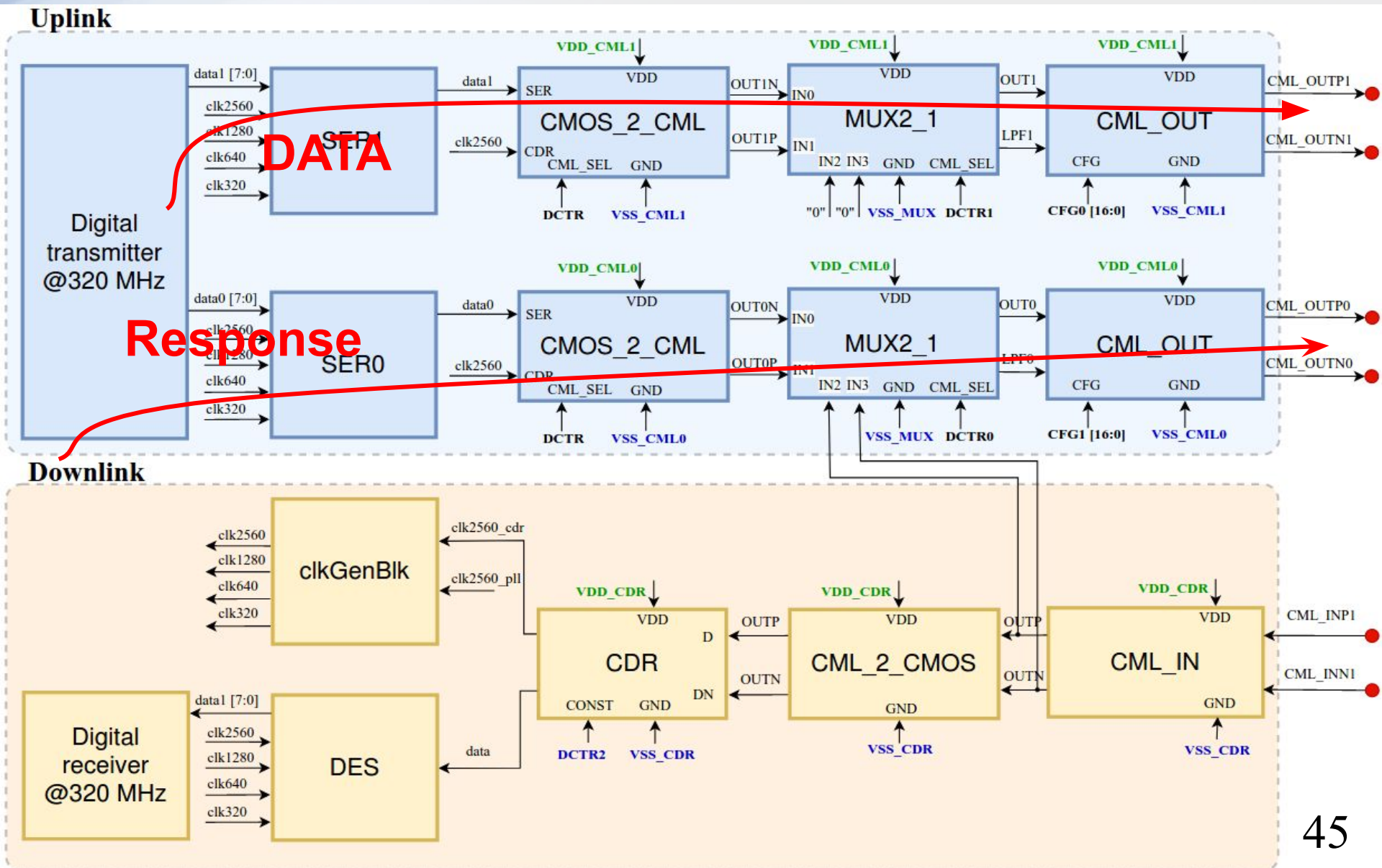
High speed interface to counting room (2)



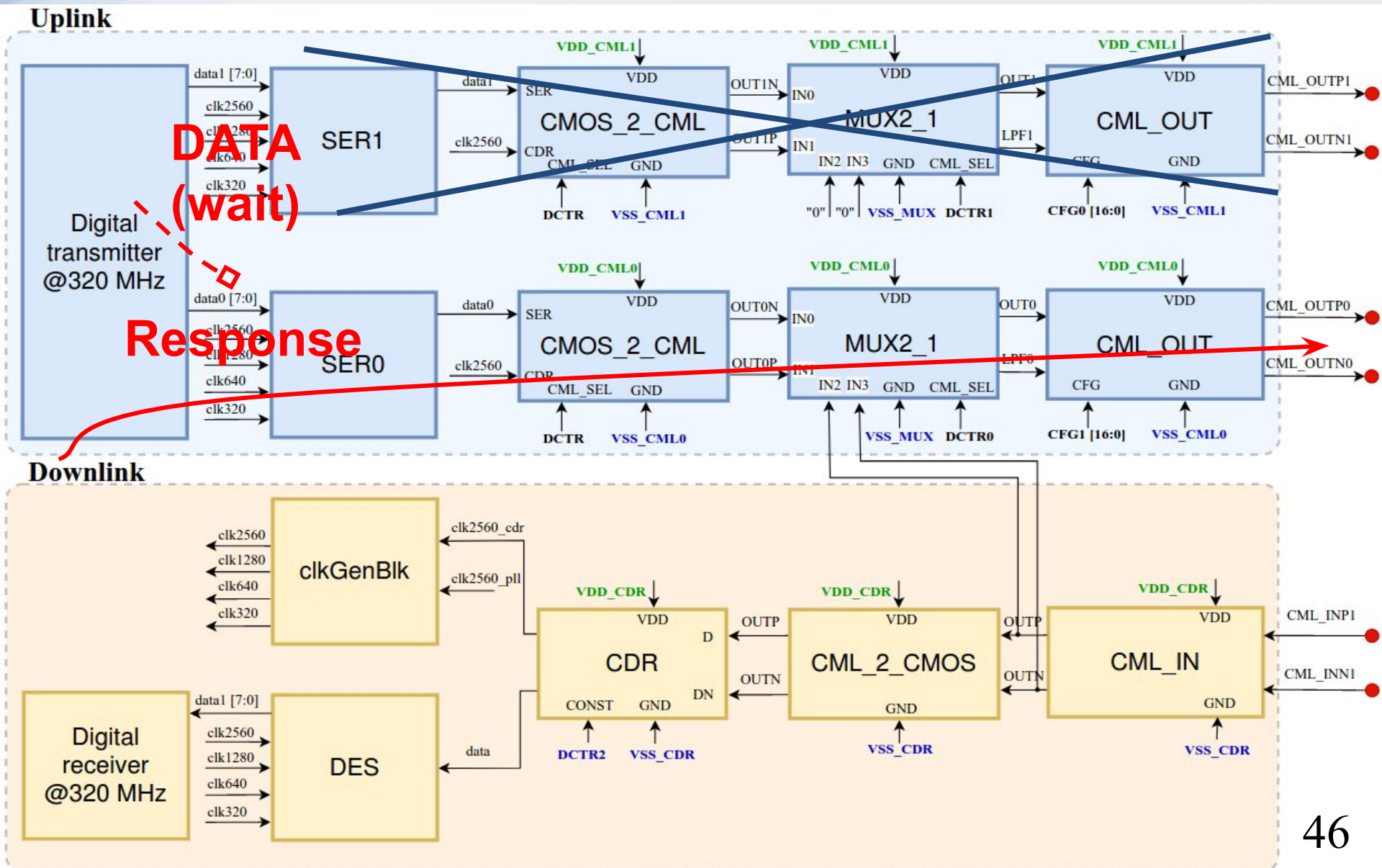
High speed interface to counting room (2)



High speed interface to counting room (2)



High speed interface to counting room (3) (one CML mode)

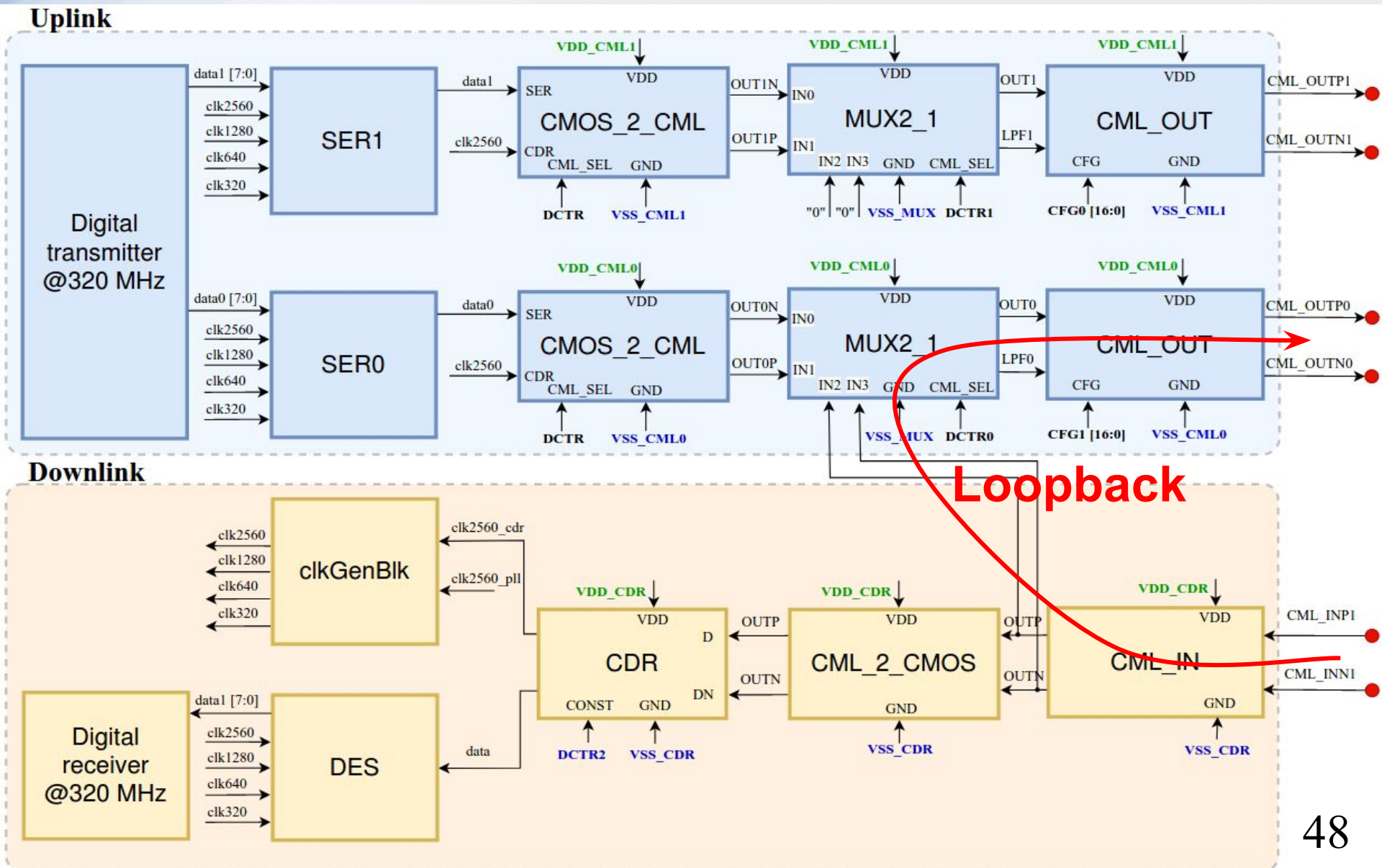


High speed interface to counting room (4)

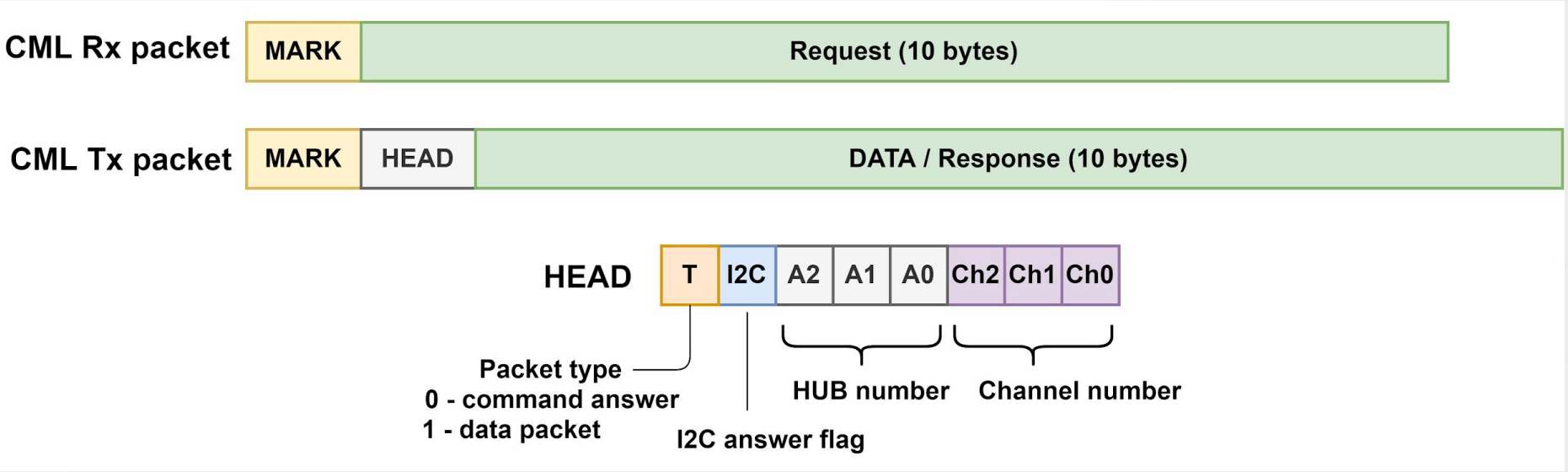
(main CML interface features)

- CML data are encoded by 8b/10b
- CML Rx receives command request
- CML Tx 0 translates command response and SAMPA data (commands have higher priority than data)
- CML Tx 1 translates SAMPA data if CML Tx 0 is busy and two CML Tx are used

High speed interface to counting room (loopback mode) (4)



CML protocol (1)



When T=0 then packet contains command Response

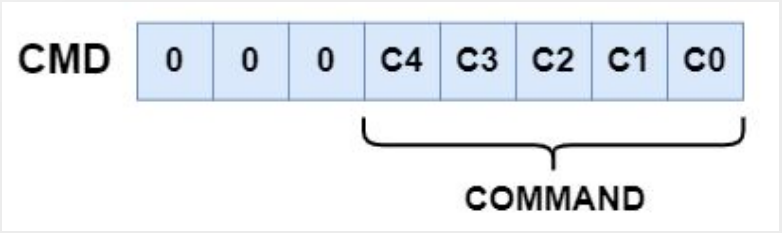
When T=1 then packet contains 10 bytes DATA

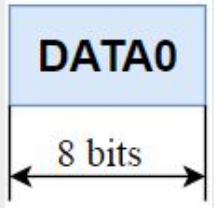
CML protocol (2)
Format of commands

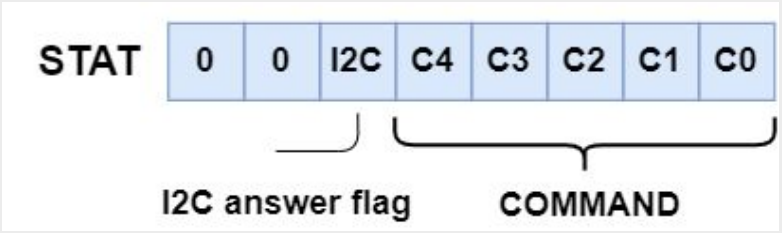
Request	CMD	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
Response	STAT	DATA8	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Commands:

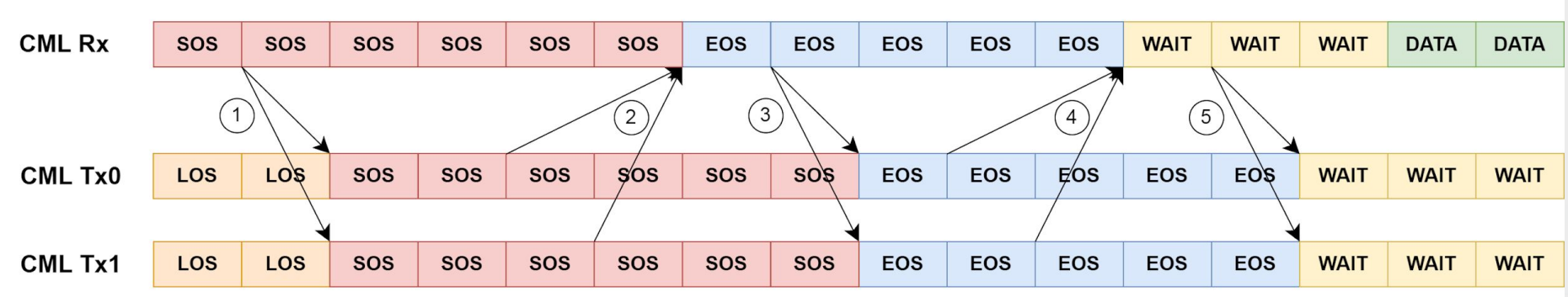
- Config load
- Config read
- ASIC Soft Reset
- SAMPA Trigger out
- SAMPA reset
- I2C read
- I2C write
- Debug commands







CML protocol (3)
Synchronization procedure



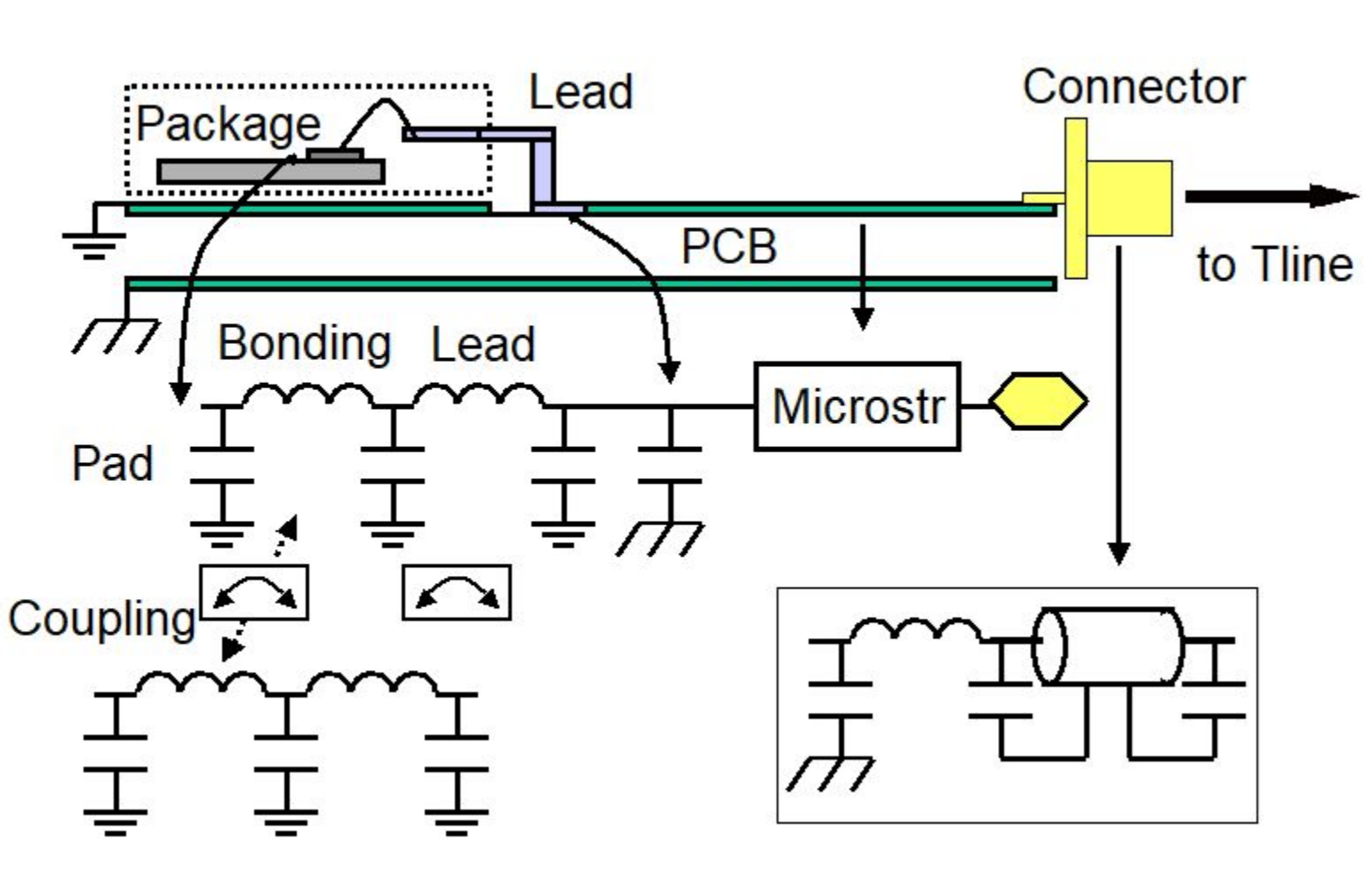
Steps:

1) ASIC starts of synchronization
2) Controller synchronize both channels
3) ASIC sends EOS
4) Controller finalize synchronization
5) ASIC finalize synchronization

CML modes:

- LOS (lost of sync) - K28.4
- SOS (start of sync) - K28.1
- EOS (end of sync) - K28.3
- WAIT - K28.5
- Data packet
- Command packet

CML interface parasitics



Some tips and tricks on radiation tolerance

Krohn M., Bentele B., Christian D., Cumalat J., Deptuch G., Fahim F., Hoff J., Shenai A., Wagner S. Radiation tolerance of 65nm CMOS transistors // J. of Instr., 2015, V.10, pp. C05009.

Bucher M., Nikolaou A., Papadopoulou A., Makris N., Chevas L., Borghello G., Koch H., Faccio F. Total Ionizing Dose Effects on Analog Performance of 65 nm Bulk CMOS with Enclosed-Gate and Standard Layout // 2018, at International Conference on microelectronic test structures, Austin, USA.

Bonacini, P. Valerio, R., Avramidou R., Ballabriga R., Faccio F., Kloukinas K., Marchioro A. Characterization of a commercial 65 nm CMOS technology for SLHC applications // JINST, 2012, V.7, pp. P01015.

Kulis S., Jara Casas L., Ceresa D., Miryala S., Christianses J., Francisco R., Gnani D. Characterization of radiation effects in 65 nm digital circuits with the DRAD digital radiation test chip // J. of Instr., 2017, V.12, pp. C02039-C02039.

Lacoe R., Improving Integrated Circuit Performance Through the Application of Hardness-by-Design Methodology // IEEE Transactions on Nuclear Science, 2008, V.55, pp. 1903-1925.

Fleetwood D., Total Ionizing Dose Effects in MOS and Low-Dose-Rate-Sensitive Linear-Bipolar Devices // IEEE Transactions on Nuclear Science, 2013, V.60, pp. 1706-1730.

Claeys C., Simoen E., Physics and Modeling of Radiation Effects in Advanced CMOS Technology Nodes. // Simulation of Semiconductor Processes and Devices, Springer, 2004, pp.181-190.

Camplani A. Shojaii S., Shrimali H., Stabile A., Liberali V. CMOS IC Radiation Hardening by Design, 2014, V.27, pp. 251-258.

Seixas L., Goncalez O., Souza R., Finco S., Vaz R., da Silva G., Gimenez S. Improving MOSFETs' TID Tolerance Through Diamond Layout Style // IEEE Transactions on Device and Materials Reliability, 2017, V.17, pp. 593-595.

Faccio F. Michelis S., Cornale D., Paccagnella A., Gerardin S. Radiation-induced short channel (RISCE) and narrow channel (RINCE) effects in 65 and 130 nm MOSFETs // IEEE Trans. Nucl. Sci., 2015, V.62, pp. 2933-2940.

Menouni M., Barbero M., Bompard F., Bonacini S., Fougeron D., Gaglione R., Pozanov A., Valerio P., Wang A. 1-Grad total dose evaluation of 65nm CMOS technology for the HL-LHC upgrades // J. of Instr., 2015, V.10, pp. C05009.

Lee M., Lee H. "Dummy Gate-Assisted n-MOSFET Layout for a Radiation-Tolerant Integrated Circuit // IEEE Transactions on Nuclear Science, 2013, V.60, pp. 3084-3091.

Díez-Acereda V., Khemchandani S.,, del Pino J., Mateos-Angulo S. RHBD Techniques to Mitigate SEU and SET in CMOS Frequency Synthesizers // Electronics, 2019, V.8 p. 690.

Maurice G. et al. (RD53 Collab.) The RD53A Integrated Circuit // CERN-RD53-PUB-17-001, 2019, Version 3.51.