Readout electronics for TPC detector in the MPD/NICA project

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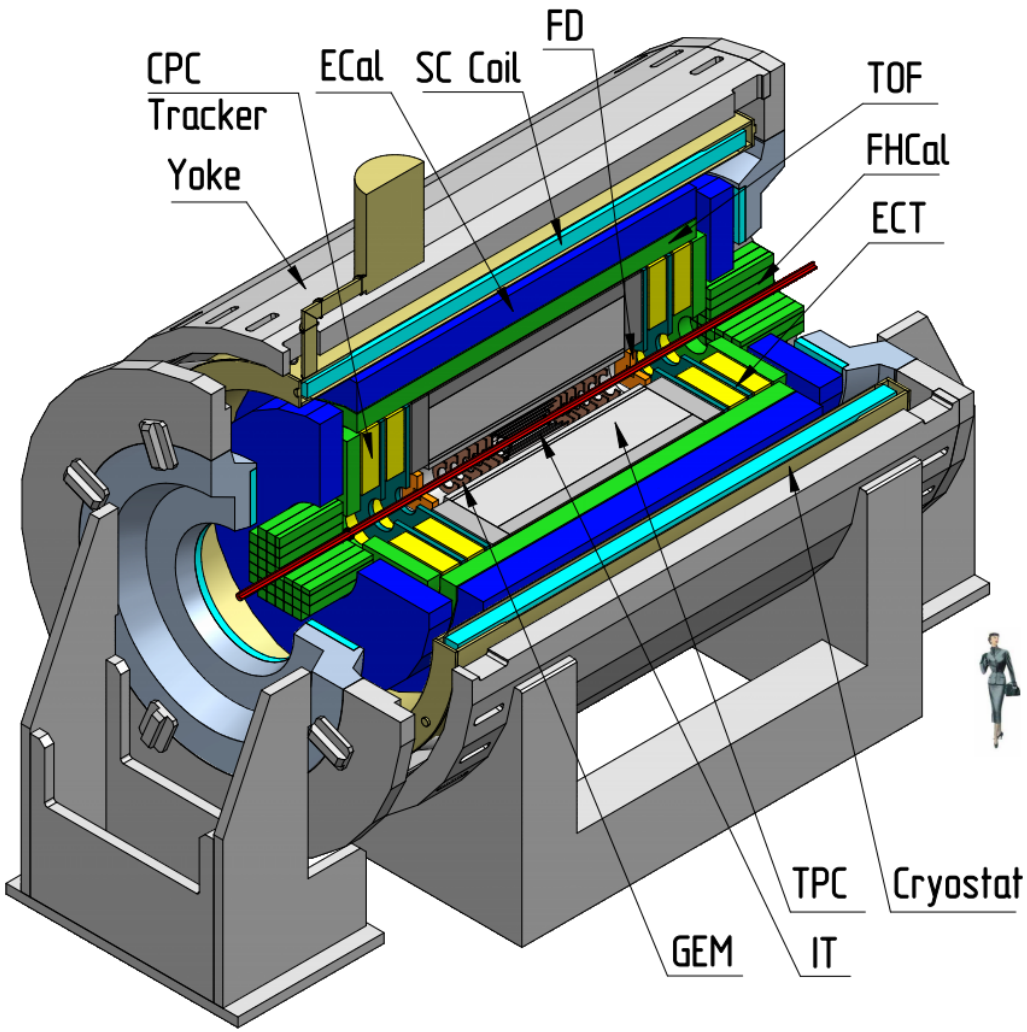
Outline

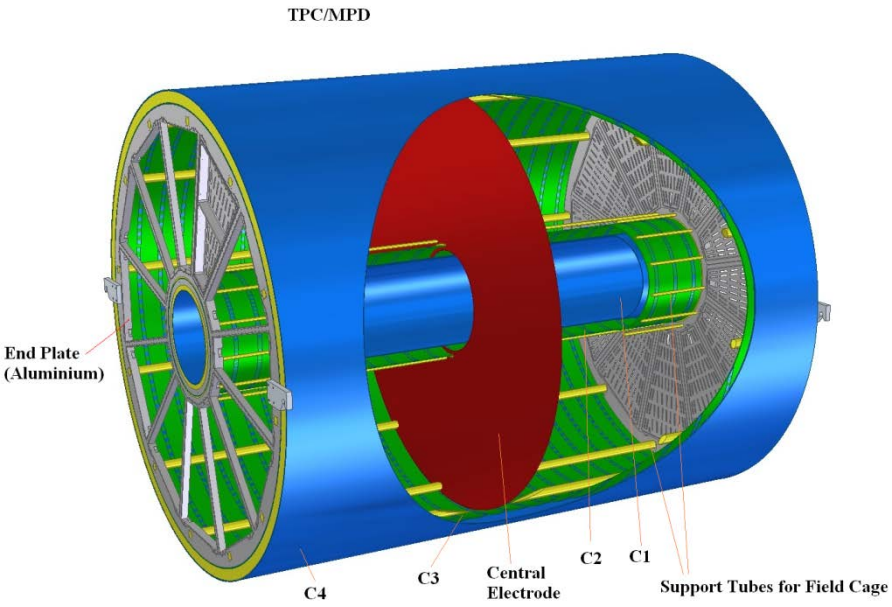
- TPC/MPD design overview and general characteristics
- Requirements for the data readout system
- Readout Control Unit (RCU)
- Front-End Card (FEC)
- Testing of FEE
- Future improvements (possible design version)
- Conclusions

General view of the TPC in the MultiPurpose Detector (MPD) of NICA project



TPC - Time projection chamber
IT - Inner Tracker
TOF - Time of Flight
ECal - Electromagnetic calorimeter
ETC - Straw end-cap tracker
FHCal - Forward Hadron Calorimeter
FD - Forward Detector
CPC tracker - Cathode Pad Chamber

TPC parameters



Item	Dimension
Length of the TPC	340cm
Outer radius of vessel	140cm
Inner radius of vessel	27 cm
Outer radius of the drift volume	133cm
Inner radius of the drift volume	34cm
Length of the drift volume	170cm (of each half)
HV electrode	Membrane at the center of the TPC
Electric field strength	~140V/cm;
Magnetic field strength	0.5 Tesla
Drift gas	90% Ar+10% Methane, Atmospheric pres. + 2 mbar
Gas amplification factor	~ 10^4
Drift velocity	5.45 cm/μs;
Drift time	< 30μs;
Temperature stability	< 0.5°C
Number of readout chambers	24 (12 per each end-plate)
Segmentation in φ	30°
Pad size	5x12mm^2 and 5x18mm^2
Number of pads	95232
Pad raw numbers	53
Pad numbers after zero suppression	< 10%
Maximal event rate	< 7 kHz (Lum. 10^{27})
Electronics shaping time	~180 ns (FWHM)
Signal-to-noise ratio	30:1
Signal dynamical range	10 bits
Sampling rate	10 MHz
Sampling depth	310 time buckets

Requirements for the data readout system

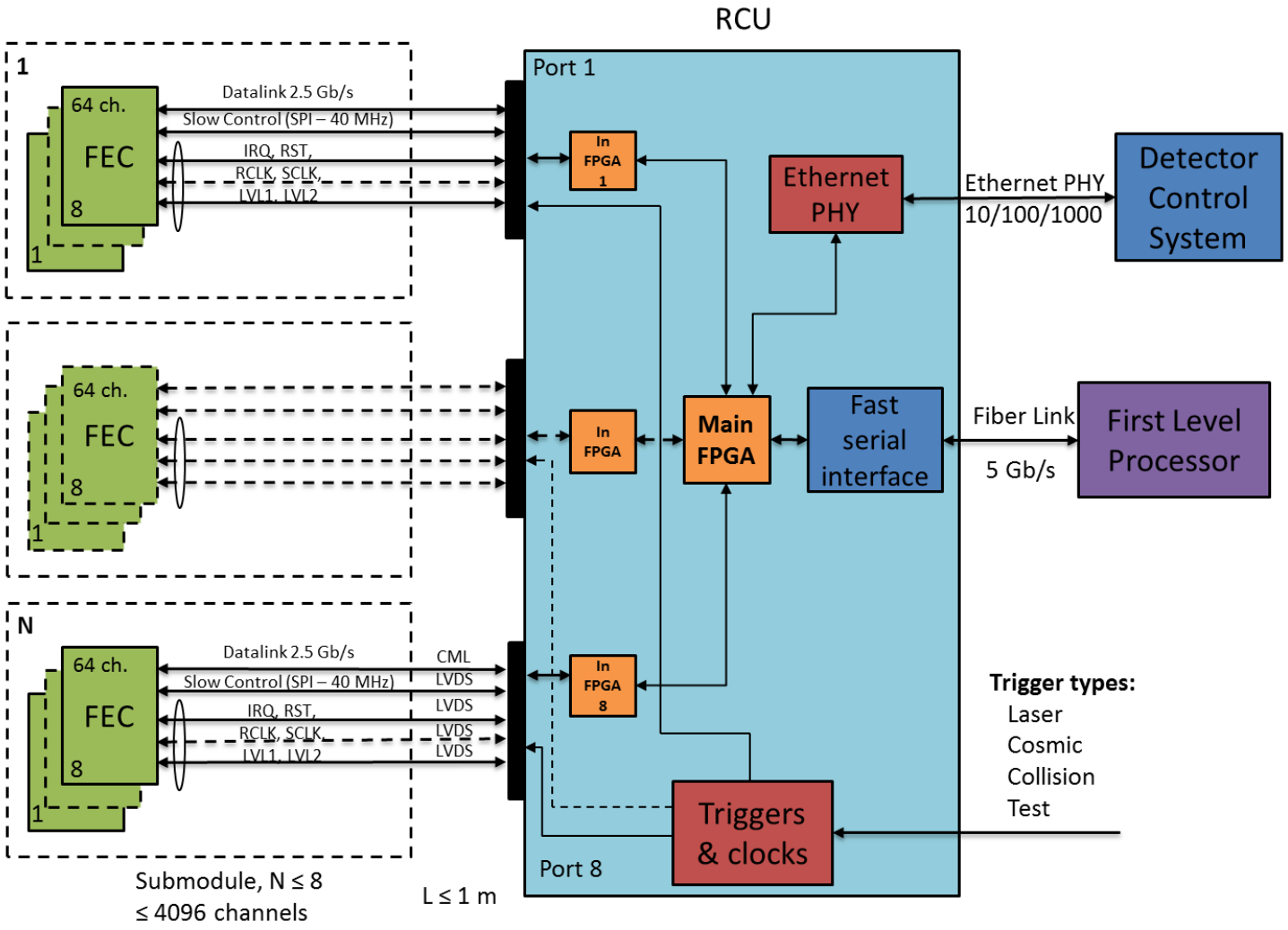
- Total number of channels is: 95 232
- Trigger rate – 7 kHz, max tracks per event - 1000
- Mean data stream with zero suppression – 7 GB/s
- Mean data stream without zero suppression – 260 GB/s

- Requirement for TPC end-caps transparency (because of FEE is shading CPC Tracker, ECT, TOF)

Readout electronics status

- Main components of FEE are FECs and RCUs
- SAMPA option – design in progress
- ALTRO+PASA option (FEC64S) - design completed
- Pilot system (512 ch) – under test
- Controller design - completed
- Controller manufacture – December 2017
- First Level Processor concept (for cosmic test)– under design

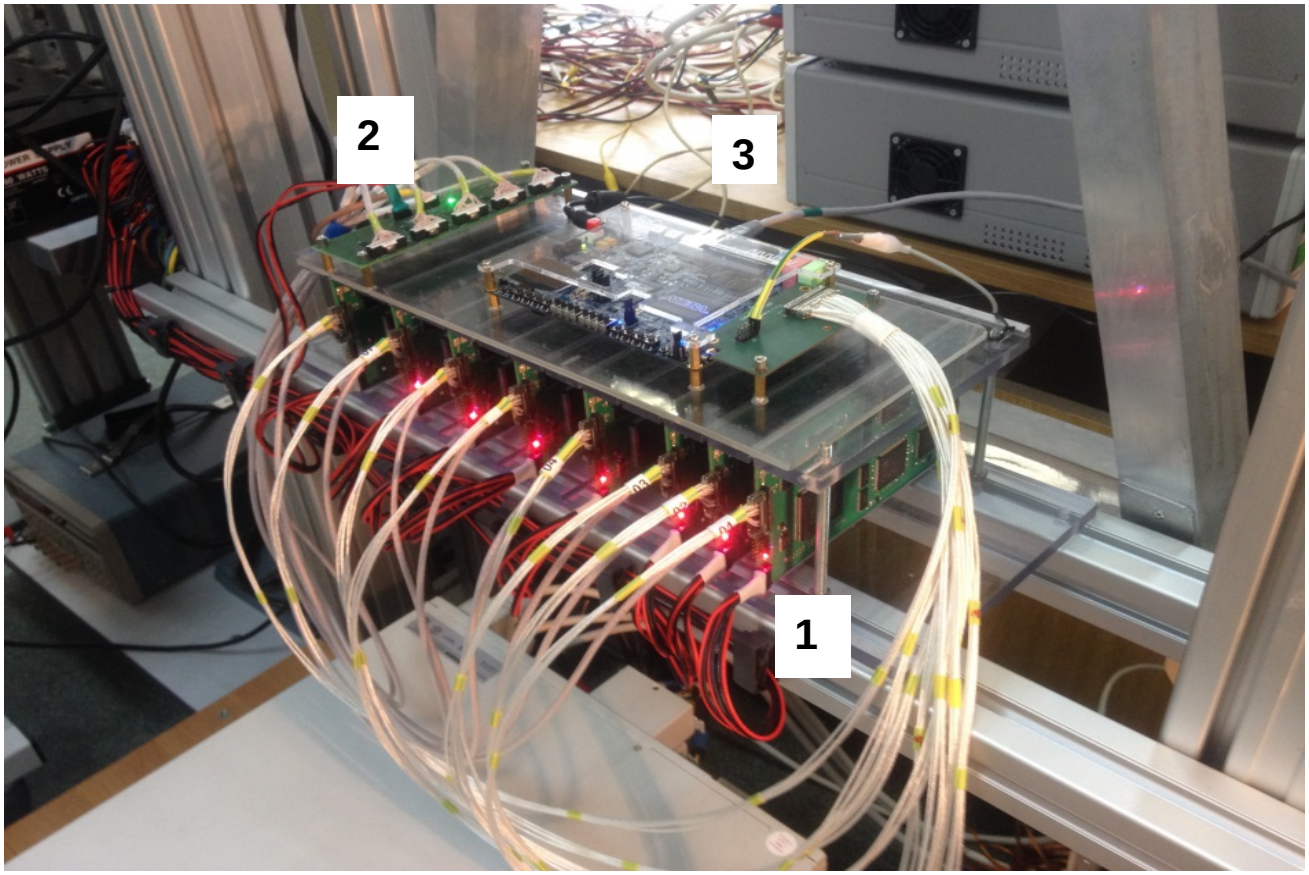
FEE block diagram for one readout chamber



Readout Control Unit (RCU)

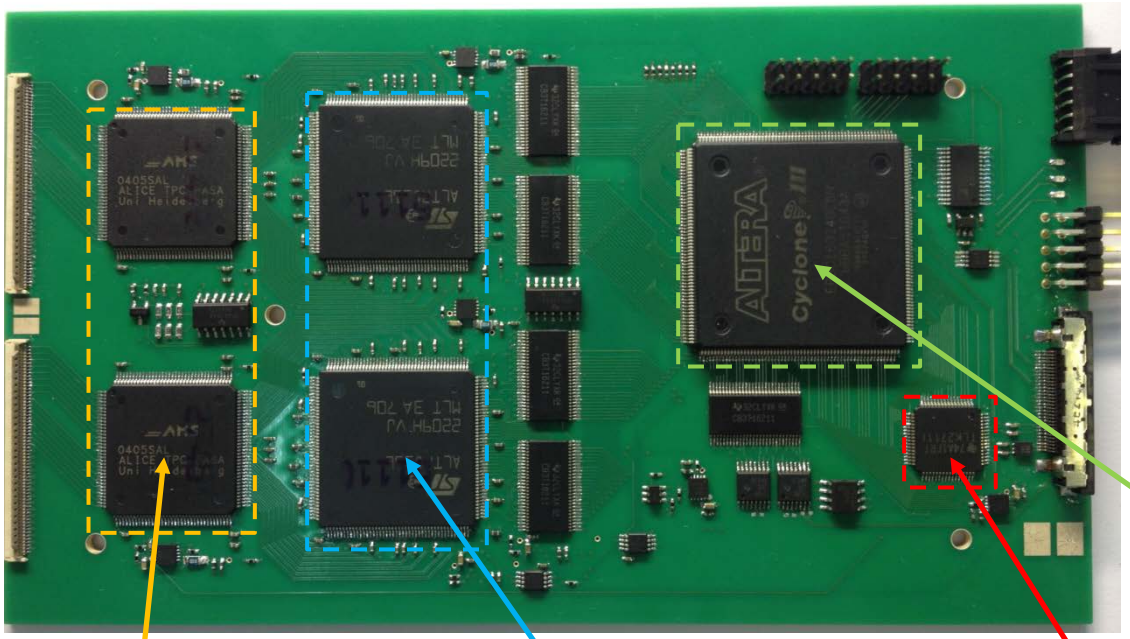
- The RCU design with base functionality including FECs initialization and data acquisition is performed.
- FPGAs firmware is designed and simulated.
- The part of FPGA firmware tested with Altera development board as RCU emulator.
- RCU full schematic is completed.
- PCB layout has started.

Eight cards at the test setup



1) FECs array (512 ch. in total); 2) clocks and control signal distribution card; 3) RCU emulator

64-ch. Front-End Card (top side)



- Signal to noise ratio, S/N - 30
- $\sigma_{NOISE} < 1000e^-$ (C=10-20 pF)
- Dynamic Range – 1000
- Zero suppression
- Buffer (4 / 8 events)

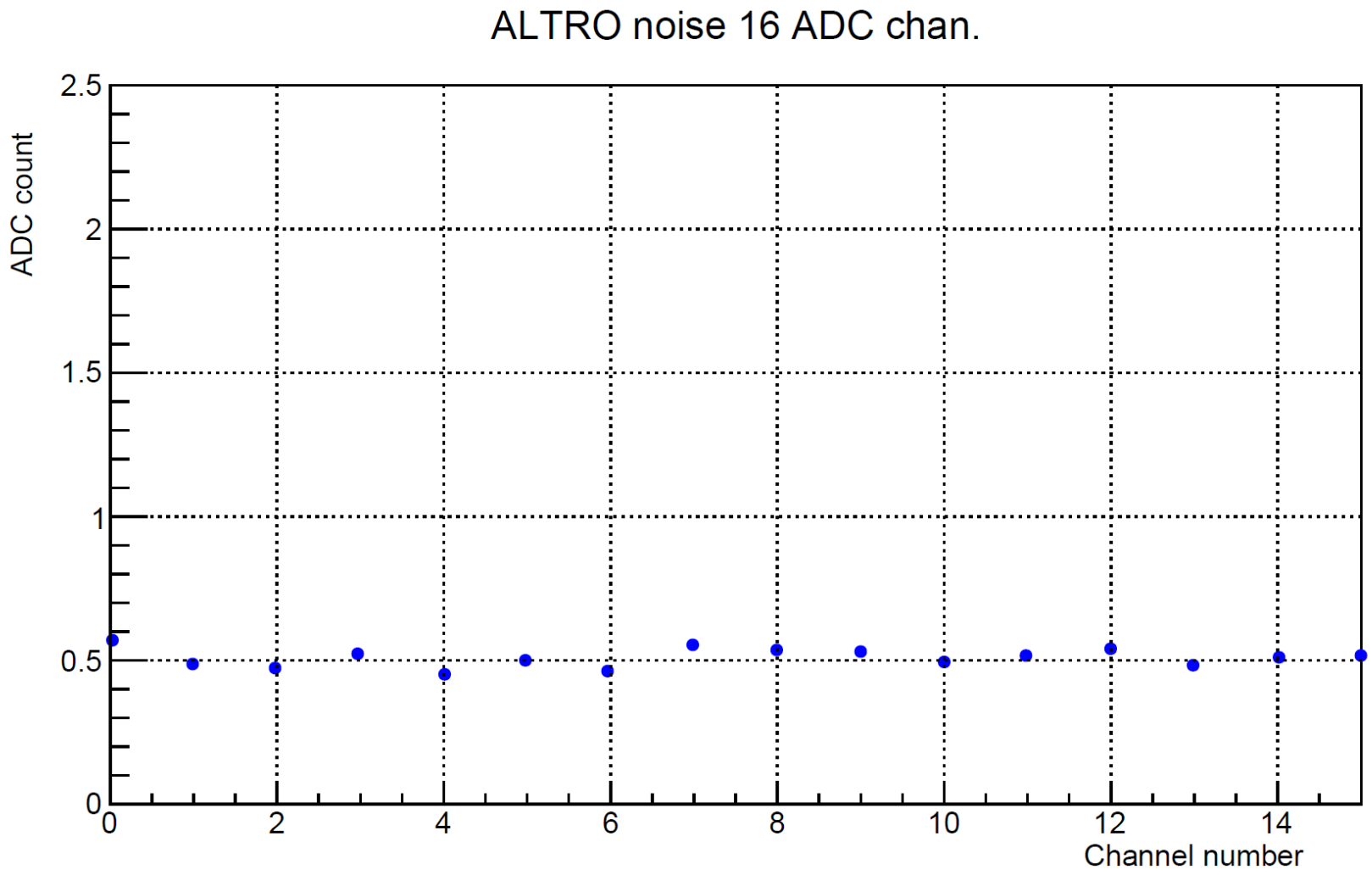
ALTERA FPGA - board control

PASA chip
16 channels ASIC (low noise amplification of the signal)

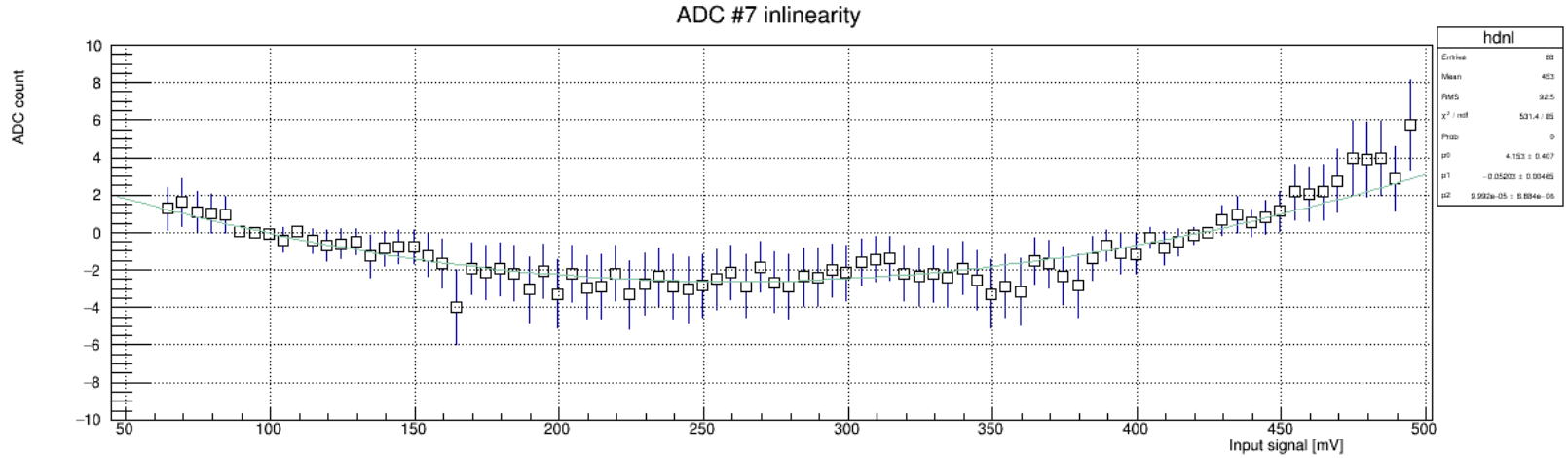
ALTRO chip
16 channels ASIC (digitization and signal processing)

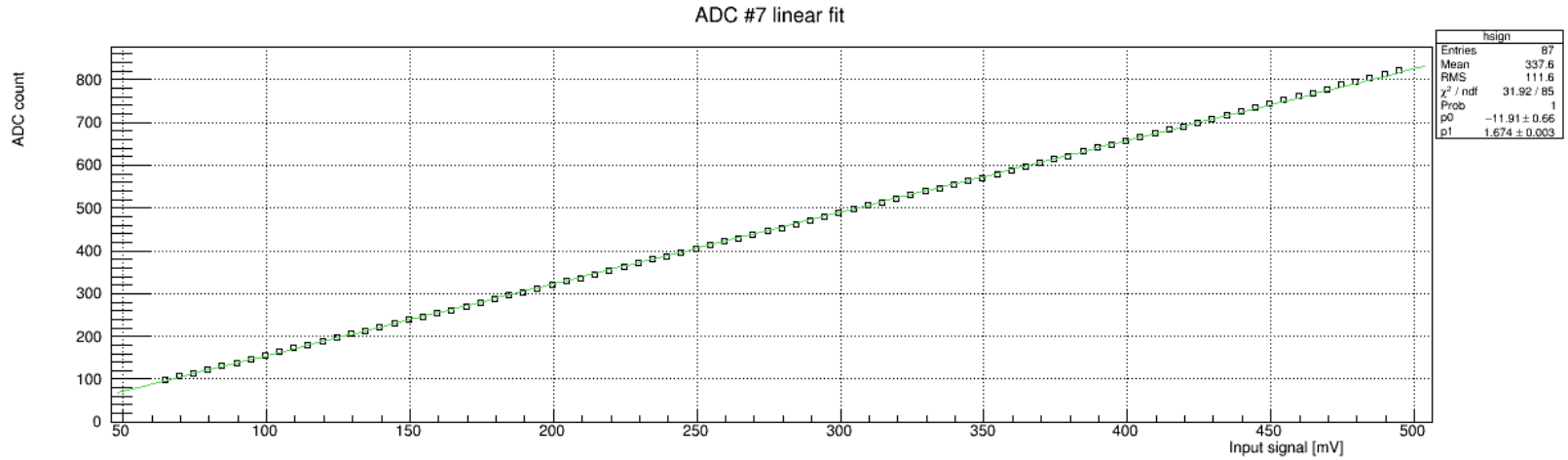
TLK2711
Serial interface
Data throughput up to 2.5 Gb/s

FEC noise measurement



FEC linearity





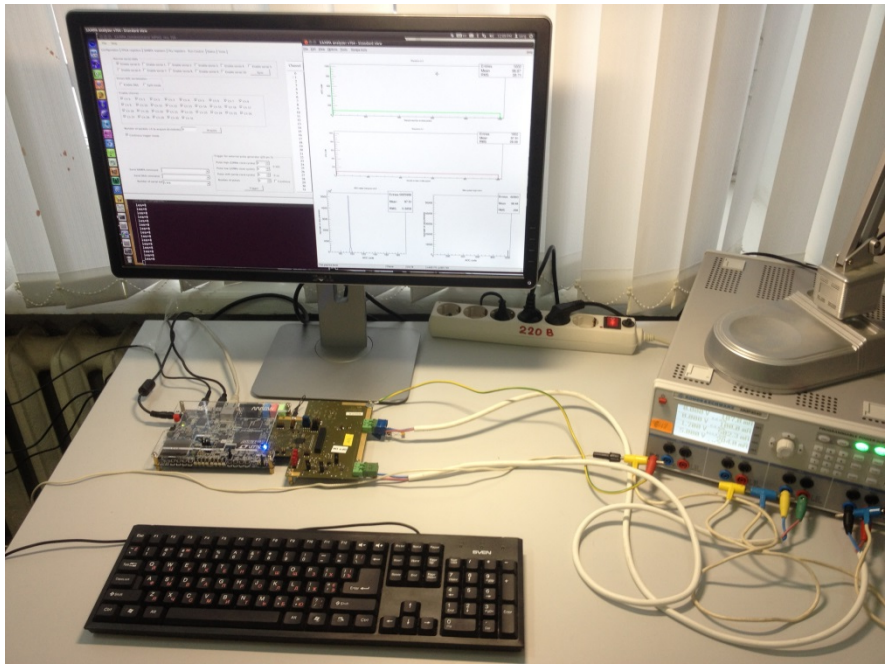
New ASIC for TPC electronics (SAMPA)

- New ASIC SAMPA [1,2] is under development.
- Few amount of pilot chips version was tested and measurement results show us feasibility of design SAMPA-based FEC for the TPC MPD/NICA.
- Concept of usage SAMPA chip in FECs was defined.

[1] S.H.I. Barboza et all. SAMPA Chip: a New ASIC for the ALICE TPC and MCH Upgrades. // J. Instrum. 2016. V. 11. C02088.

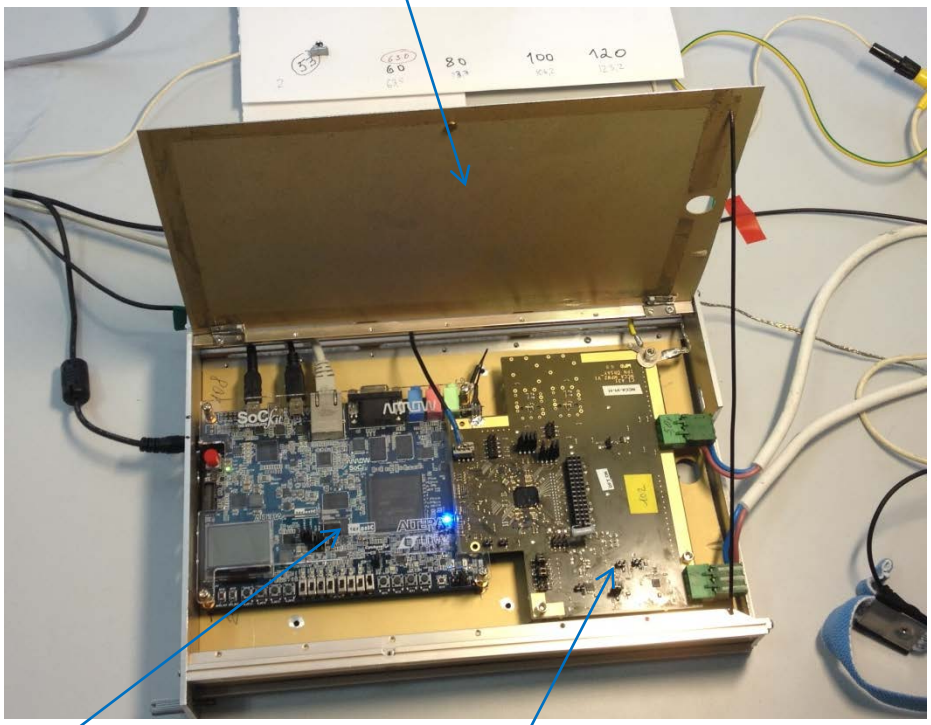
[2] J.Adolfsson et al., SAMPA Chip: the New 32 Channels ASIC for the ALICE TPC and MCH Upgrades. // J. Instrum.2017 V. 12. C04008.

SAMPA testing in Dubna



General view of test bench

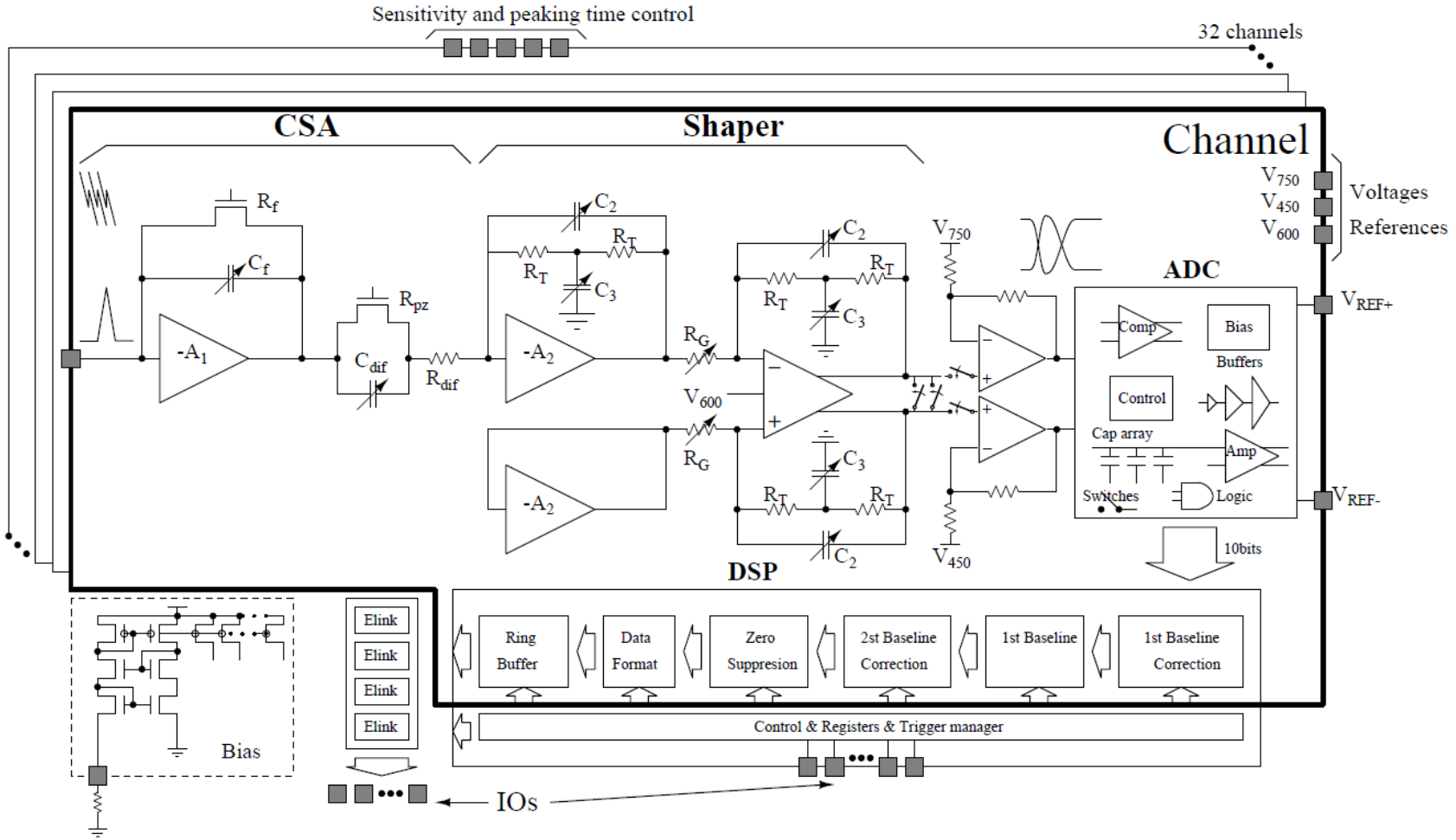
Shielding box



Altera Cyclone V
SOC Kit

SAMPA test board

SAMPA block diagram



Conclusion

- FEE TPC for MPD/NICA project was designed.
- FEC testing including analog and digital parts was performed. RCU firmware was developed and verified.
- ALTRO-based FEC design is complete and trial lot of FECs was fabricated.
- RCU prototype is under verification.
- FEC concept based on SAMPA chip is defined.

Thank you for your attention!