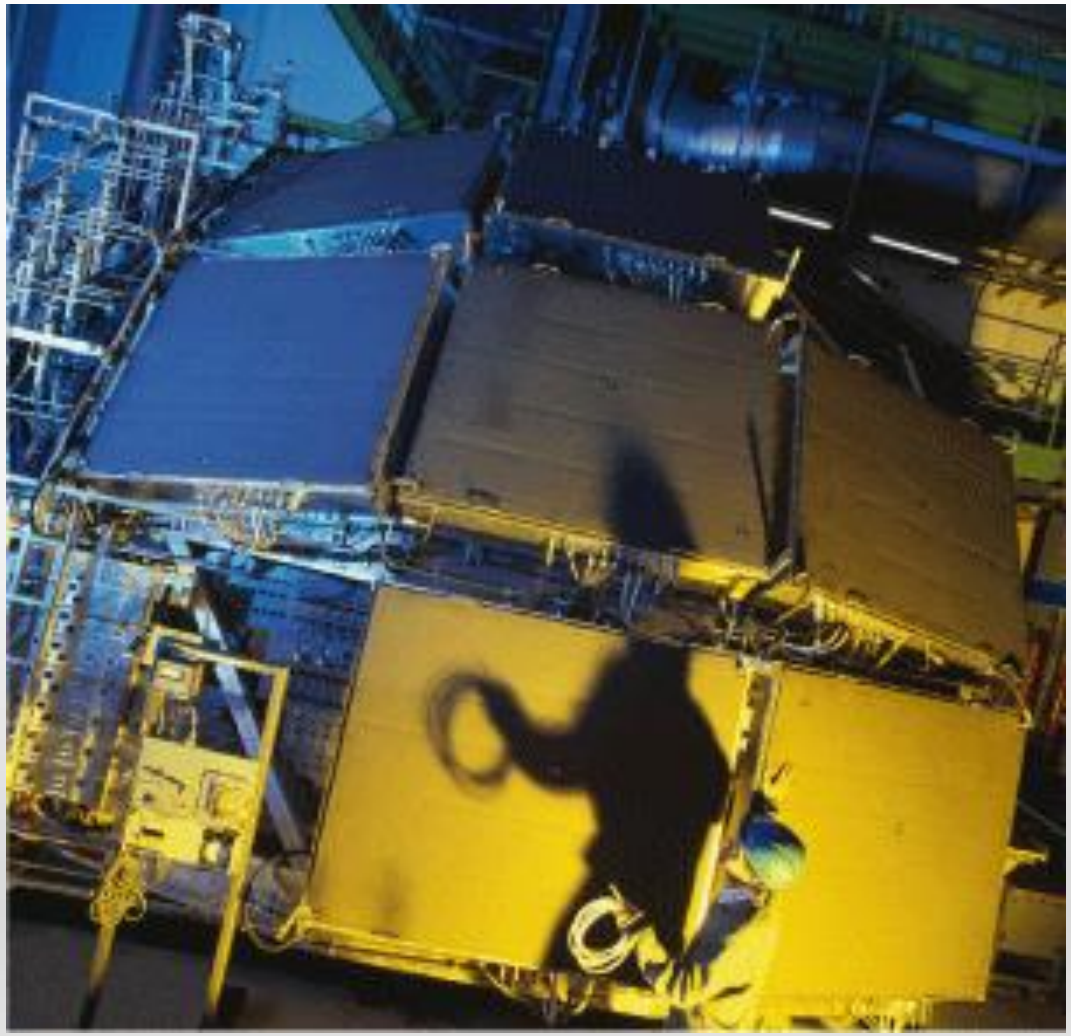


Raúl Arteche Díaz (CEADEN)

Center of Technological Applications and Nuclear Development (CEADEN), since Sept 1998.

- Working as electronic designer and Instrumentation specialist.

CERN user affiliated to the Physics department of the CEADEN, since June 2018.

- Working in the FPGA firmware upgrade for the High Momentum Particle Identification detector (HMPID).
- ALICE Webmaster

- Work experience.
- HMPID description.
- Result of the HMPID firmware upgrades.
- About ALICE ITS and MPD ITS.
- Possible contribution to MPD-ITS.

Work experience :

- Software developer for embedded systems.
- FPGA-based electronics firmware developer.
- Instrumentation specialist.
- Designer of electronic equipment.
- Interface programmer based on different protocols (I2C, SPI, RS232,CAN,USB and Ethernet)

- Full experience working with Altium Designer for electric and PCB circuit design.
- Full experience working with XILINX suite. (ISE, EDK, DSP)
- Full experience working with QUARTUS II suite.

Advance skills in several programing language :

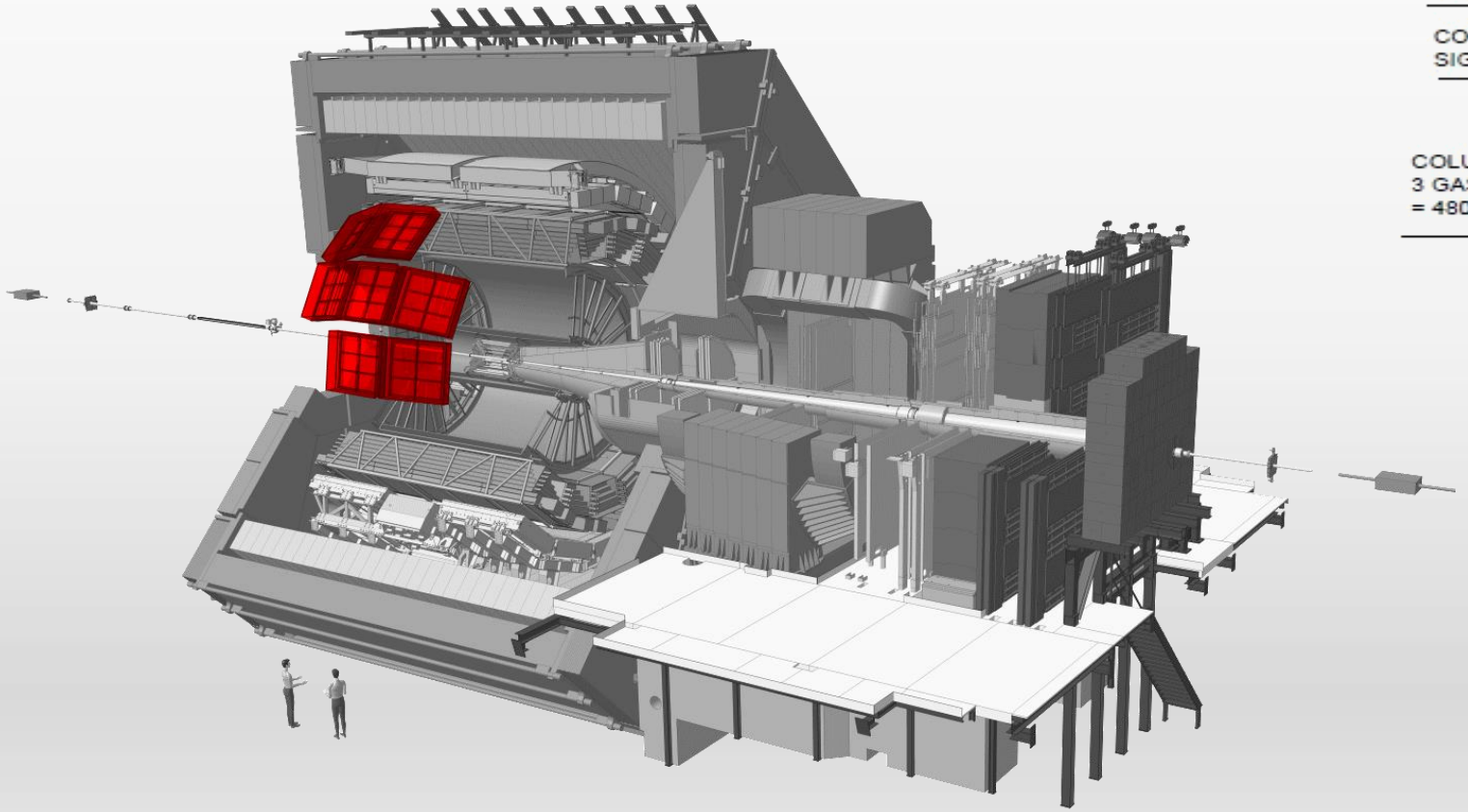
- C and C++.
- Python.
- LabVIEW programmer.

Operating system environment:

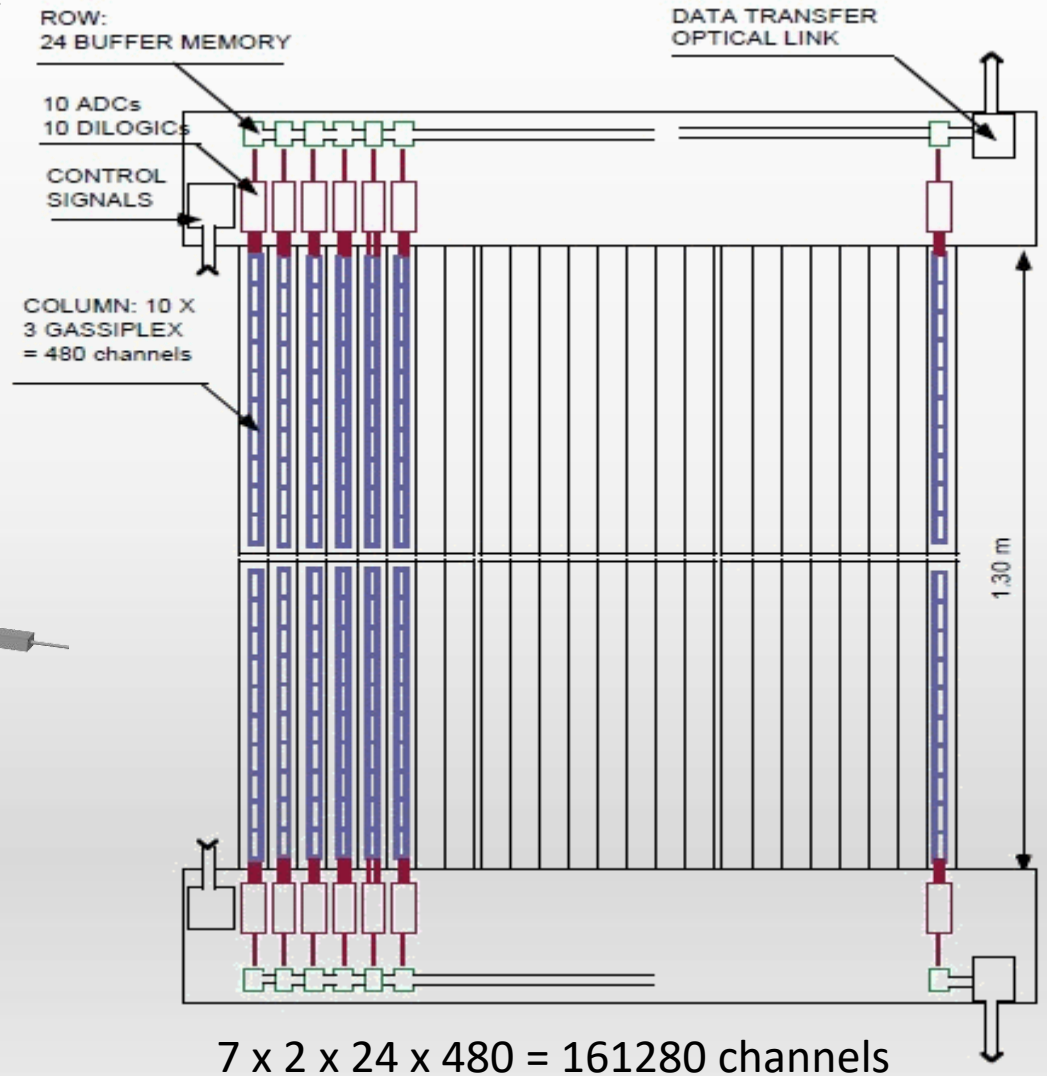
- Linux
- Windows

High Momentum Particle Identification Detector (HMPID)

The ALICE High Momentum Particle Identification (HMPID) system is composed by 7 identical RICH (**R**ing **I**maging **CH**erenkov) detectors of around 1.3x1.3 m^2 for a total CsI active area of about 11 m^2



https://cds.cern.ch/record/2302924



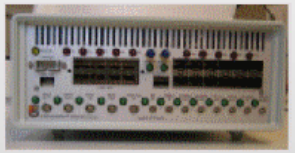
7 x 2 x 24 x 480 = 161280 channels

The front-end (FE) and read-out (RO) electronics measures the analogue signal induced on the cathode plane of a MWPC segmented into pads, in order to achieve Cherenkov photons localisation.

SIU is a Detector Data Link (**DDL**) Source Interface Unit designed for use in the data acquisition (**DAQ**) system

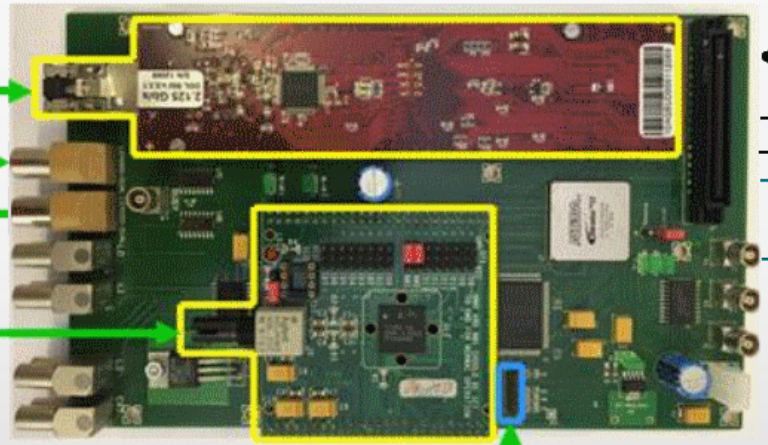
DDL SIU connected to the FLP (Bidirectional)

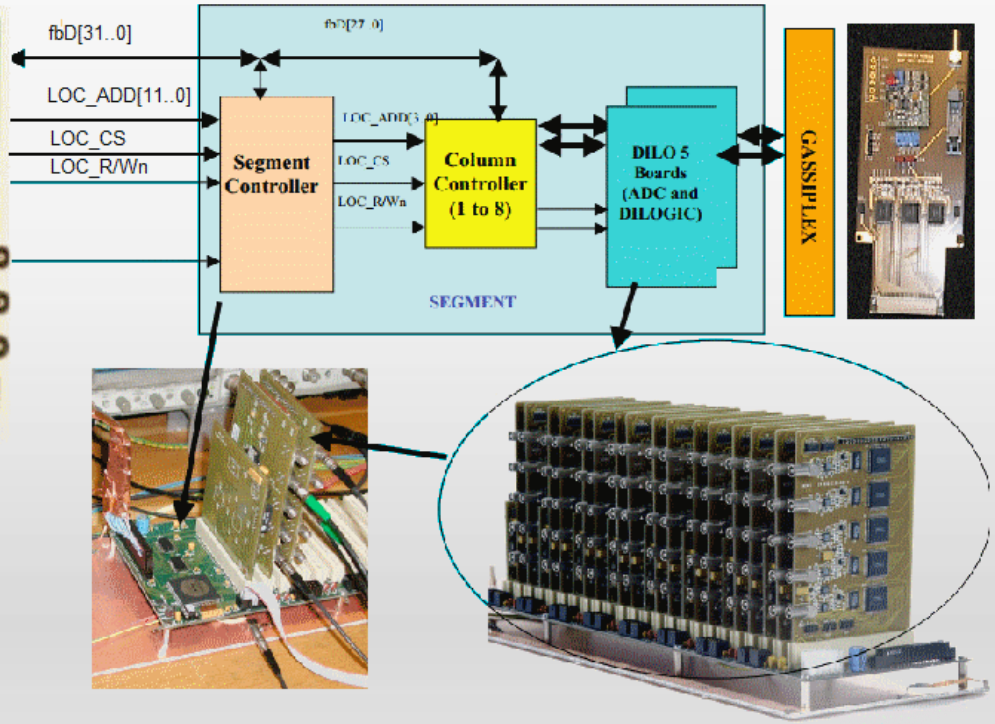
TTCRx connected to the LTU (Undirectional)



JTAG connected to ethernet programmer (Bidirectional)

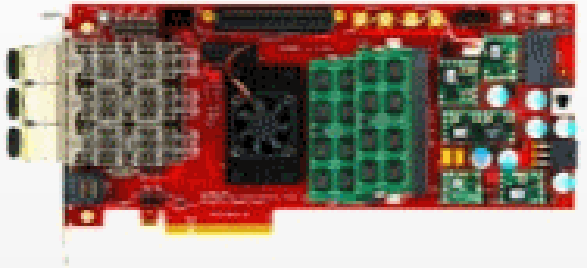
Readout Common Board (RCB)





The TTCrx acts as an interface between the Timing Trigger and Control distribution(TTC) system for LHC detectors. The LTU is common to the 14 RCB, the signals are splitters and merges using fanio VME modules and a passive optic splitter.

Detector Data Link structure



SIU is a Detector Data Link (**DDL**) Source Interface Unit designed for use in the data acquisition (**DAQ**) system of the **ALICE** experiment.

Performances

- 2.125 Gb/s optical data transmission
- Complies with CERN proprietary Detector Data Link (DDL)
- 206 MB/s maximum sustained bandwidth
- Half duplex 32-bit data path and flow control
- Radiation tolerant (tested on the ALICE radiation levels)

http://www.cerntech.hu/products/8-siu.html

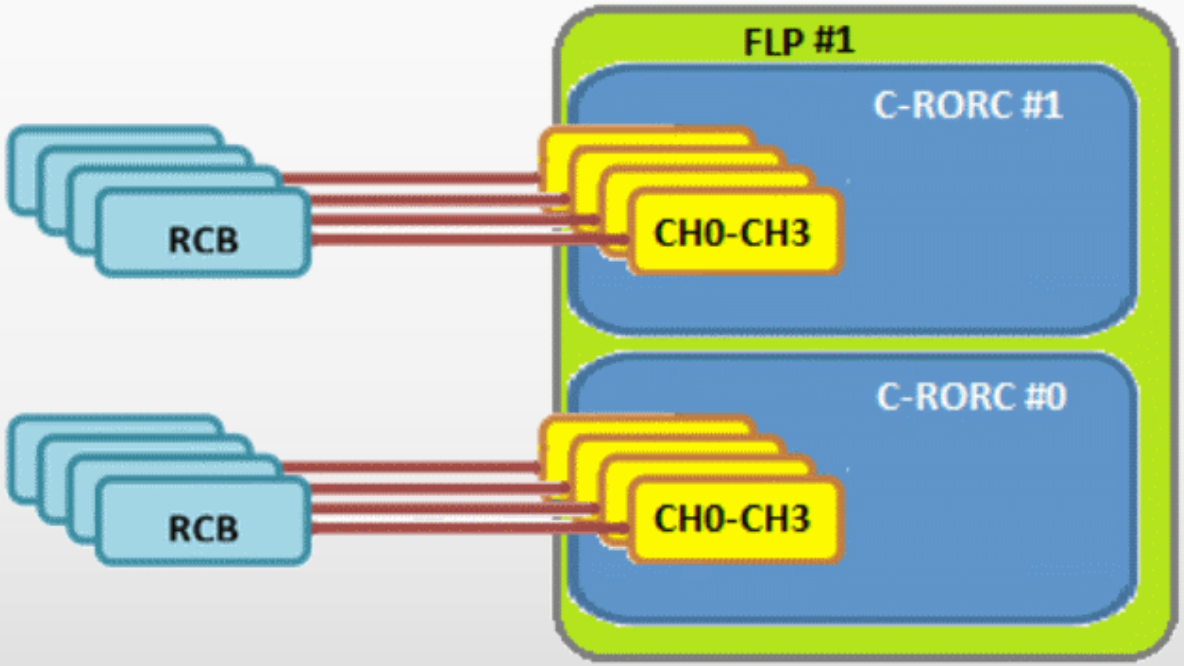
The **CRORC** is a PCI Express Read-out Receiver Card for reading out high-speed optical links of CERN experiments (ALICE, ATLAS).

Performances

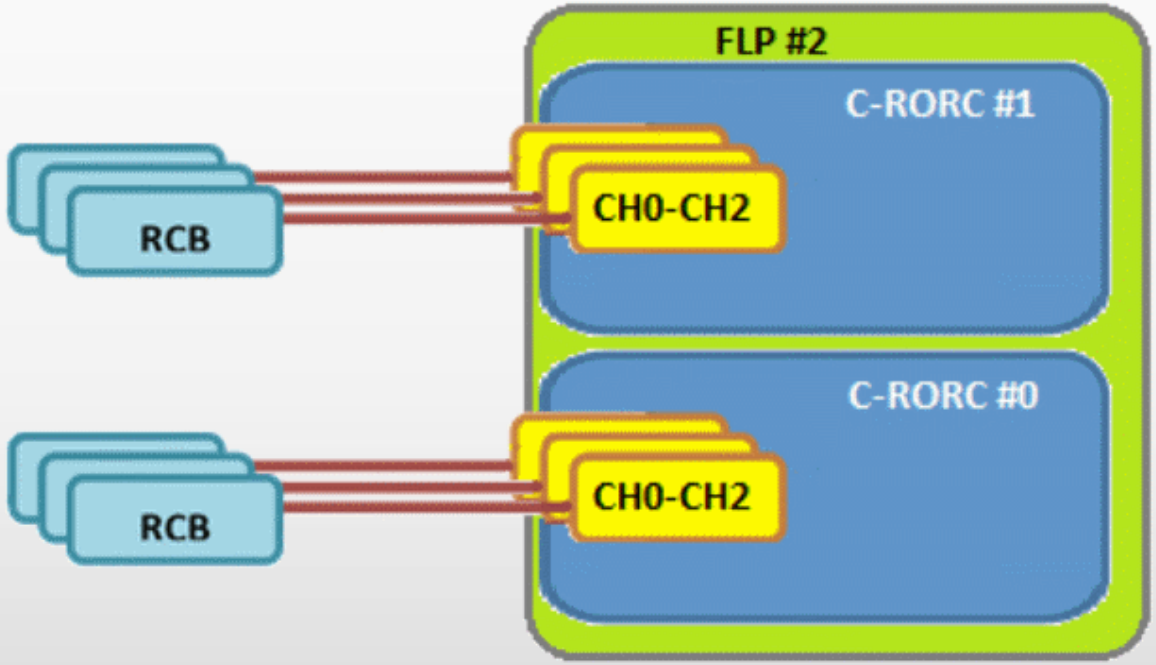
- Up to 6.25 Gb/s optical data links (12x)
- 600 MB/s maximum bandwidth per channel
- 4 000 MB/s, max. aggregate data throughput
- Complies with CERN proprietary Detector Data Links (DDL1, DDL2) w/ appropriate firmware
- Custom designed daughter boards with FMC interface

http://www.cerntech.hu/products/5-crorc.html

Total 14 link, 2 FLP



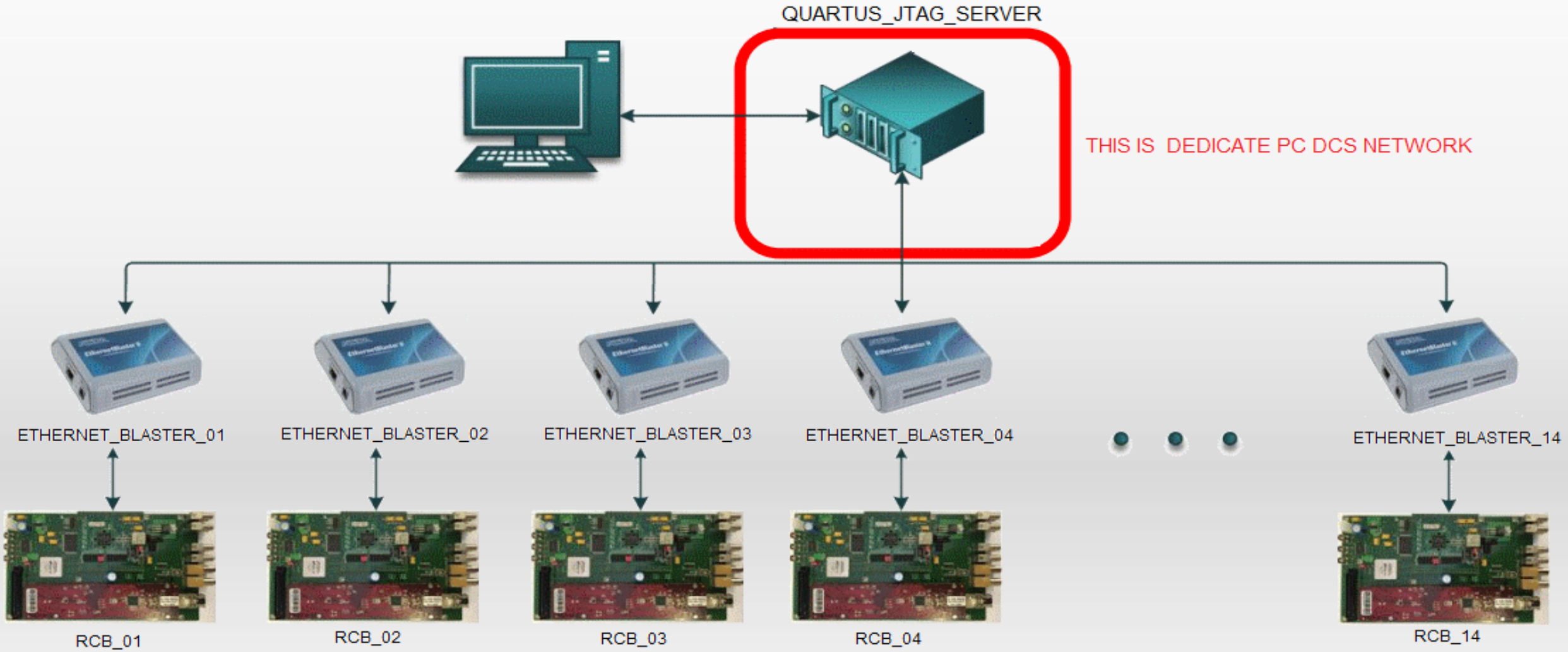
Total 8 link



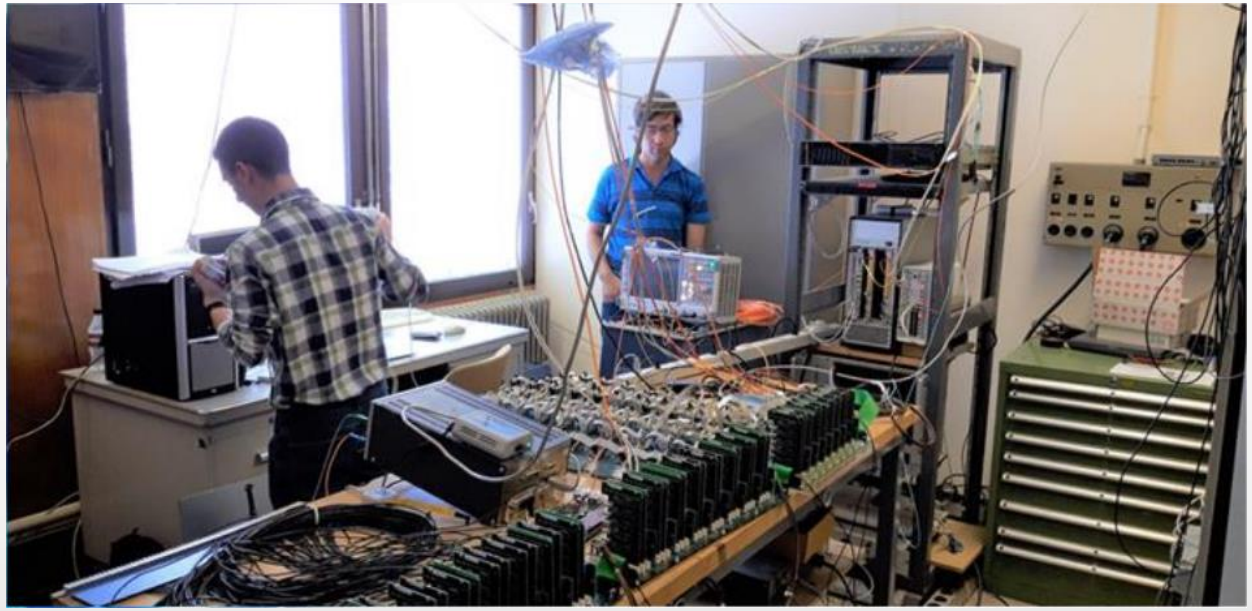
Total 6 link

- Remote Firmware update
- Signal analyzer
- Virtual JTAG for control and status

- CRAM error check ability
- Boundary scan (CRC_ERROR pin)
- Reboot the FPGA from flash



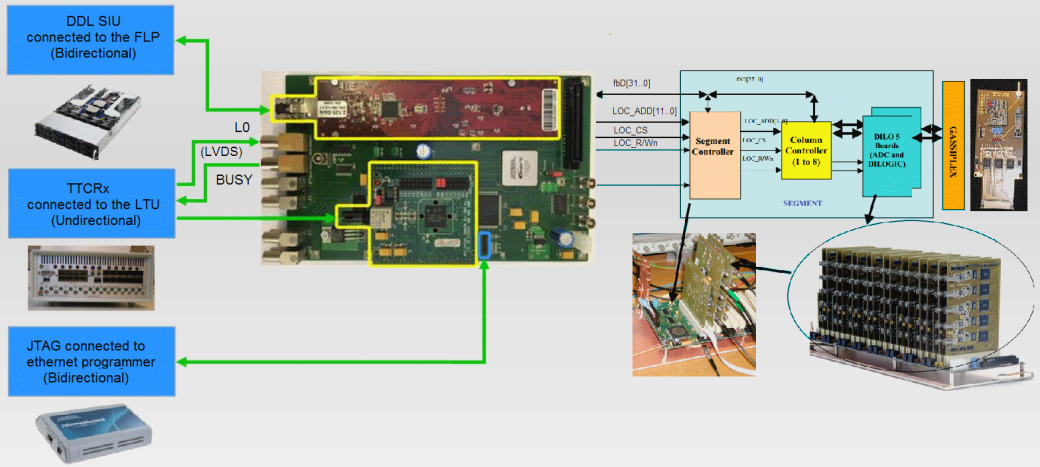
Test-bench in the LAB581 at CERN, any develop and test is done in this installation before move it to P2



Half Equipment:

- 1 RCB
- 3 SEGMENT, 24 columns

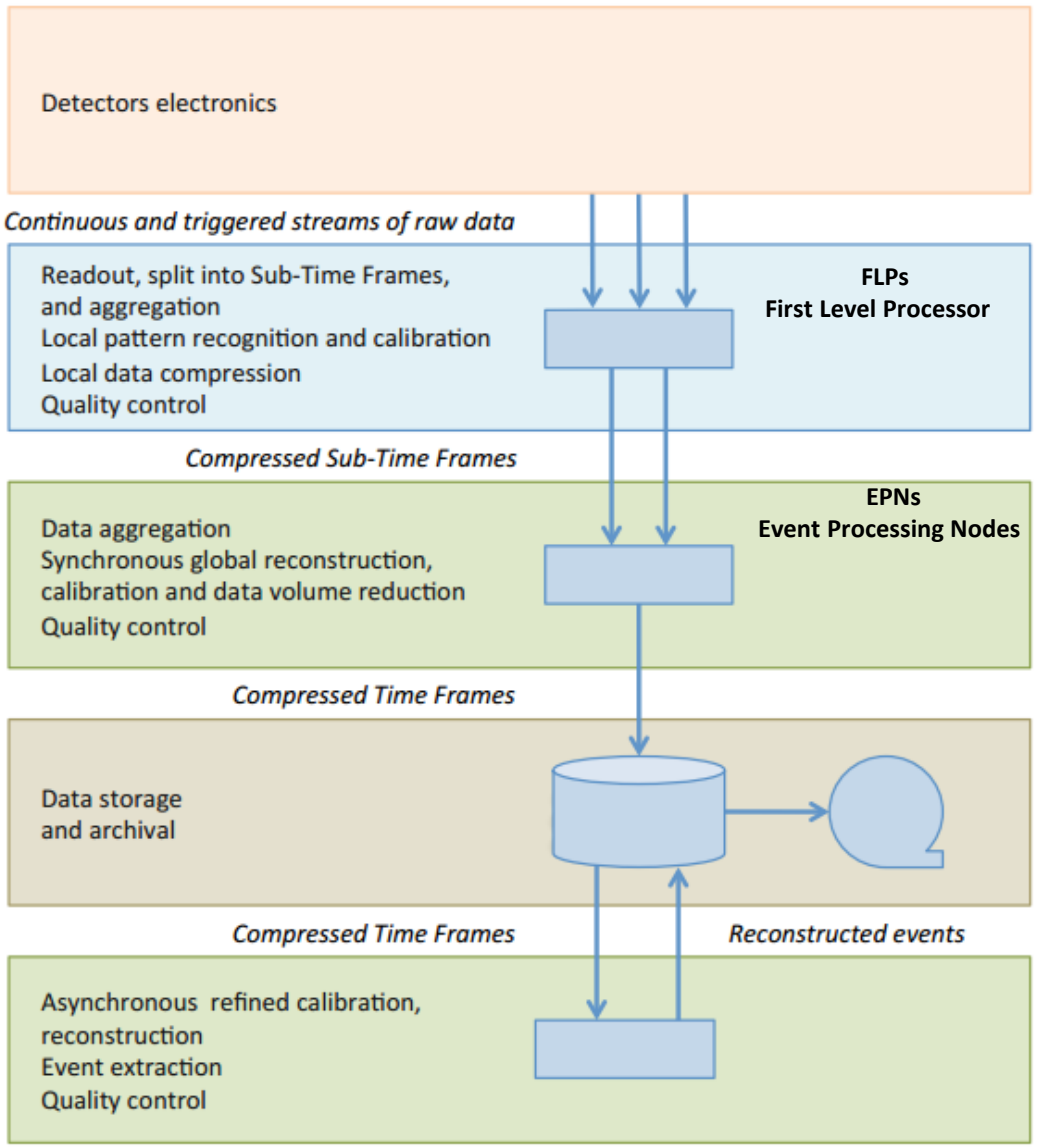
- 1 FLP
- 1 LTU
- 1 TTCex



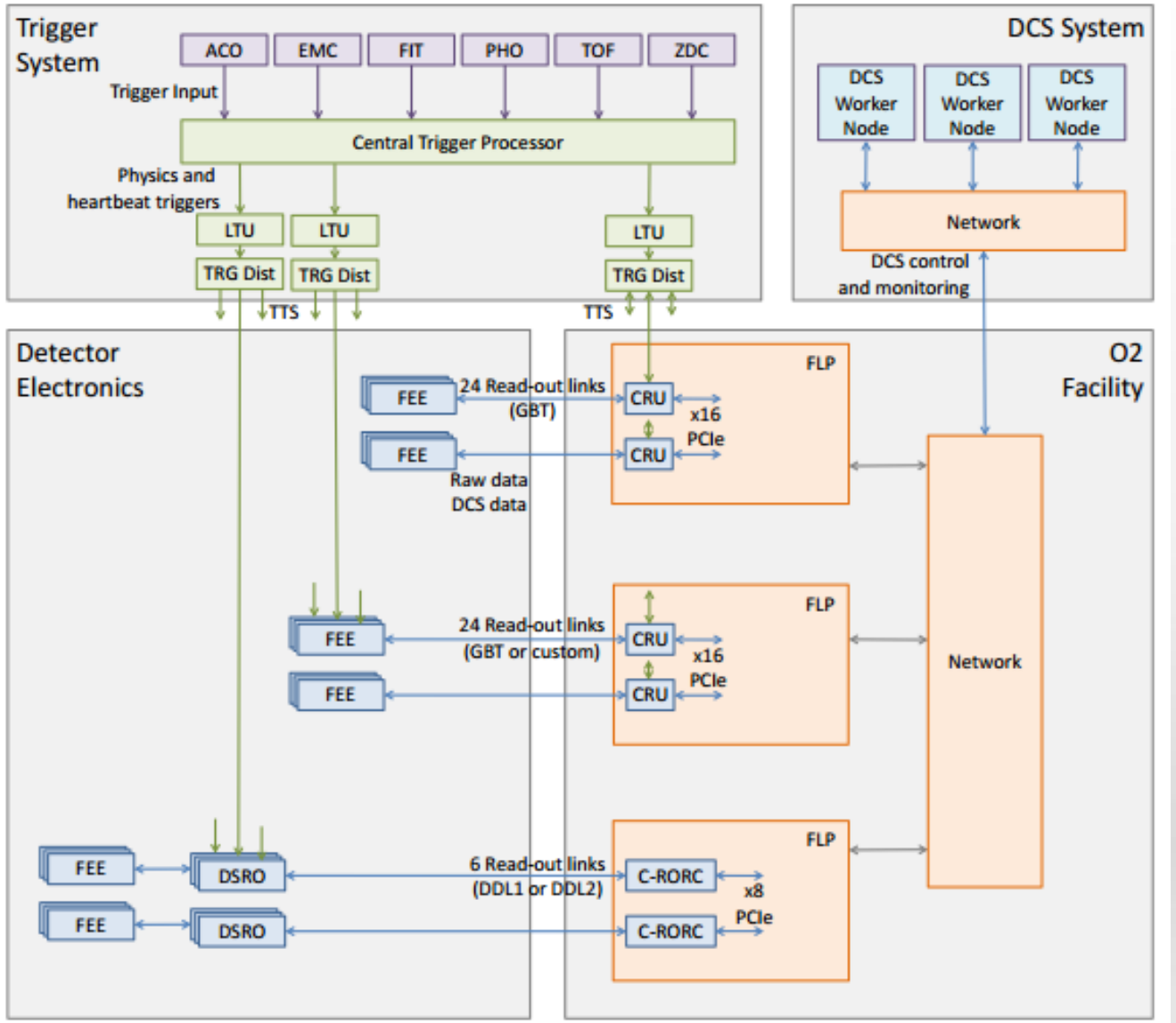
Develop Tools:

- QUARTUS II 10.1
- Ethernet Blaster JTAG

Remote access.



Functional flow of the O^2 computing system



Detector read-out and interfaces of the O^2 system with the trigger, detector electronics and DCS

The aim of this upgrade is to cope with the High Luminosity LHC period during Run 3, 2022-2024.

Collision rates of the order of 50 KHz in Pb-Pb and 200 KHz in pp respectively, are expected during the period

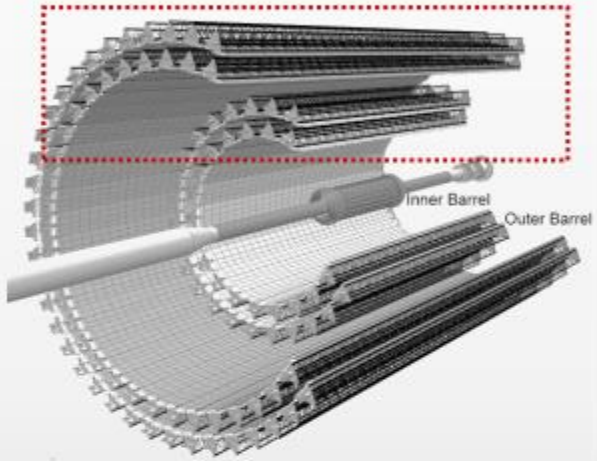
Improvements and work already done:

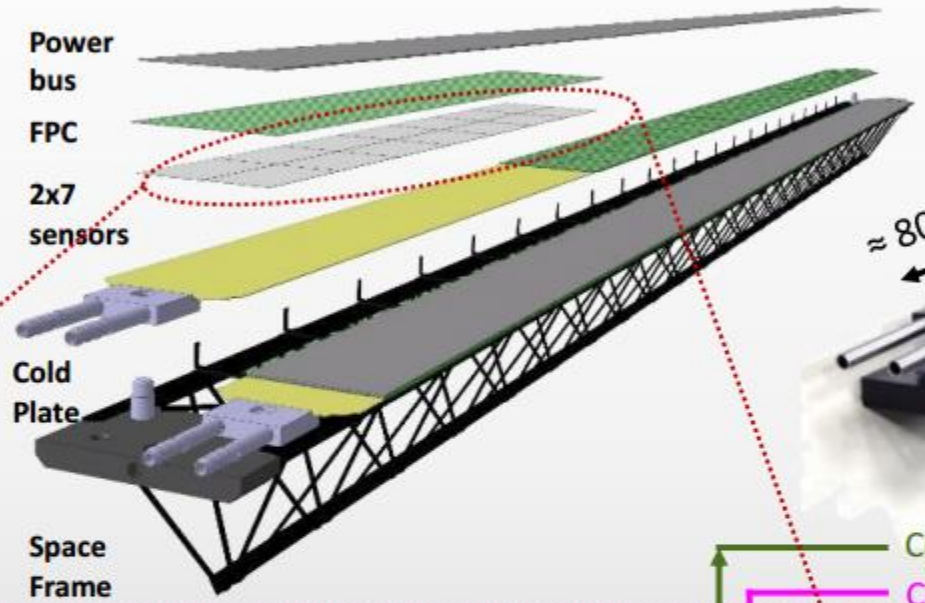
- Translated and optimized the old readout firmware (RO FW) developed in AHDL to a VHDL implementation.
- Implemented a new clock generation and distribution in the Readout Common Board (RCB)
- Improved the read out data transmission time
- Provided the RO FW with an enabling/disabling mask to exclude failing electronics columns
- Implemented a new control channel using a bidirectional JTAG communication.
- Developed command lines utilities and shell scripts for the configuration and read out of raw data from C-RORC cards used in the O^2 framework of ALICE and interfacing the HMPID via optical links.

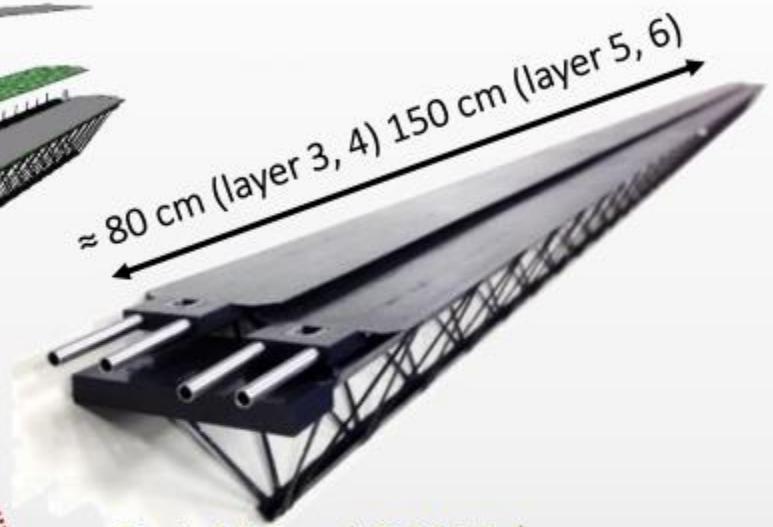
All the improvements and work have already resulted in

- An event read out rate up to 15 KHz in pp and 8KHz in Pb-Pb collisions respectively, three times higher than in Run2
- Very successful VS tests. Full chains up to EOS with QC in FLP and EPN confirmed.

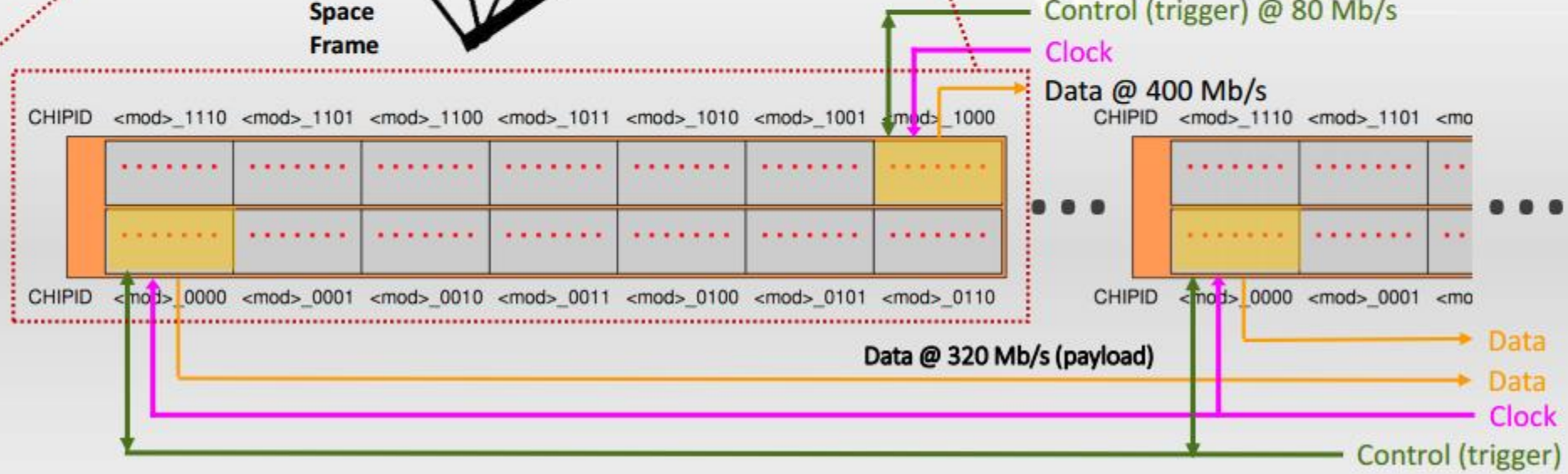
Mid/Outer layers module: 2 symmetric groups of **1 master** and **6 slave** chips. Only the master accesses the data/control and clock lines toward/from the outer world. Bandwidth (per master) is **400 Mb/s** (320 Mb/s payload).







Layer	Modules per stave	Length [cm]
3, 4	8	70
5, 6	14	150

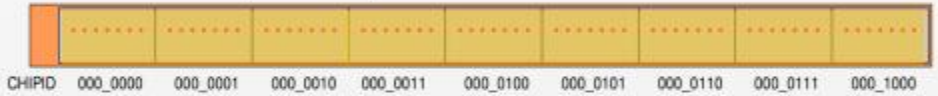


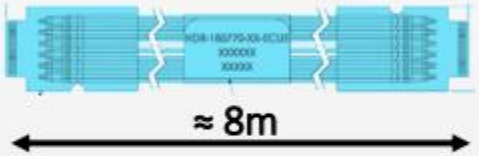
FEE – Connection to the detector – RUs and PBs pairing

Each Readout Unit is connected to a stave (1:1 pairing through the whole ITS, 192 RUs in total) through copper cables (almost 8m long), which carry both bidirectional control lines (40 MHz, 80 Mb/s) and unidirectional clock and data lines (400 Mb/s outer layers and 1.2 Gb/s inner layer). Power Boards can either power a single stave (outer layers) or two staves (middle layers).

Inner Layers

9 data lines, 1 clock, 1 control



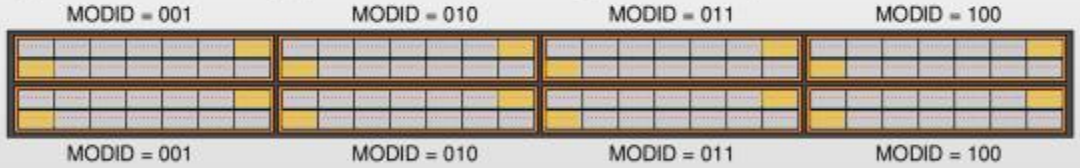


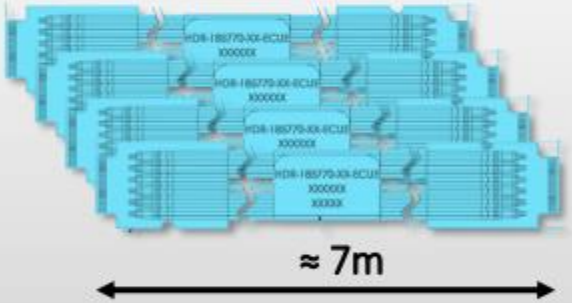
1 Readout Unit

½ Power Board, 1 ch

Middle Layers

(4+4+4+4) data, (1+1+1+1) clock, (1+1+1+1) control



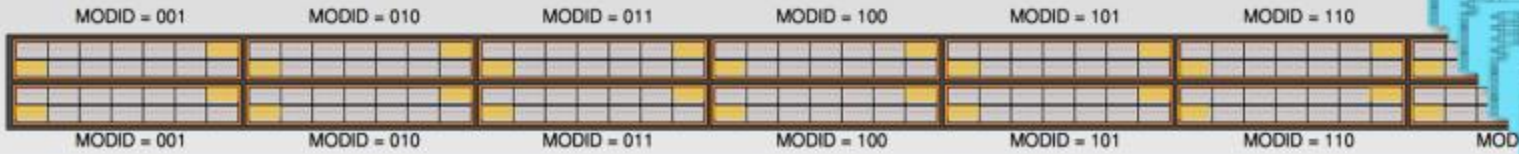


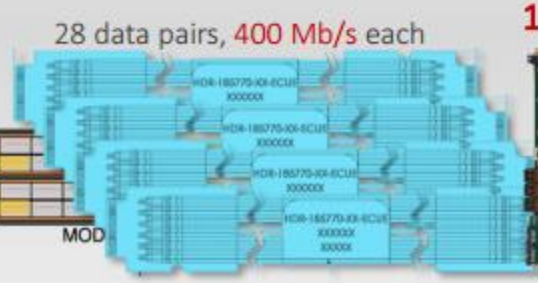
1 Readout Unit

½ Power Board, 8 ch

Outer Layers

(7+7+7+7) data, (1+1+1+1) clock, (1+1+1+1) control



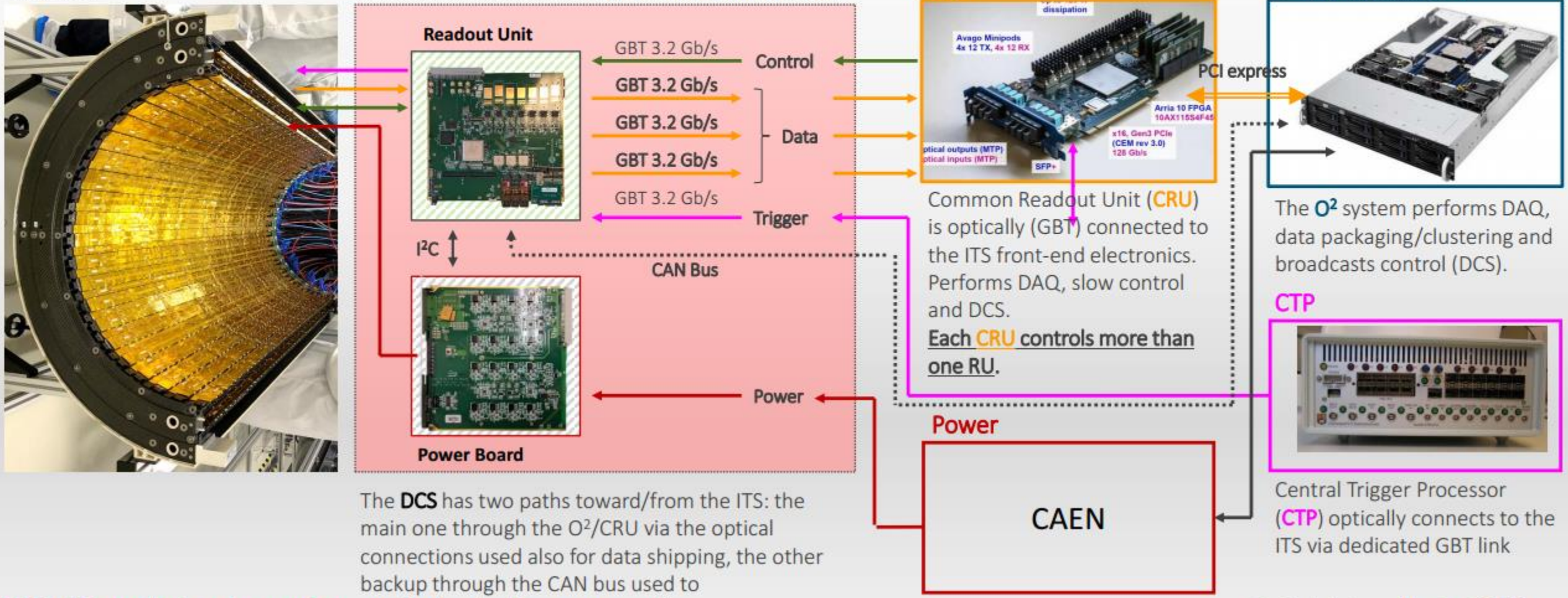


1 Readout Unit

1 Power Board, 16 ch

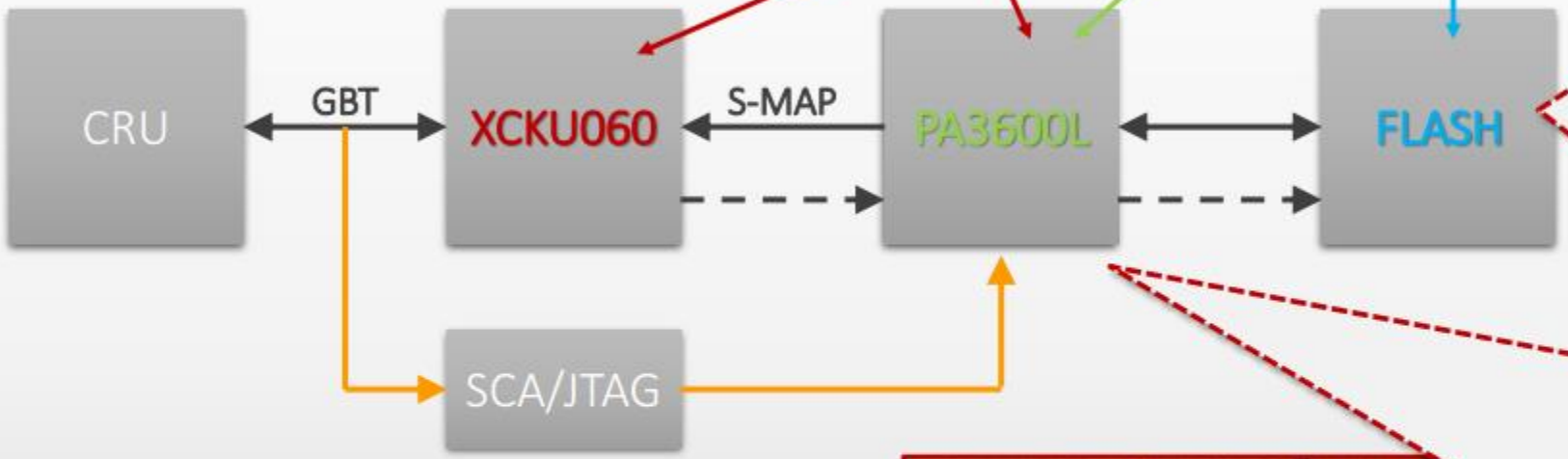
FEE – Actual system implementation

- The ITS Front End Electronic (FEE) is divided into modular **Readout Units (RU)**, identical for each layer.
- Each readout unit controls an entire stave, including power to the sensors (through custom-made **Power Boards**).
- The experiment DAQ, Trigger and Control interfaces with the RU only through the Common Readout Unit.



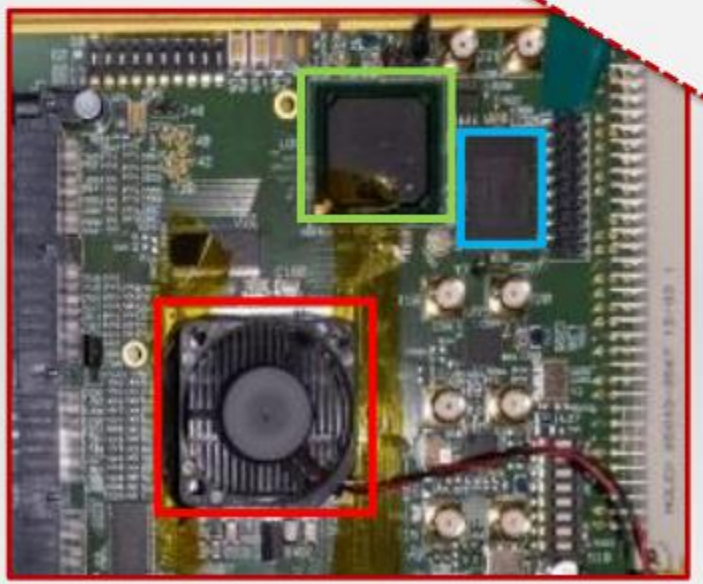
Radiation tolerance – scrubbing subsystem

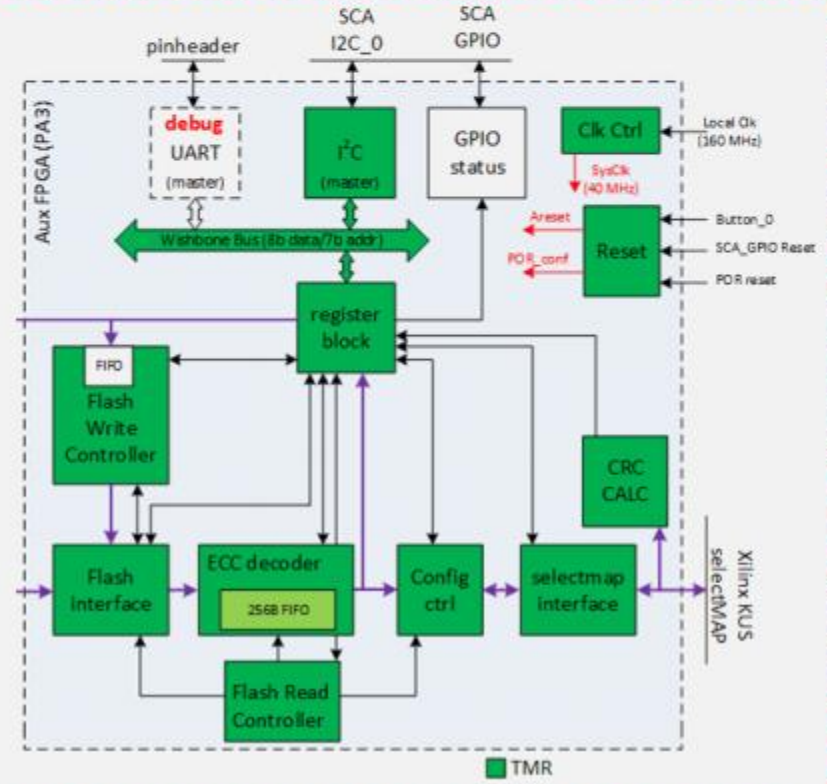
While some SEU cannot be avoided (clock resources, IO facilities, etc. the vast majority happen in the CRAM, and can be actively manage by a combination of **TMR design**, **scrubbing** and **ECC**.



XCKU060 **boot image** + the **scrubbing image (about 50 Mbyte in total).** Scrubbing image is:

- 0/1 inverted to lower the FLASH cross-section (0→1≈10^{-16} cm^2, 1→0≈10^{-21} cm^2).
- ECC added at the end of every frame.
- Actually 2 copies stored in parallel.

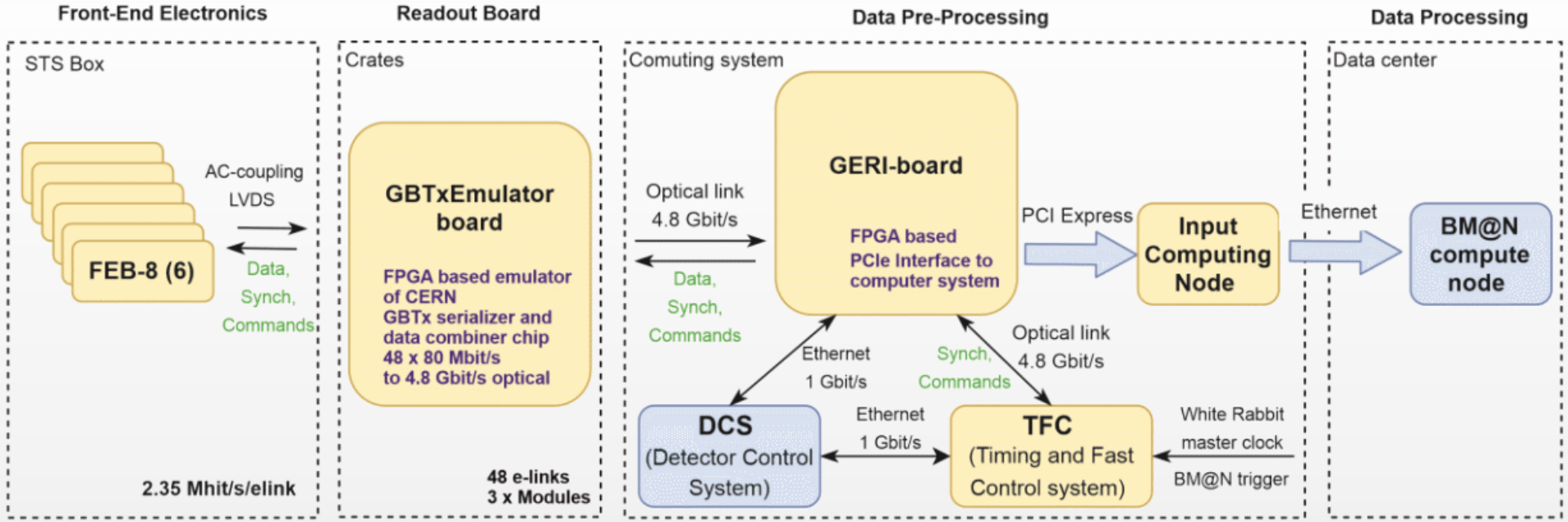




Scrubbing features

- Continuous scrubbing of the main XCKU060 FPGA (**1.7s cycle**), TMR protected firmware and critical IOs.
- Completely controllable through the GBT/SCA channel (rad-hard path).
- Redundant firmware golden copy in FLASH, with ECC per-page correction.
- TMR blocks in PA3 firmware protects the firmware from transients.

Test bench base on BMN SiliconTracker DAQ



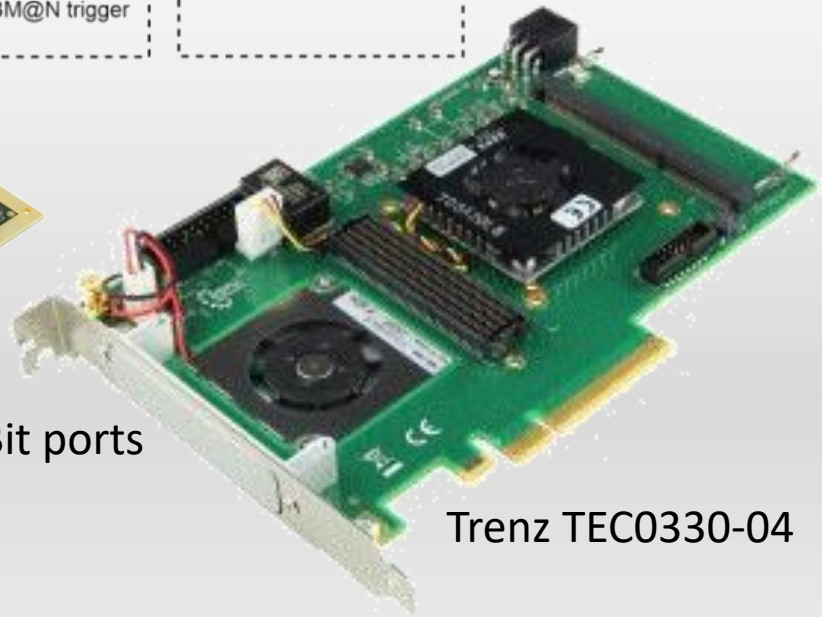
Trenz TE0712

connectivity for 6 FEB-8

GBTxEMU-3Sens Board

Trenz TEF0008

FMC Card with four SFP+ 10 GBit ports

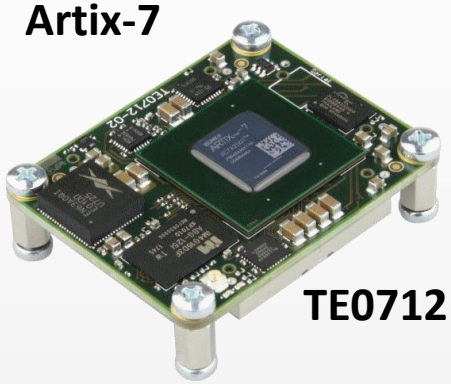


Trenz TEC0330-04

https://indico.gsi.de/event/10807/contributions/45364/attachments/31931/41993/BMN_SiliconTracker_DAQ_01.07.2020.pptx

Trenz Electronic SoMs with 4 x 5 cm form factor

Artix-7



TE0712

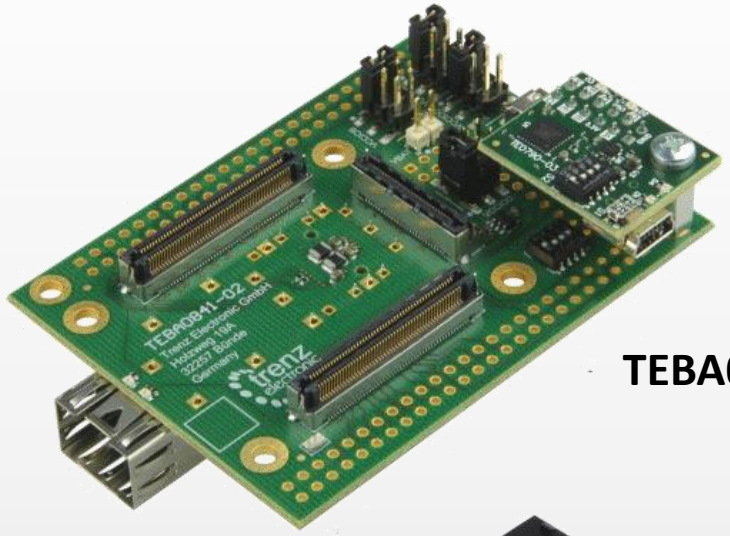
Kintex-7

TE0741

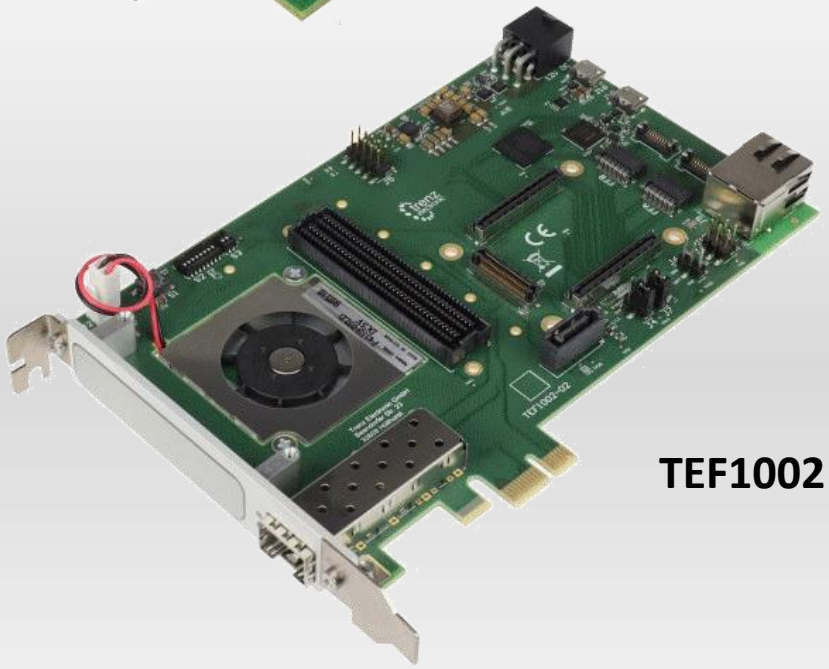
Kintex UltraScale

TE0841

Carrier boards for SoMs with 4 x 5 cm form factor



TEBA0841



TEF1002

Possible contribution to MPD-ITS

- Share the experiences from the firmware development for ALICE-HMPID.
- Collaborate on the design and construction of a test bench based on GBT protocol.
- Participate on the integration of the detector to the DAQ system.
- Development and test of FPGA firmware's.
- Development of the application for controlling and reading the detector (C, C++, Python or Labview).

Thank you !

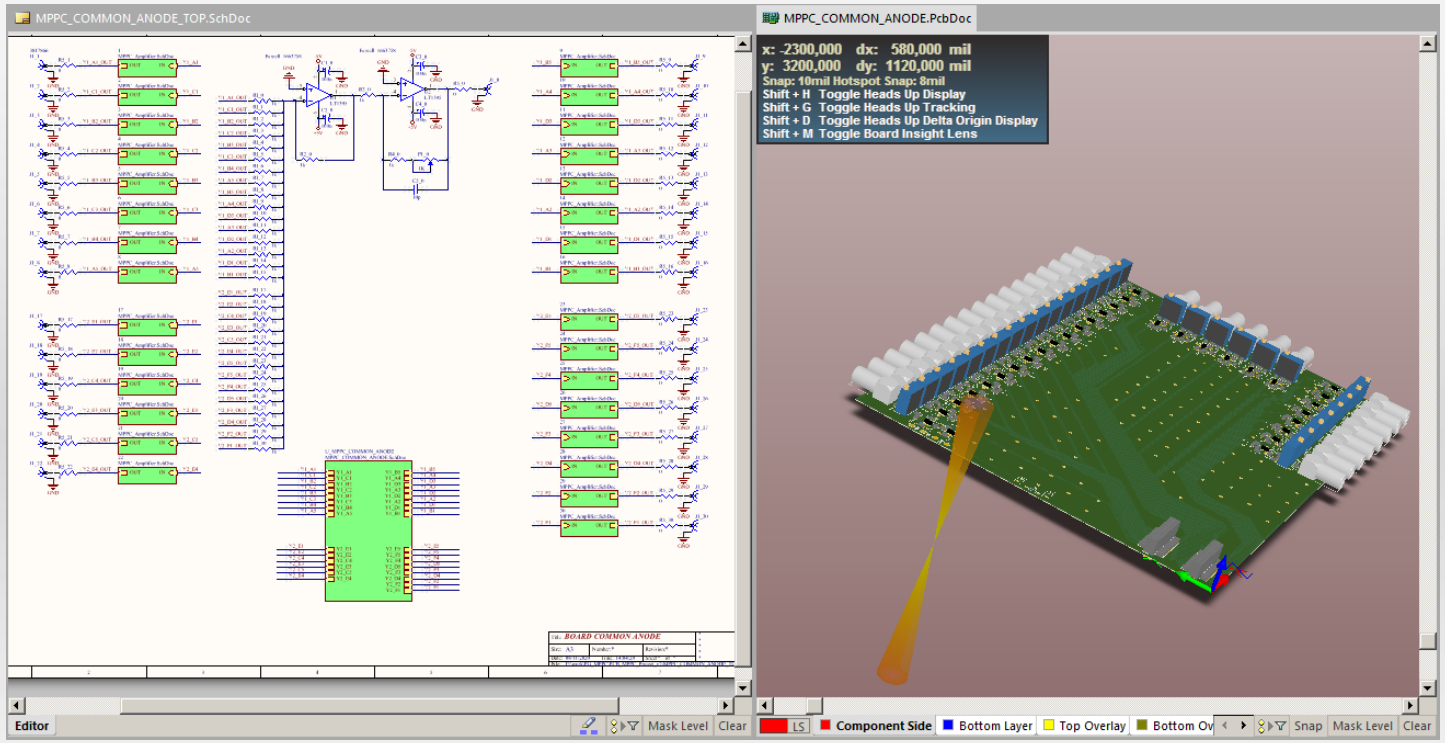
Backup Slides

Developed two analog readout board to a MPPC silicon photomultipliers for a characterization of a ΔE-TOF detector prototype for the FOOT experiment

Jan 2018 – Apr 2018 , **INFN Torino**

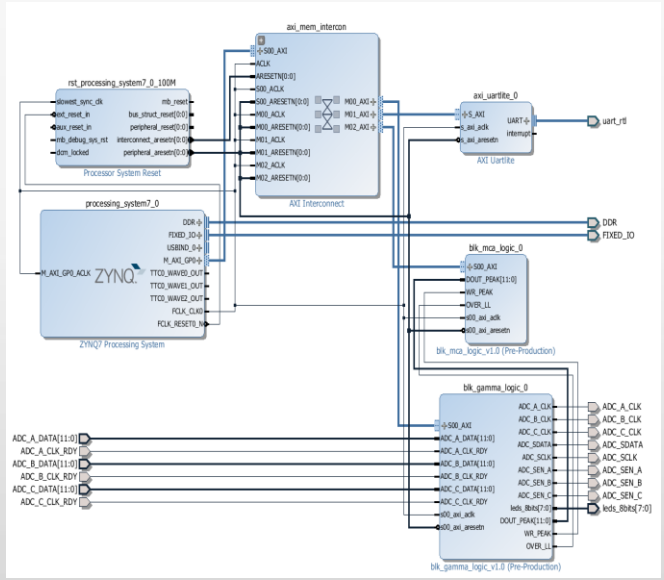
Development of two analog readout board to a MPPC silicon photomultipliers for a characterization of a ΔE-TOF detector prototype for the FOOT (**F**ragmentati**O**n **O**f **T**arget) experiment. The final ΔE-TOF detector will be composed of two layers of plastic scintillator bars with orthogonal orientation and will measure, for each crossing fragment, the energy deposited in the plastic scintillator (ΔE), the time of flight (TOF), and the coordinates of the interaction position in the scintillator.

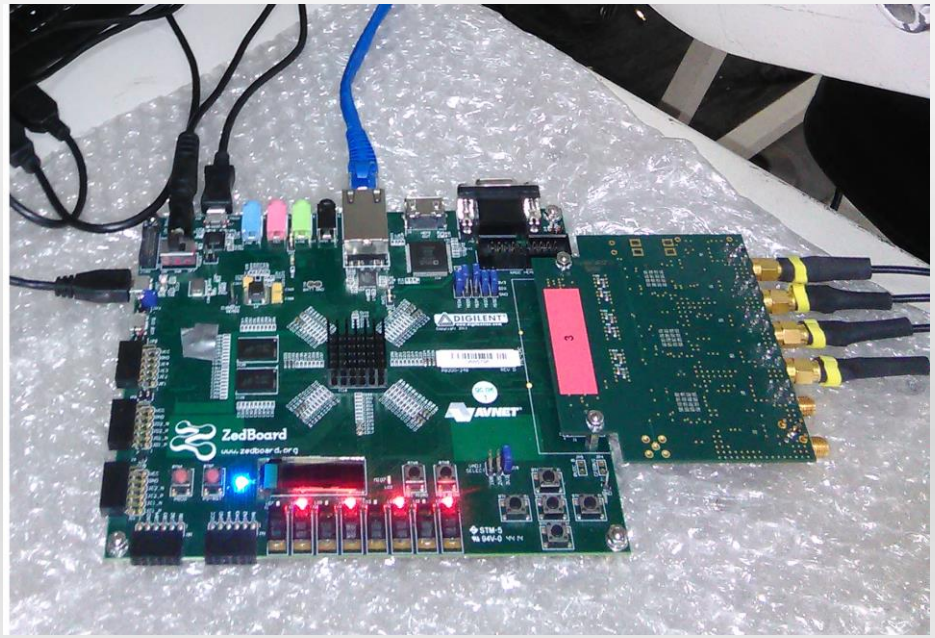
https://doi.org/10.1016/j.nima.2018.09.086

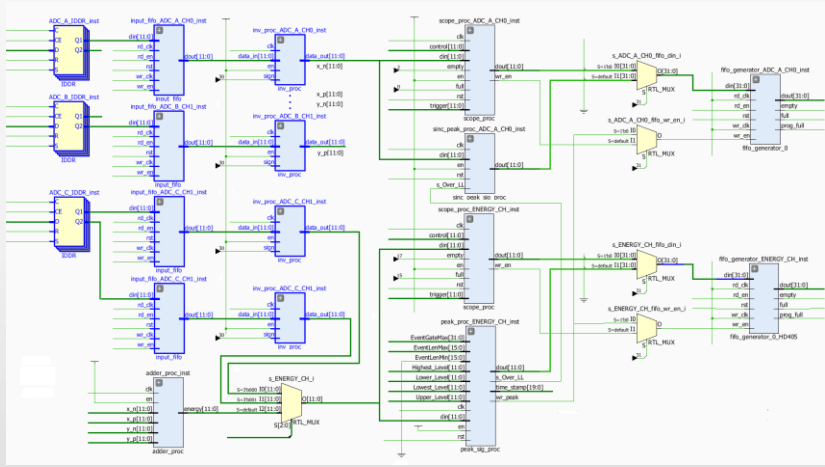


Developed a firmware for ZYNQ device base on FreeRTOS/lwIP libraries for a Prototype of Gamma Camera acquisition system
Jan 2017 – Jul 2017 , **CEADEN, Cuba**

The aim of this project was to develop the firmware for a ZYNQ device, based on FreeRTOS/lwIP libraries. The purpose of the firmware was to implement the Ethernet communication between the acquisition system and the PC. The system is used for the refurbishment of Gamma Cameras in the Cuban public health system.

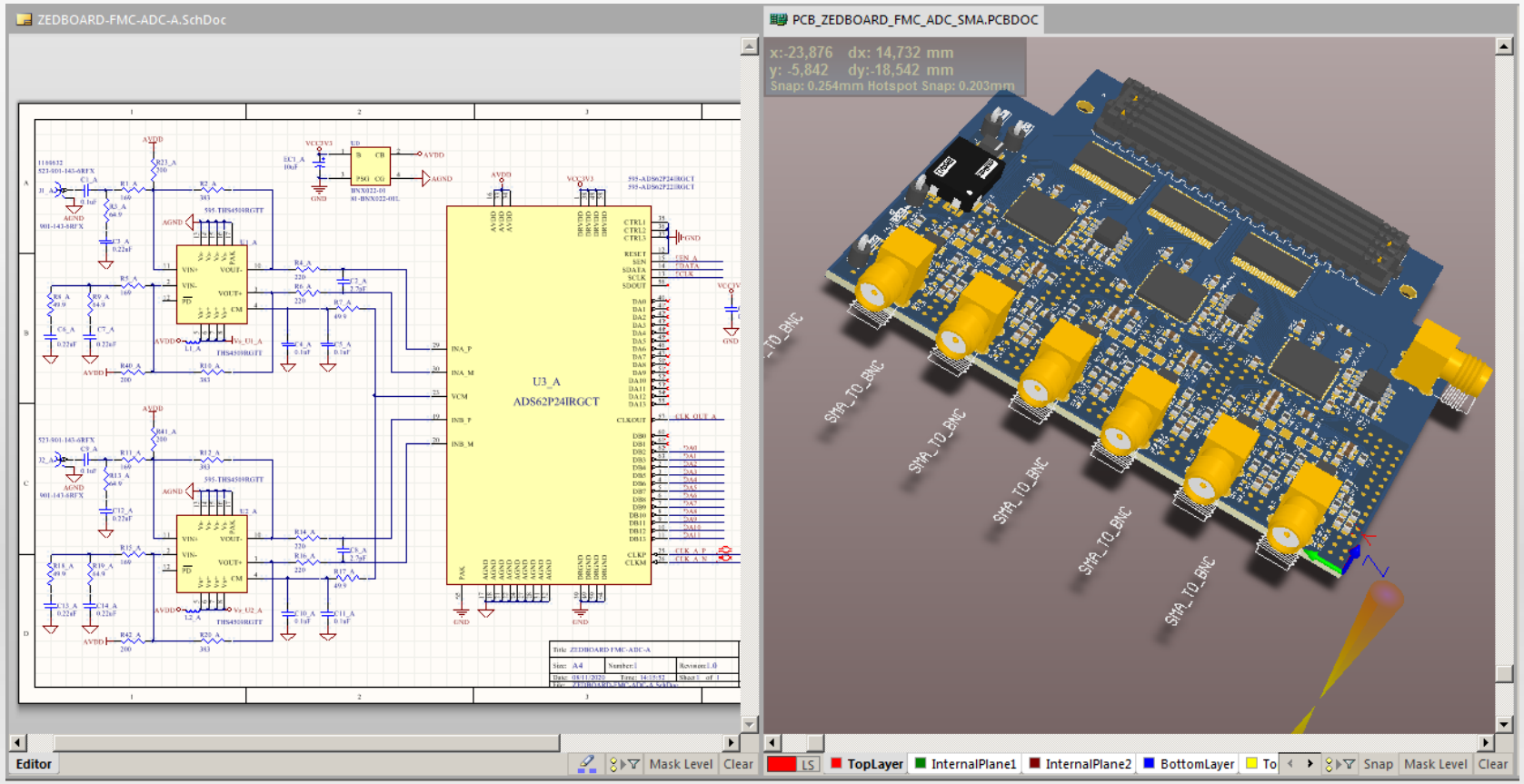






Developed an FMC board with six 14bits ADC channel at 65MS/s.
Jan 2016 – Jun 2016, **Forschungszentrum Jülich GmbH, Germany**

Design of an FPGA Mezzanine Card (FMC) with six 14bits ADC channels at 65MS/s to be interfaced with the Digilent ZedBoard. The acquisition board was developed to be used in the refurbishment of Gamma Cameras in the Cuban public health system.



Developed to the project SoLiδ a Matlab/Simulink Testing and Simulation Framework
Aug 2015 – Oct 2015, **University of Antwerp, Belgiun**

Setup a Matlab/Simulink framework to test and simulate neutron trigger algorithms based on a trapezoidal filter for pulse shape discrimination using FPGA. The development permitted "rapid setup and a viable implementation in hardware" in the context of the Solid project.
https://www.uantwerpen.be/en/rg/particle-physics-group/research/solid-experiment/

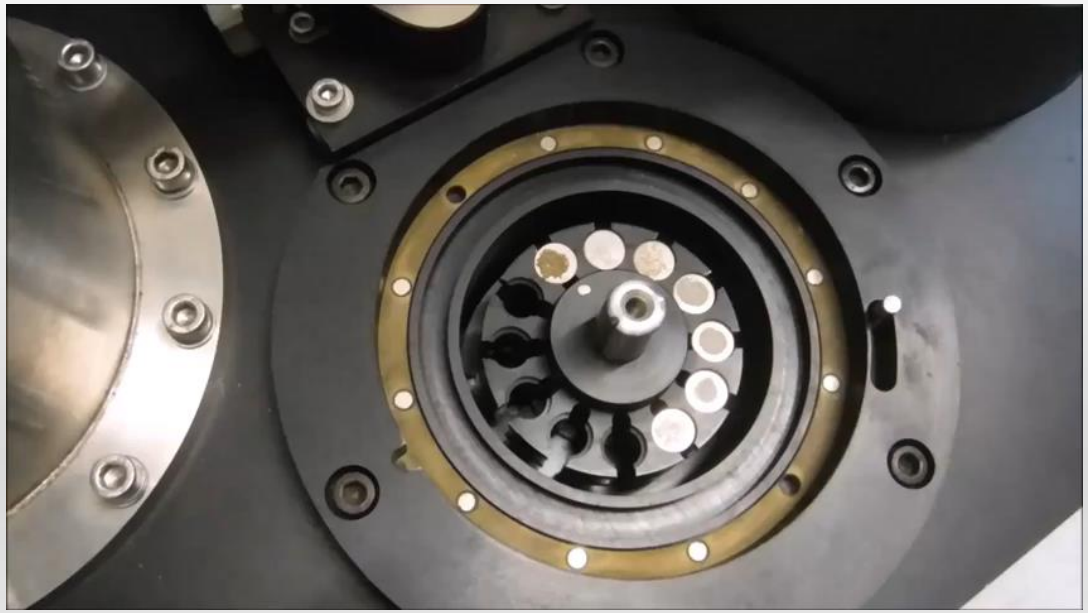
Developed a step motor controller control the positioning of the detection system of Radioactive ion beams in Brazil
Jun 2013 – Oct 2013, **Institute of Physics of the University of São Paulo (IFUSP)**

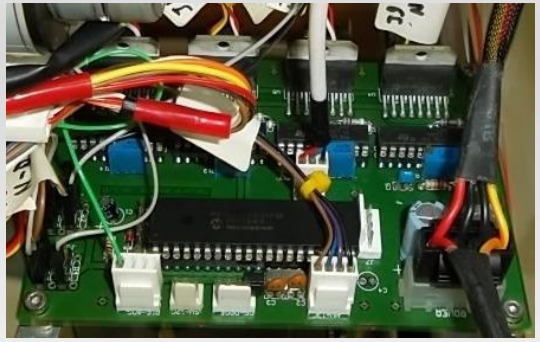
A step motor controller was developed in order to control the positioning of the detection system in the scattering chamber (chamber-3) of the RIBRAS project. The RIBRAS-SMC is a small board, based on the microcontroller PIC18F4550, capable of control four Step Motors and eight optic micro switches. The board is controlled through the USB using the driver libusb, the use of this driver allow as establish the communication in Linux or Windows. In this case all the communication was implemented using USB control transfer and custom vendors request commands.
http://www.academia.edu/1130658/The_RIBRAS_facility

Developed the electronic part of an optically-stimulated luminescence reader for dating applications.

Jan 2011 – Mar 2013, **CEADEN. Cuba**

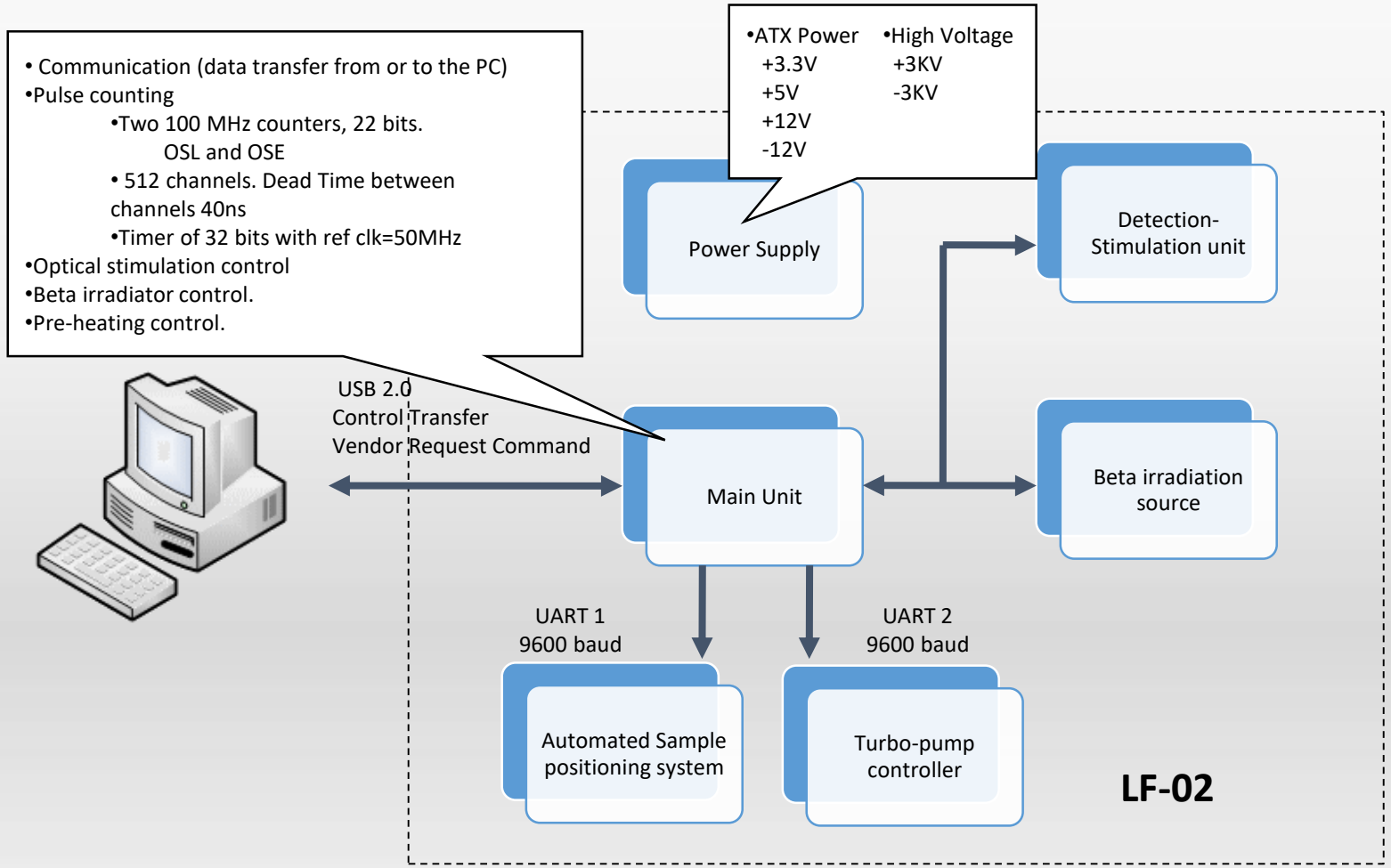
Optically Stimulated Luminescence (OSL) is a technique used for dating, several subsystems that operate in parallel are electronically integrated in the reader. In order to fulfill this requirement an instrument based in Xilinx FPGA technology and micro controllers was developed.



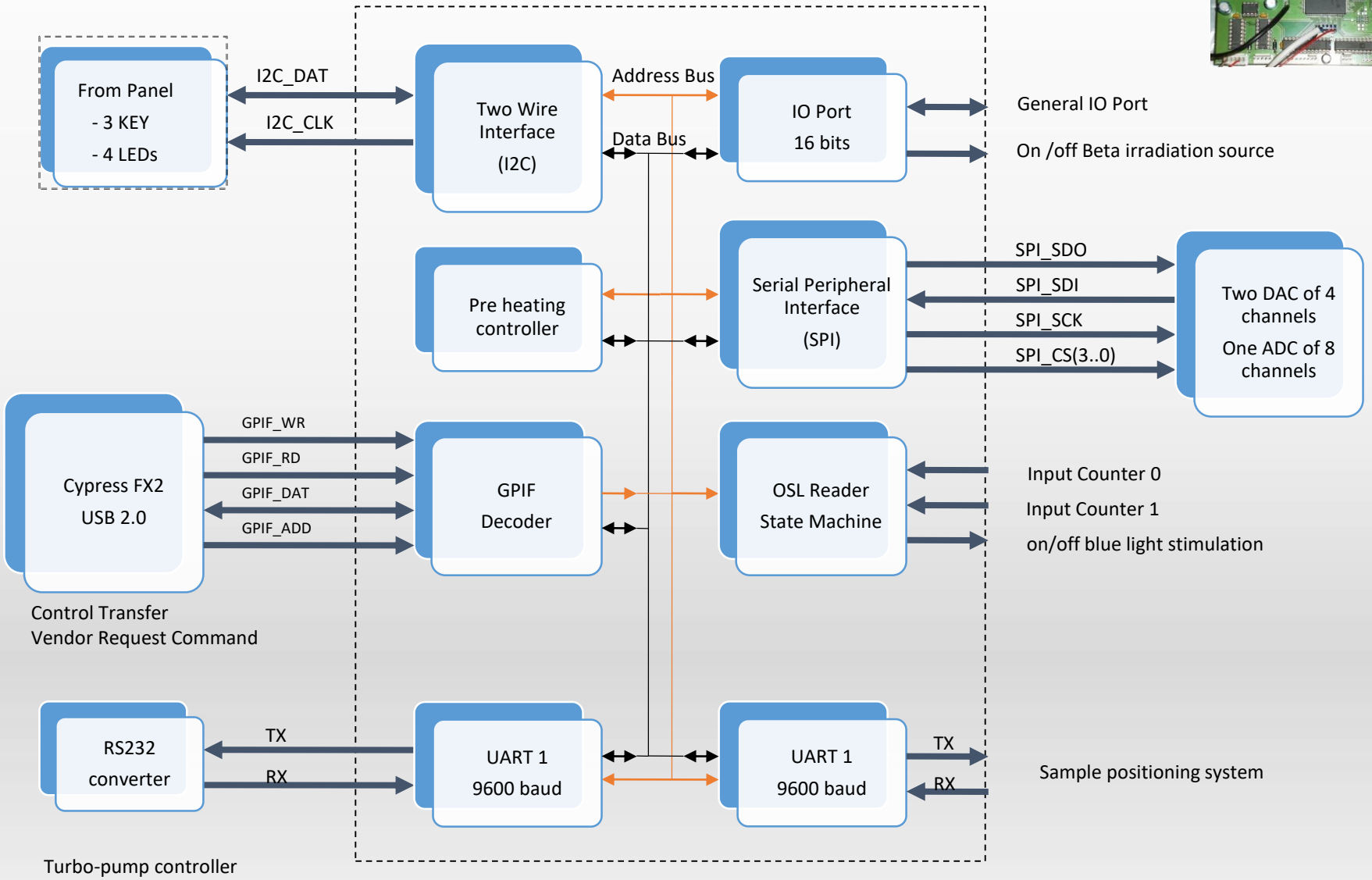


General diagram of the OSL reader

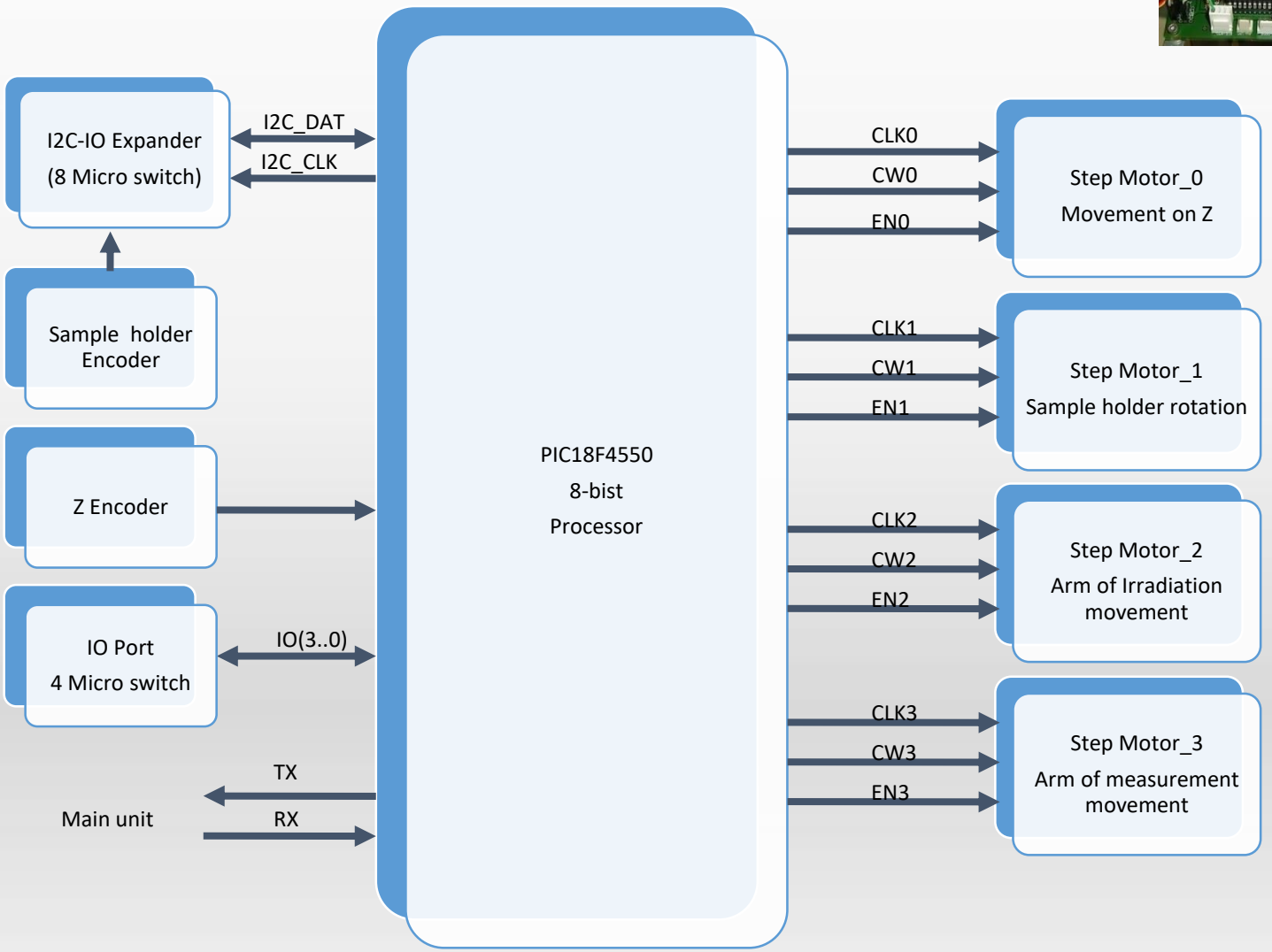
In practice this is accomplish if several subsystems that operate in parallel are electronically integrated in the reader



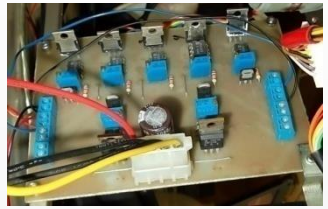
Main unit diagram.

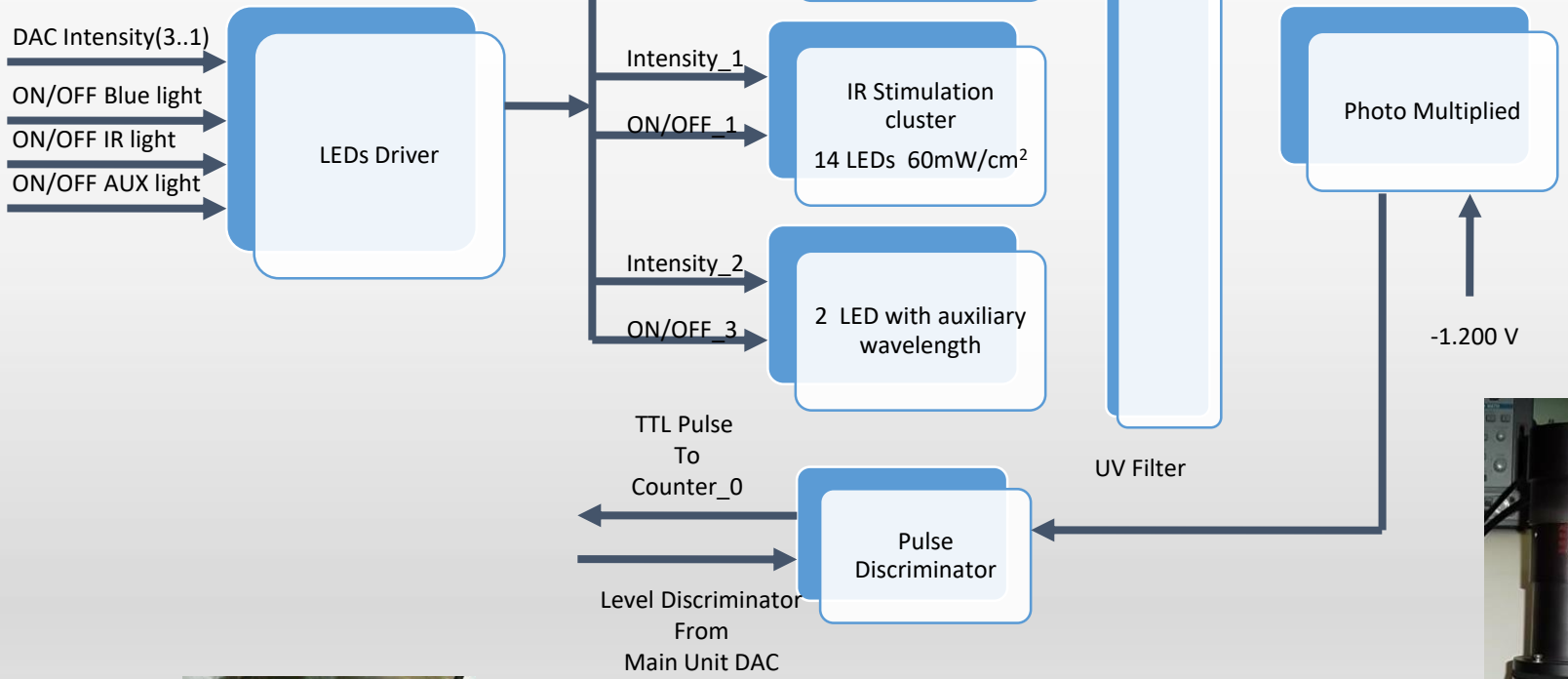


Sample positioning unit diagram.



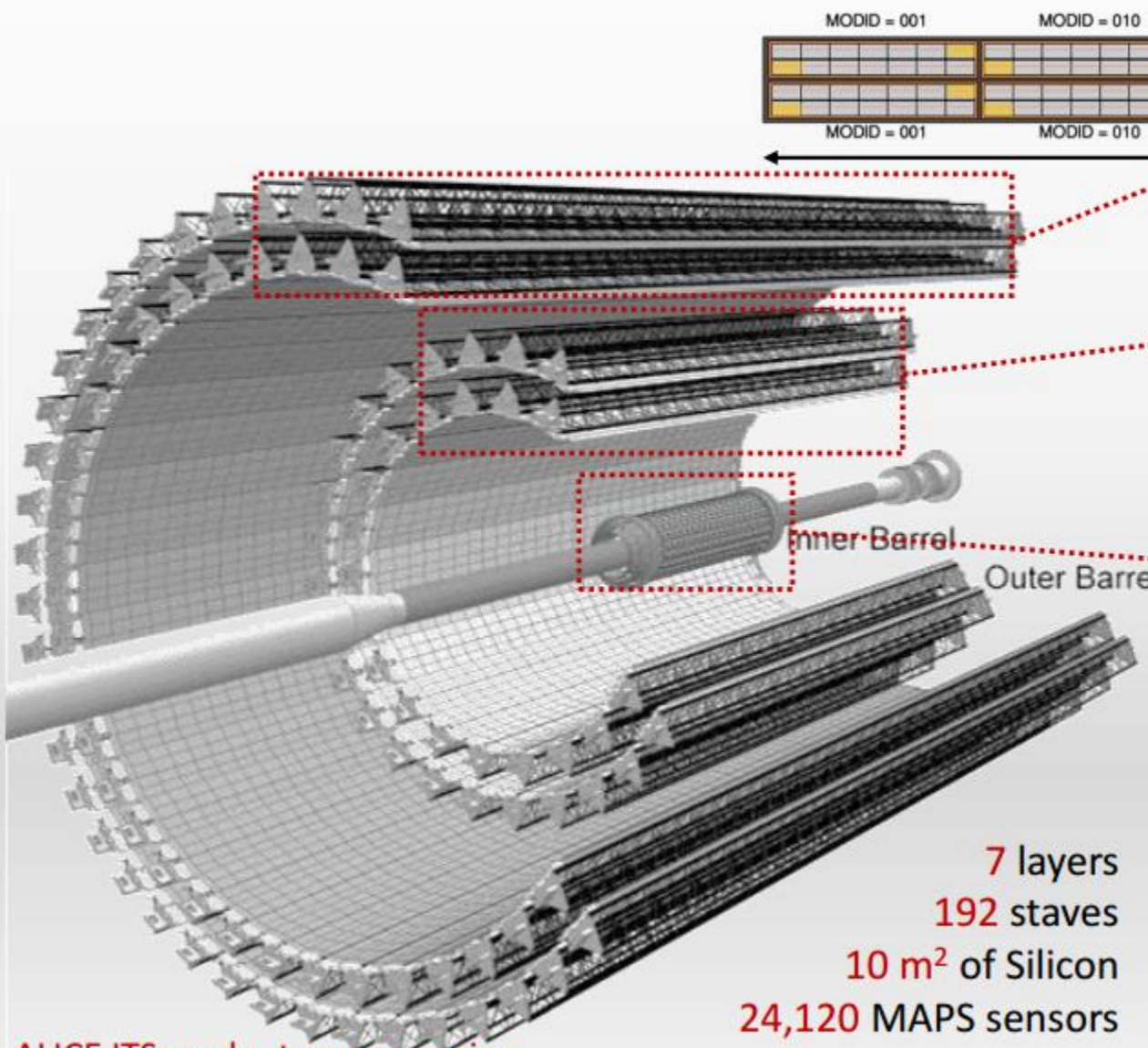
Detection-Stimulation unit.

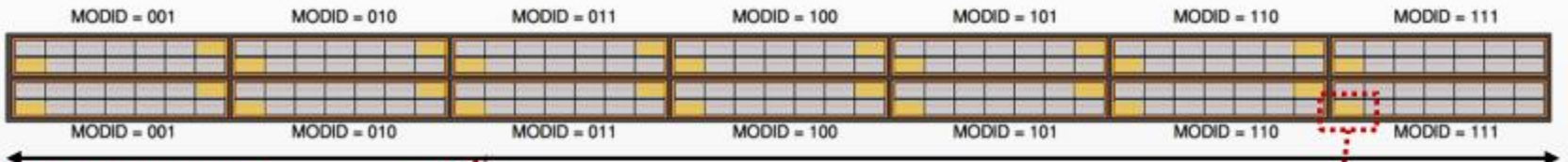


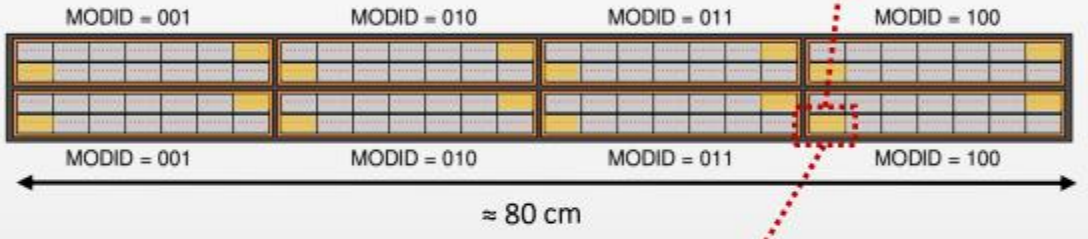


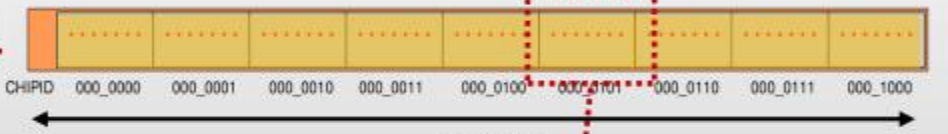
The ITS detector readout challenge

With the new ALICE ITS we face the problem of reading about **12.6 Gpixel** in the most power-efficient possible way.









7 layers
192 staves
10 m² of Silicon
24,120 MAPS sensors

The very same sensors is used to populate the entire detector.

ALICE ITS readout and powering

FEE – Connection to the detector – inner barrel

Inner layers stave, **9 master** sensors, each reads/drives a shared control/trigger (80 Mb/s) line and drives an individual high speed (**1.2 Gb/s**, 960 Mb/s payload) data line.