Forward Silicon Tracker and beam detectors

upgrade status

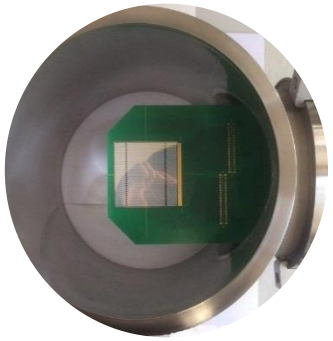
Bogdan Topko behalf on Forward Silicon Tracker team

7th Collaboration Meeting of the BM@N Experiment at the NICA Facility,
19 April 2021

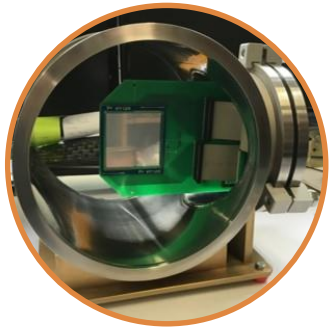
Contents

- Forward Silicon Tracker and beam detectors
- Beam profilometer
- Beam tracker
- Multiplicity trigger
- Front-end electronics test bench configuration
- FST Si modules test bench configuration
- Storing and analyzing measurement data solution
- FEE testing results
- Si modules testing results
- Summary

Forward Silicon Tracker and beam detectors

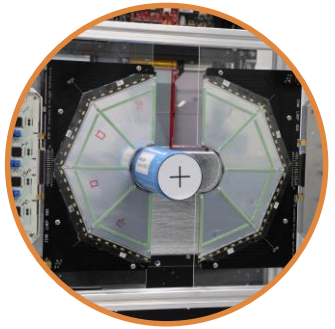


Beam profilometer x2



Beam tracker x3

Target

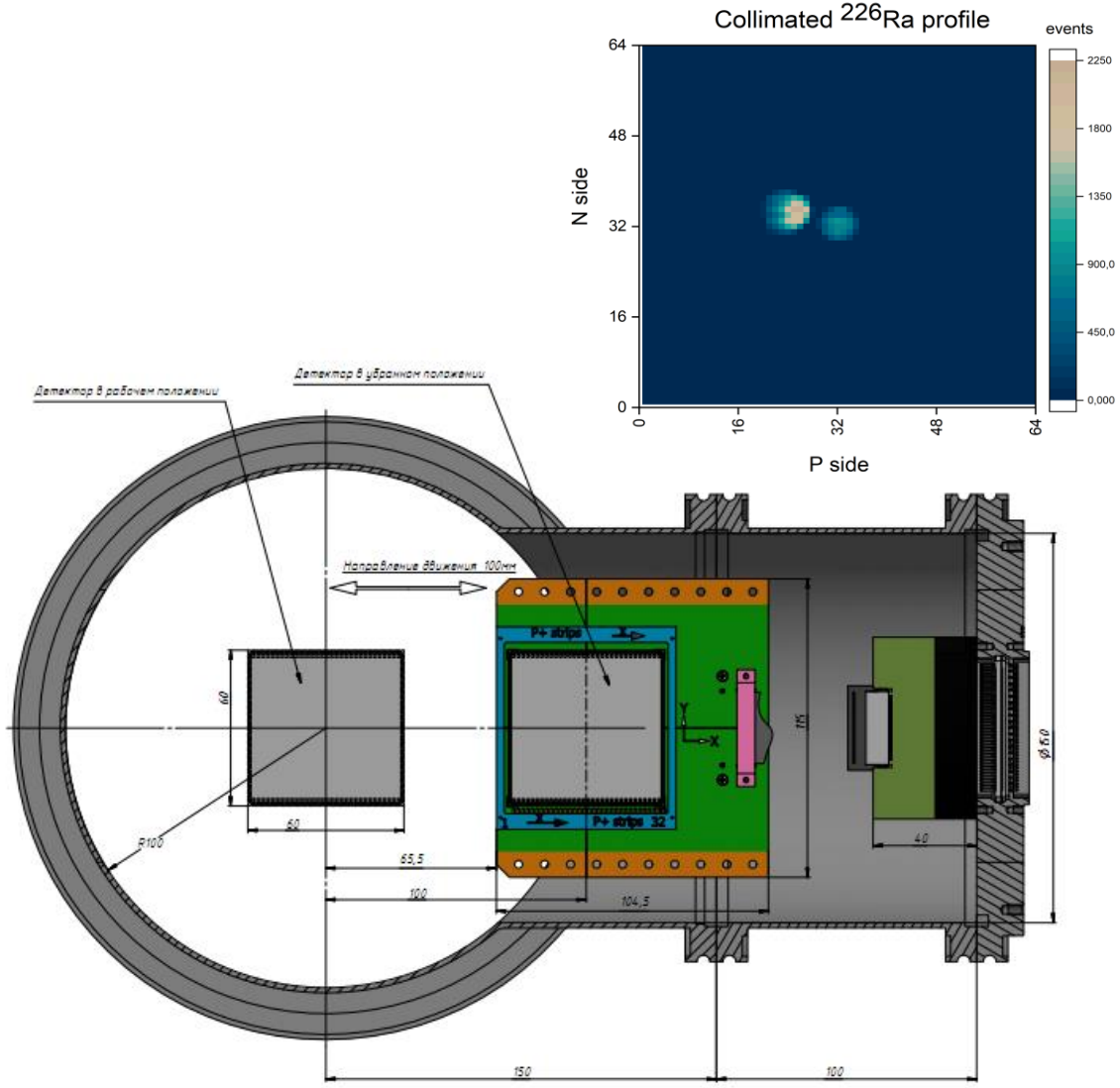


Multiplicity trigger

Forward Silicon Tracker x3

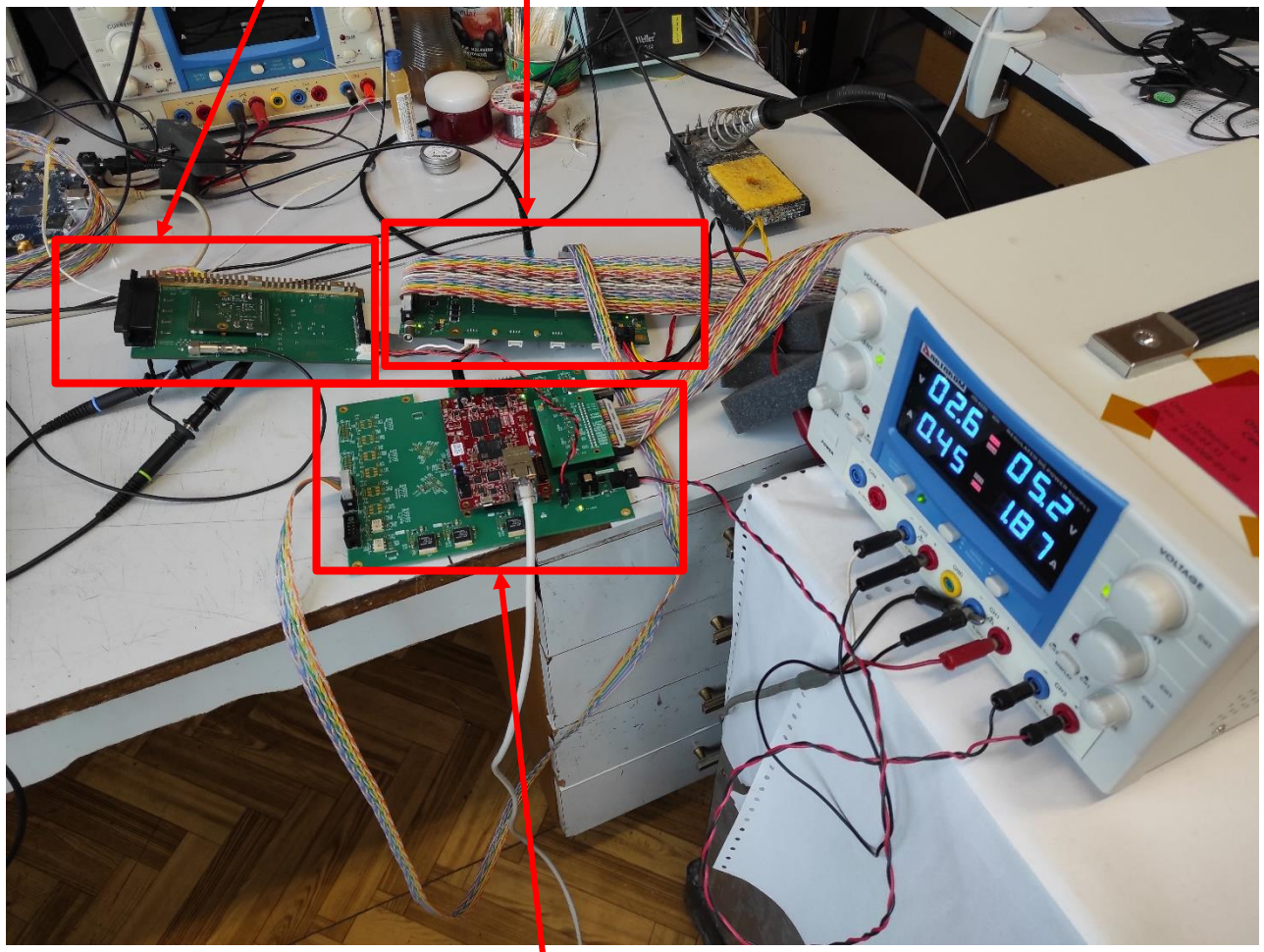
Direction of Ion Beam

Beam profilometer

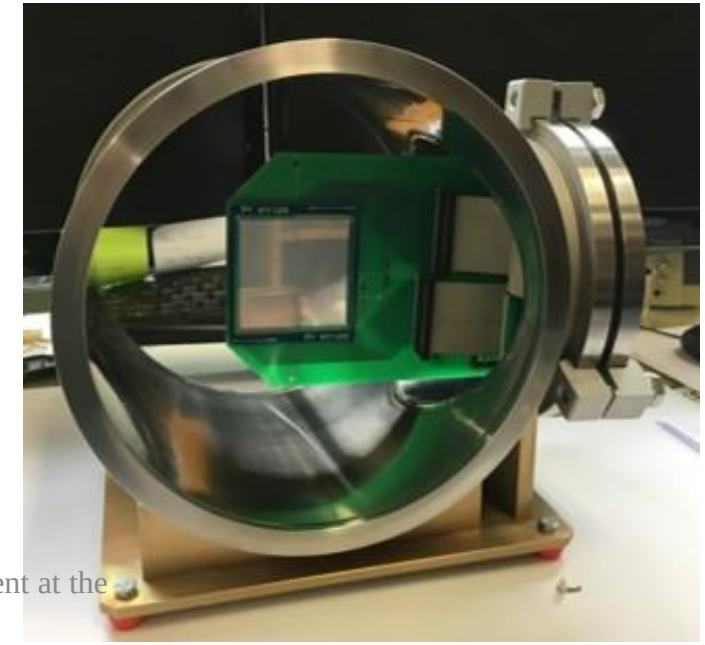


- **detector:** DSSD, 32×32 strips, pitch p+ / n+ strips 1.8 mm, thickness 175 μm, active area 60 × 60 mm^2;
- **mechanical design:** The mechanical construction supports automatic removal of profilometer planes from beam zone to special branch pipe after beam tuning;
- **FEE:** for light ions based on **VA163 + TA32cg2 (32 ch, dynamic range: -750fC ÷ +750fC)**;
- **current status:** two vacuum stations with flanges and cable connectors are ready, Silicon Detectors assembled on PCBs and tested with alpha-source (5.5 MeV), (**FEE+ADC+DAQ**) design in progress within schedule.

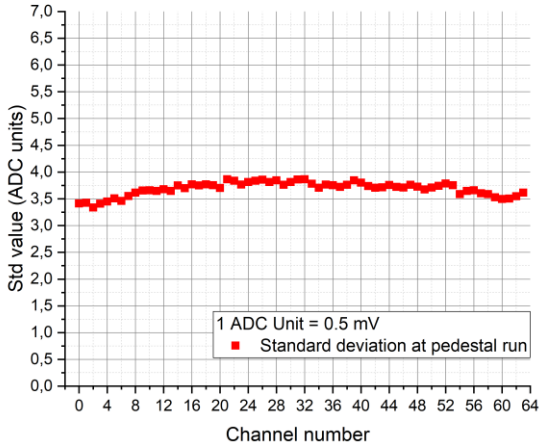
Beam tracker



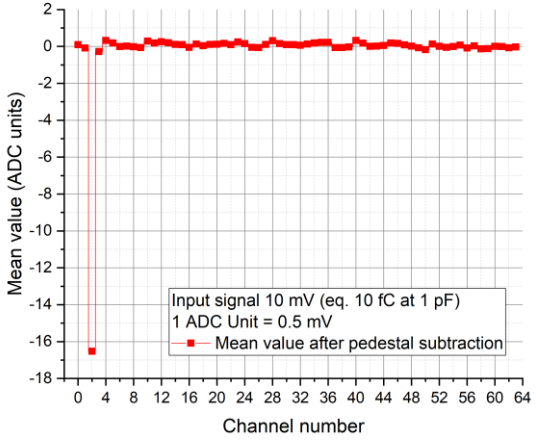
- **detector:** DSSD, 128×128 strips, pitch p+ / n+ strips 0.47 mm, thickness 175 μm, active area 61×61 mm^2;
- **FEE:** based on **VATA64HDR16.2 (64 ch, dynamic range: -20 pC ÷ +50 pC)**;
- **current status:** three vacuum stations with flanges and cable connectors are ready, Silicon Detectors assembled on PCBs and tested with alpha-source (5.5 MeV). Cross-board and FEE PCB are under test (left picture). Mechanical support and FEE cooling in progress within schedule.



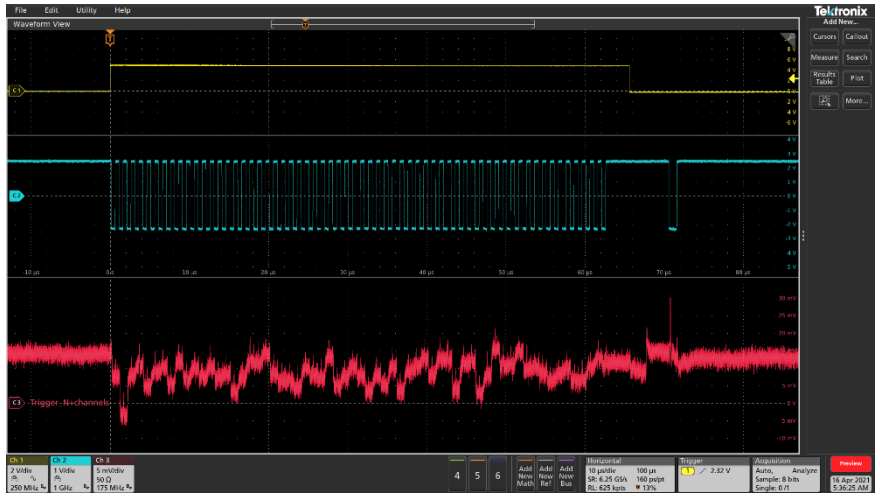
Beam tracker FEE first test result



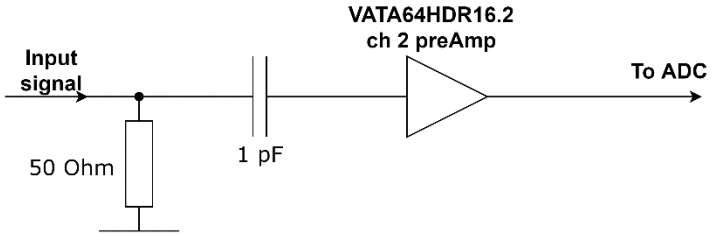
Standard deviation values per ASIC channel at pedestal run



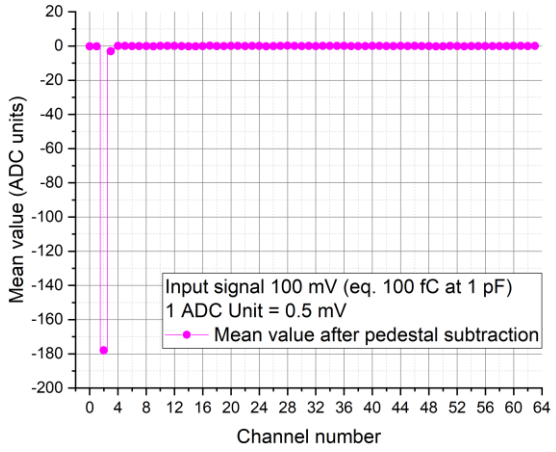
Mean values per ASIC channel
at test signal run 10 mV in ASIC ch #2 (after pedestal subtraction)



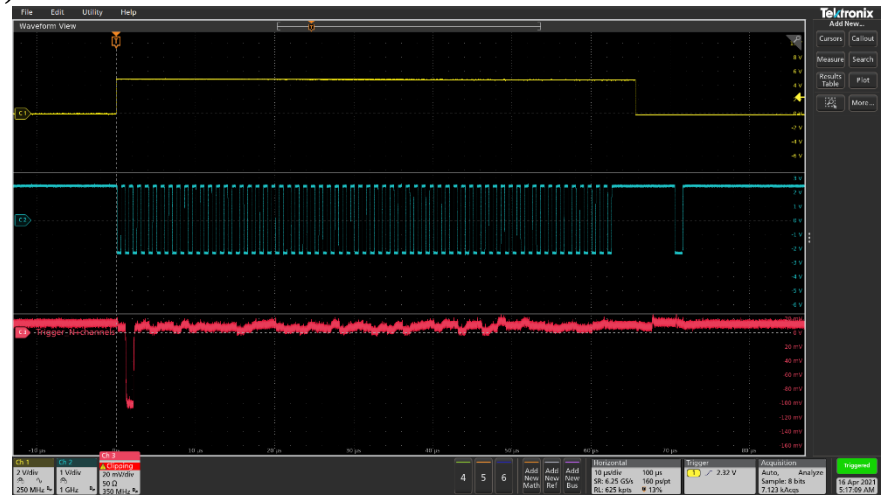
Oscilloscope screenshot at test signal run 10 mV



Simplified measurement circuit for ASIC ch #2

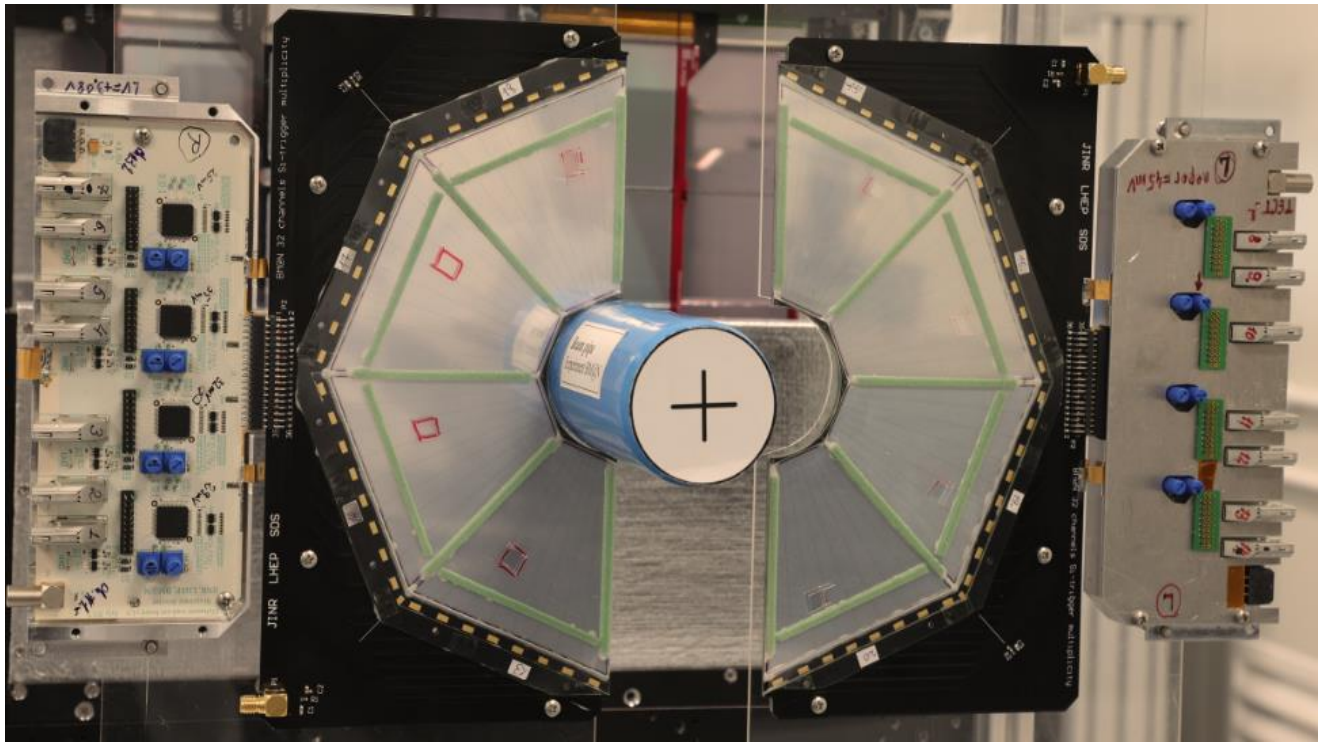


Mean values per ASIC channel
at test signal run 100 mV in ASIC ch #2 (after pedestal subtraction)



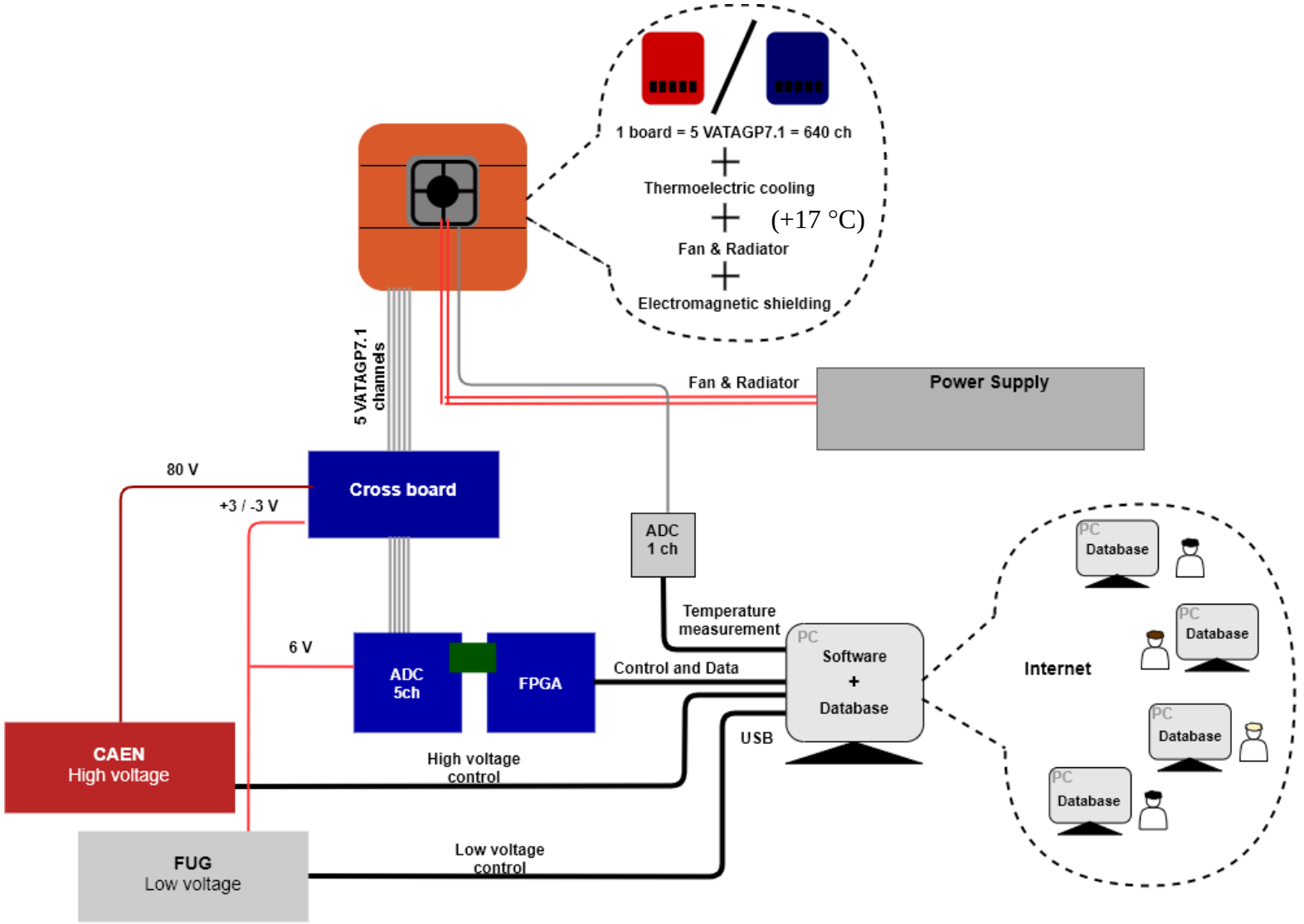
Oscilloscope screenshot at test signal run 100 mV

Multiplicity trigger



- **detector:** Silicon single-sided Detector, 525 μm thickness, 8 strips located at an angle with an interval of 5.63° and is an isosceles trapezoid in shape (45°) and active area 30.8 cm^2 (5 times bigger than previous Si-multiplicity trigger 2018).
- **mechanical design :** new design is based on 2 symmetric half-planes (inner diameter Ø52 mm), which simplify multiplicity trigger assembling process around installed beam pipe. Multiplicity trigger is located at 62 mm downstream the target.
- **FEE:** based on 32 channel IC-AST-1-1 (Minsk) with adjustable threshold.
- **current status:** two half-planes assembled and tested with previous FEE (2018). New FEE design with new gain parameters is under discussion (due to strip capacitance 5 times increase).

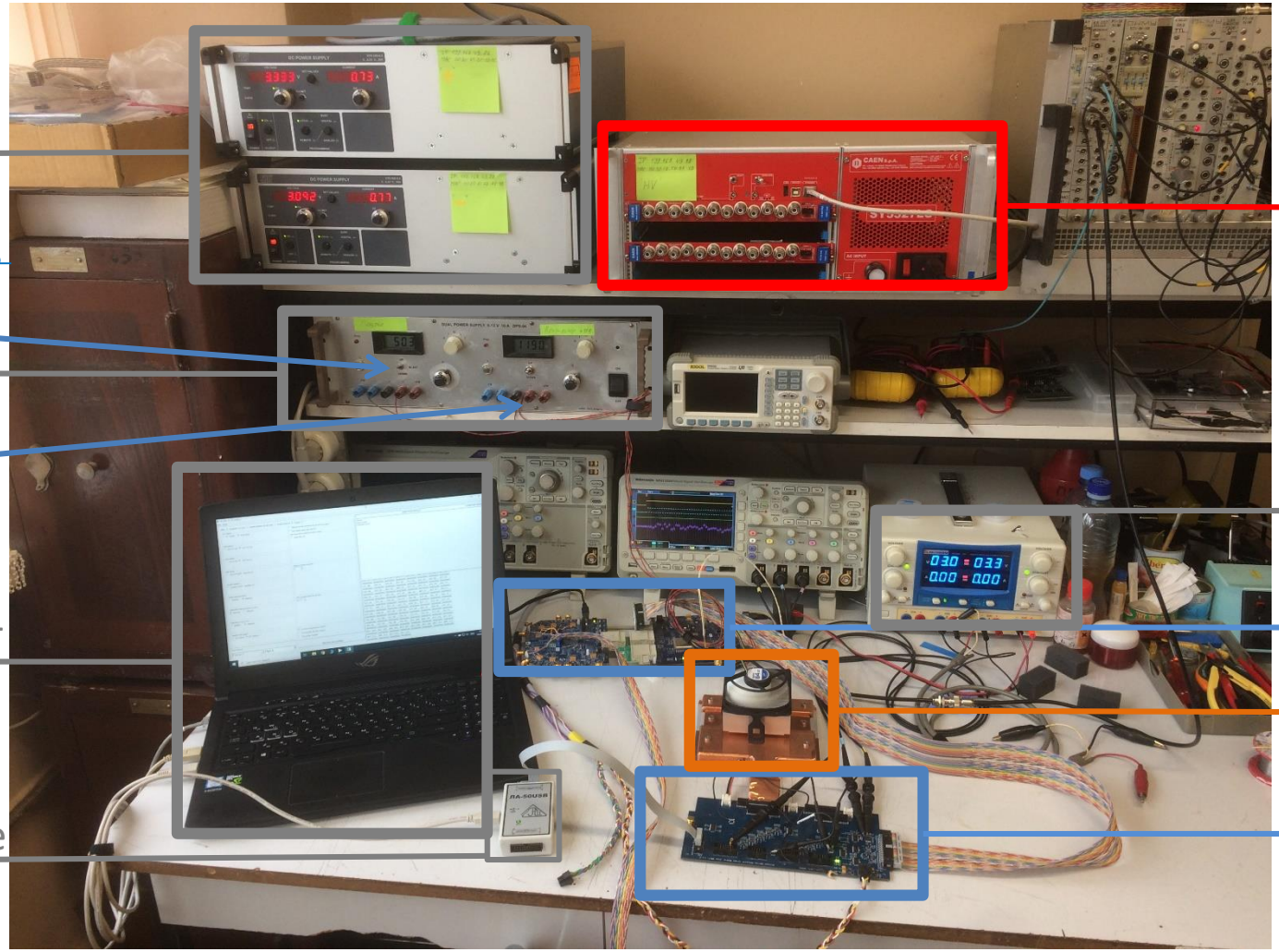
Front-end electronics test bench configuration



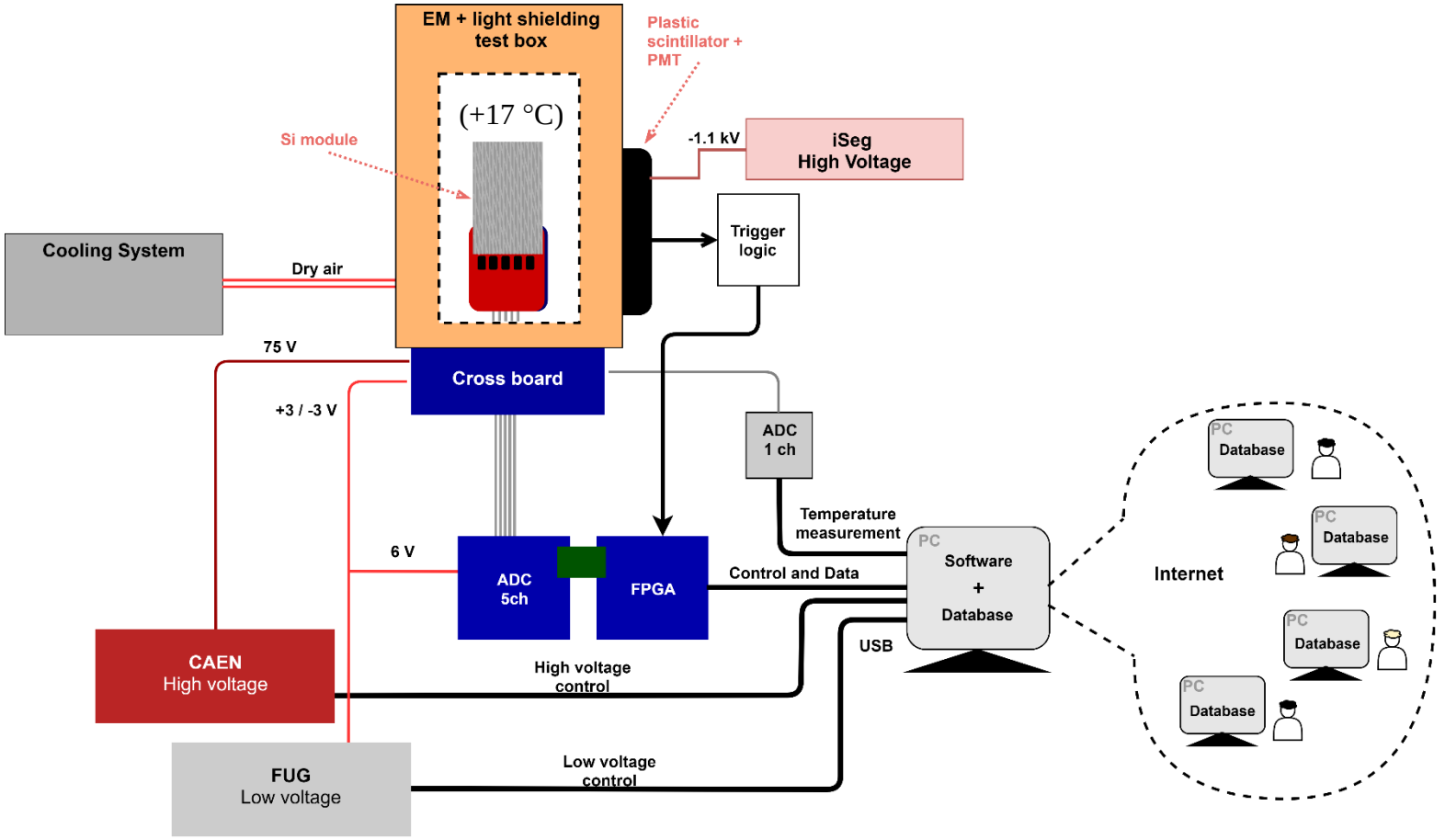
Testing scenario:

1. Connect PCB to stand (HV, LV and temperature will be measured whole time) in cooling and EM shielding box;
2. Make pedestal run for each chip without HV at pitch-adapter, save raw data;
3. Send configuration data to each chip;
4. Measure crosstalk between neighbor channels (external test signal);
5. Measure I(PA)= f(U_{HV}) leakage current of PA-640n+ (only for n+ PCB);
6. Measure ENC= f(U_{HV}) (only for n+ PCB);
7. Save data to the database.

Front-end electronics test bench configuration



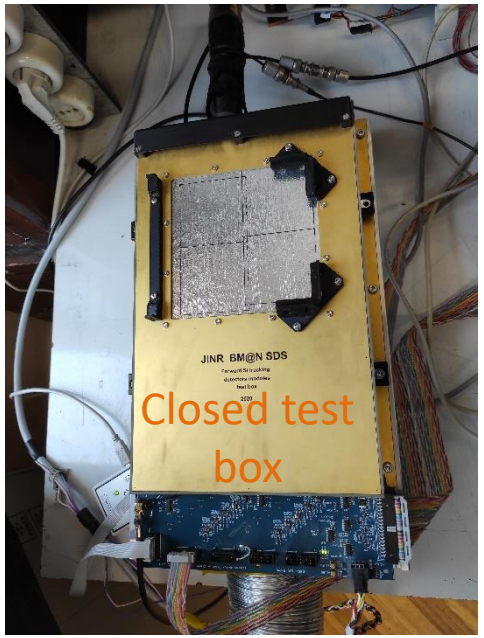
FST Si modules test bench configuration

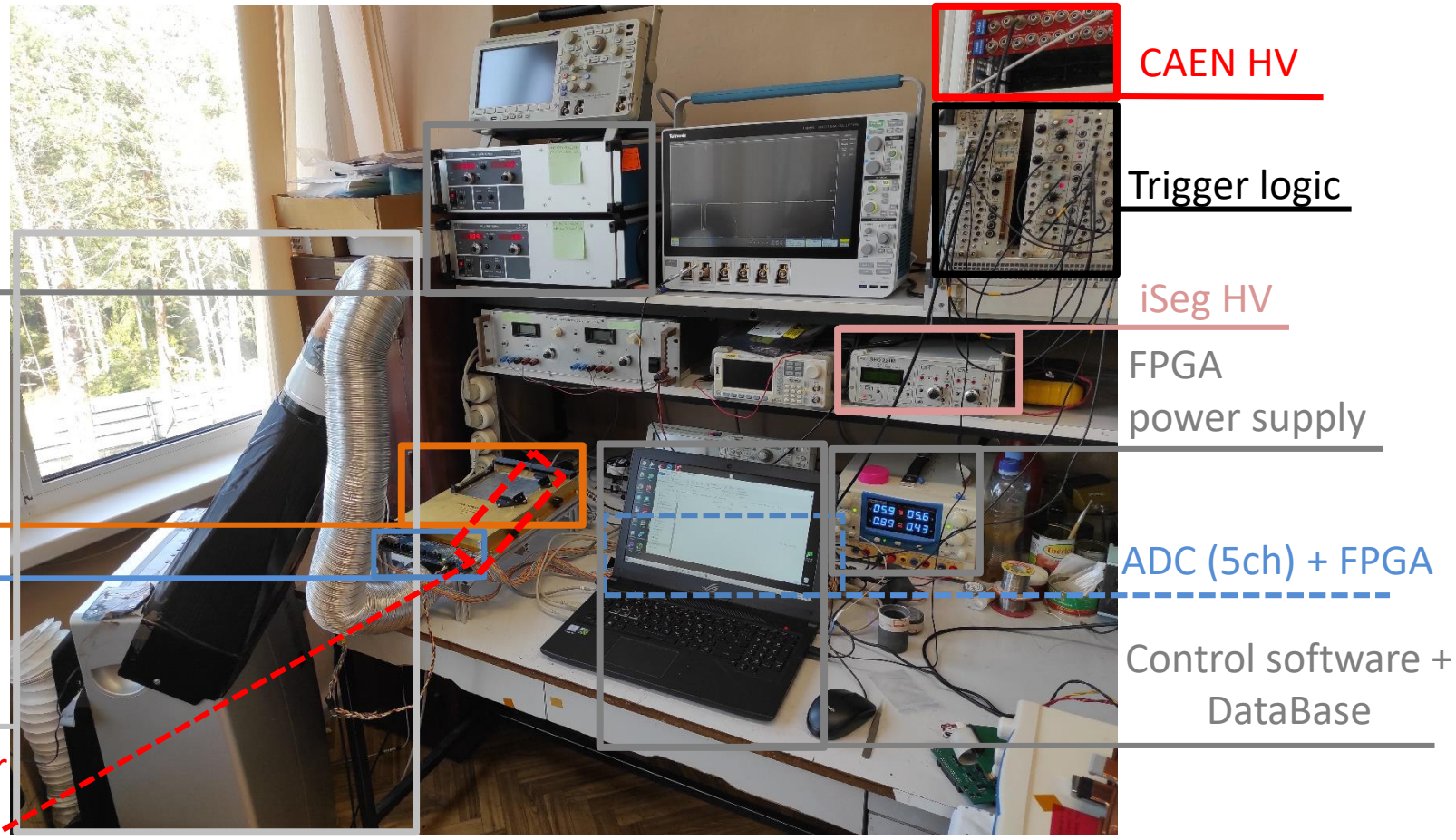


Testing scenario:

1. Connect FST Si module to stand (HV, LV and temperature will be measured whole time) inside EM + light shielding test box;
2. Send configuration data to all ASICs;
3. Make pedestal run for both module sides (ADC has 5 channels => only 1 side can be measured per run) with different HV values: 0, 25, 50 and 75 V.
4. Make run with radioactive source ^{226}Ra at different position and HV values.
5. Save measured data to the database.
6. Data analysis: a) Idark= f(U_{HV}); b) ENC = f(U_{HV}); c) amplitude of cluster distribution; d) cluster sizes distribution; e) occupancy distribution.

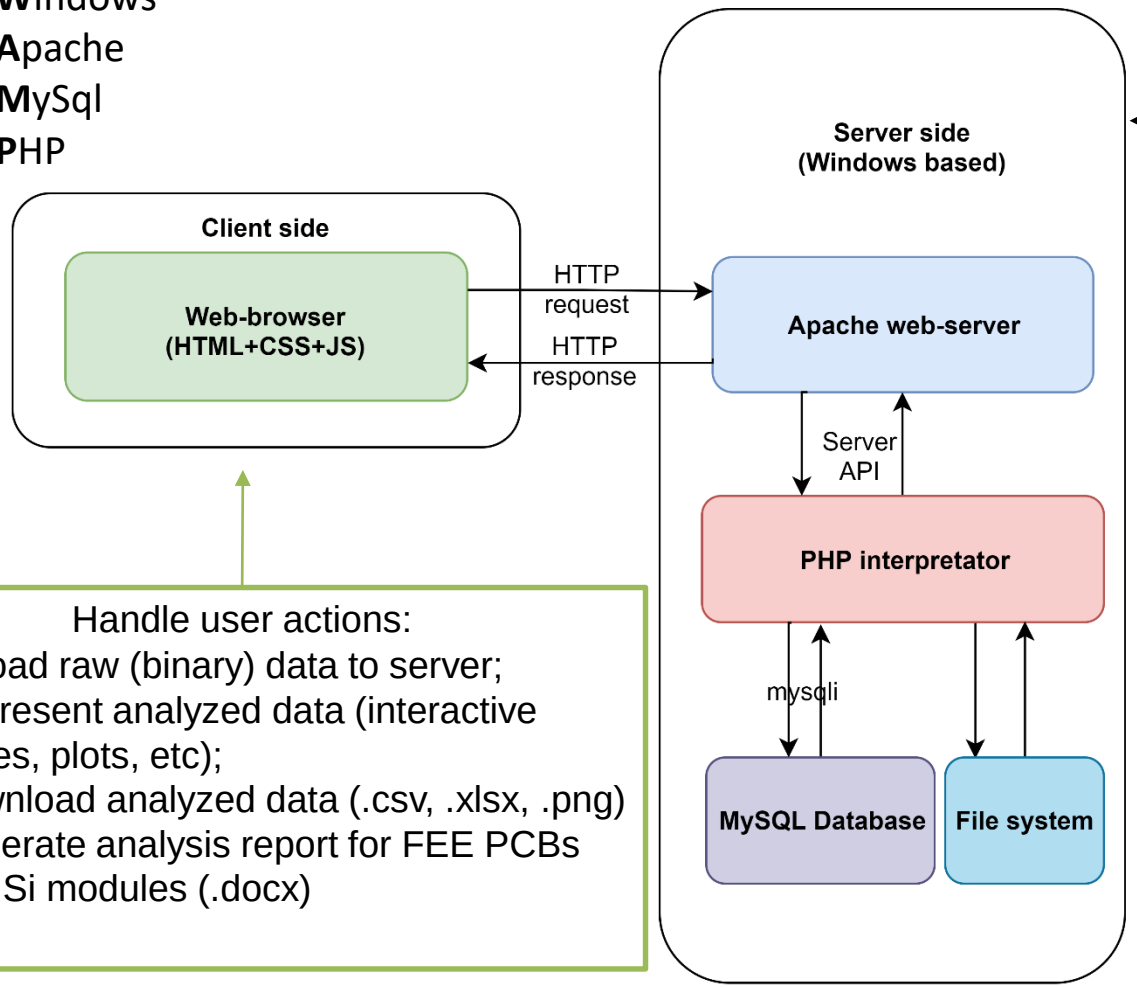
FST Si modules test bench configuration





Storing and analyzing measurement data solution

Used stack:
Windows
Apache
MySql
PHP



1. Download raw (binary) data from client side and store it in file system;
2. Preprocess data (decode and digitize raw data, parse measurement conditions);
3. Store preprocessed data in database;
4. Analyze preprocessed data;
5. Store analyzed data in database;
6. Send analyzed, preprocessed data and measurement conditions to client side

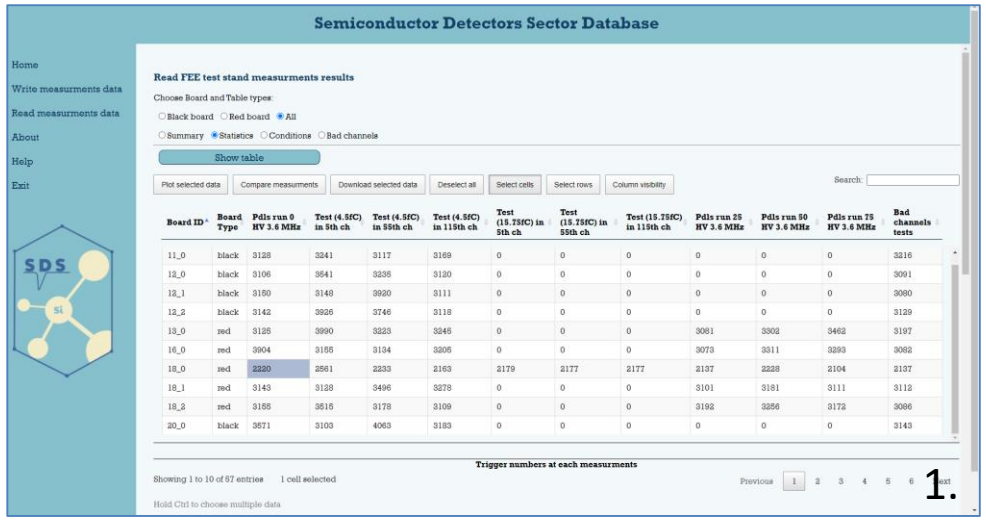
FEE:
1. Calculate mean and std for each ASIC channels;
2. Pedestal subtraction in measurement with internal ASIC test signals;
3. Calculate summary parameters (mean SNR, Xtalk coefficient, bad channels ratio).

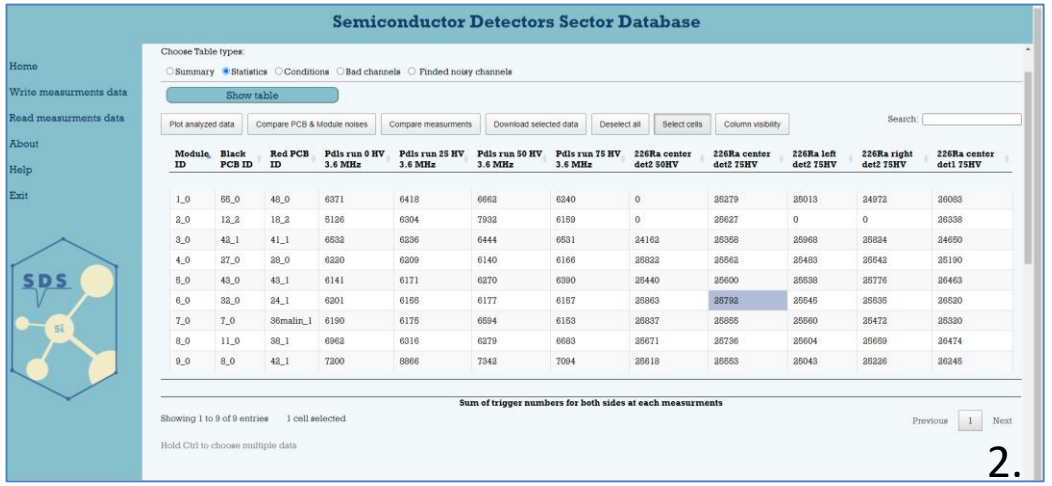
Si modules:
1. Calculate mean and std for each Si module channels;
2. Pedestal and CMS subtraction in measurement with radioactive (RA) source;
3. Cluster finding, calculate amplitude of cluster and cluster size (with RA source);
4. Occupancy distributions and landau fitting amplitude of cluster distributions (with RA source);
5. Calculate summary parameters (mean SNR for p+ & n+ sides, bad channels ratio).

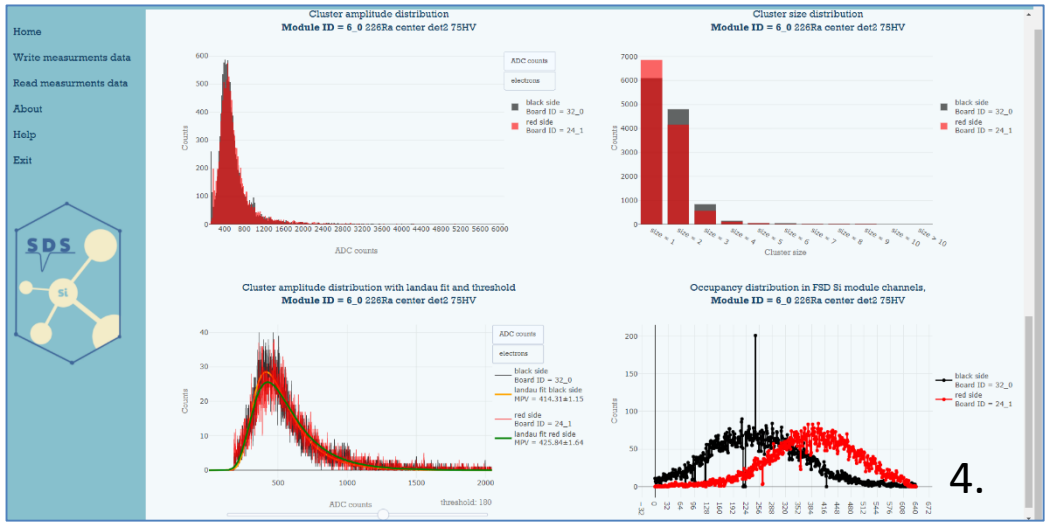
Handle user actions:
1. Upload raw (binary) data to server;
2. Represent analyzed data (interactive tables, plots, etc);
3. Download analyzed data (.csv, .xlsx, .png)
4. Generate analysis report for FEE PCBs and Si modules (.docx)

Storing and analyzing measurement data solution

Web interface





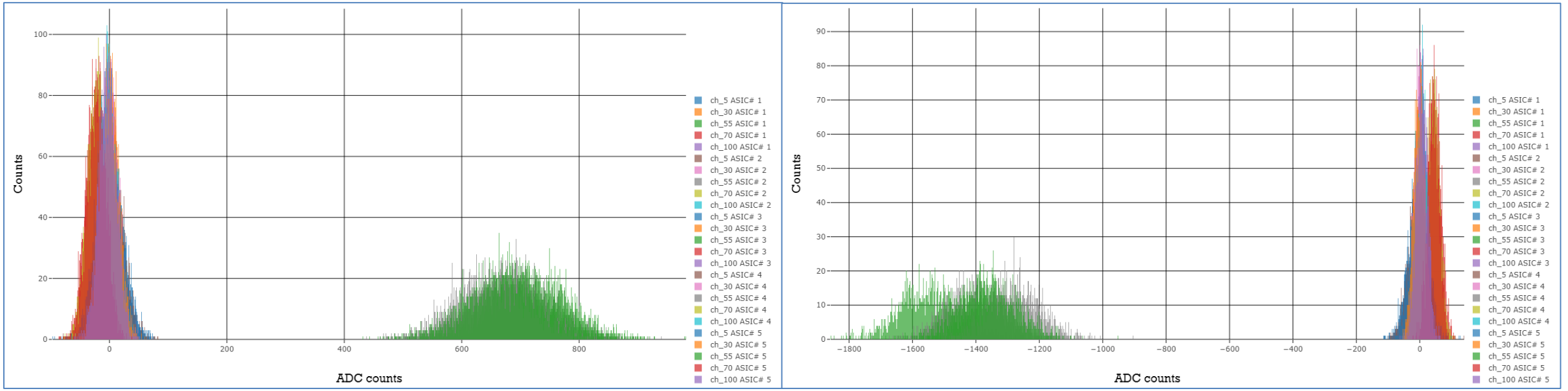


1. Interactive tables for FEE test measurements
2. Interactive tables for FST Si modules measurements
3. Interactive plots with FEE test results (chosen in table cell)
4. Interactive plots with FST Si modules test results (chosen in table cell)

JINR Grant for young scientists № 21-102-10

FEE test results

For example FEE PCB of Si module (ID 6_0)



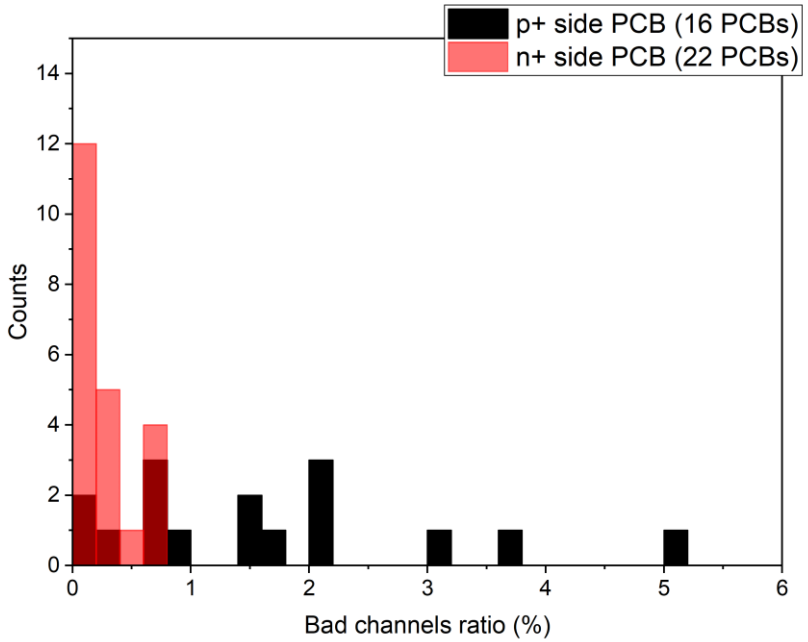
Signal distributions in ASIC channels for p+ side PCB (left) and n+ side PCB (right) after pedestal subtraction (wo CMS subtraction, Test signal 5 fC in 55th ch). Read-out frequency 3.6 MHz, T = 17 ºC.

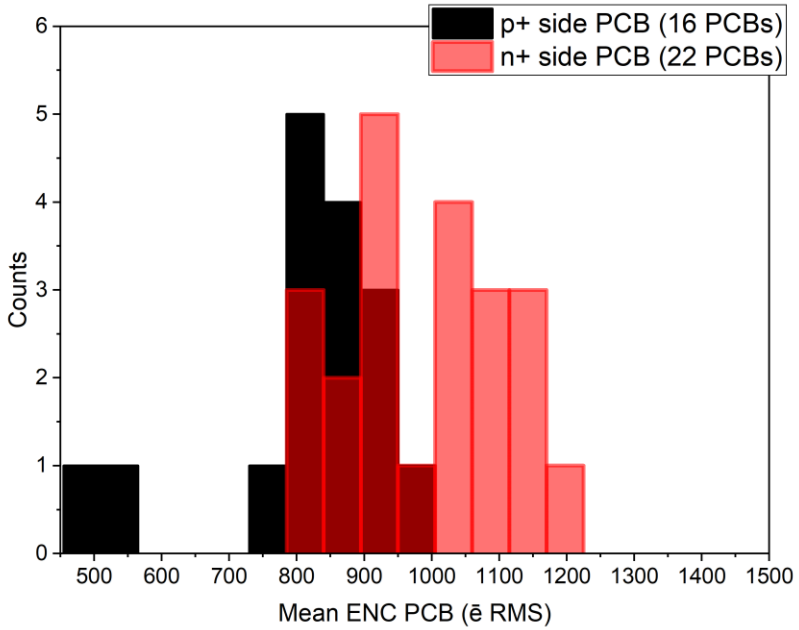
Board ID	Board type	<$ENC_{ASIC\#1}$> ē RMS	<$ENC_{ASIC\#2}$> ē RMS	<$ENC_{ASIC\#3}$> ē RMS	<$ENC_{ASIC\#4}$> ē RMS	<$ENC_{ASIC\#5}$> ē RMS	<ENC_{PCB}> ē RMS	<SNR> with internal signal	Bad channels ratio, %
32_0	**black**	**1023.40**	**945.45**	**955.44**	**926.33**	**942.46**	**958.62**	**30.8279**	**0.31**
24_1	**red**	**1125.96**	**1069.42**	**1105.30**	**1042.33**	**1190.33**	**1106.67**	**65.3742**	**0.31**

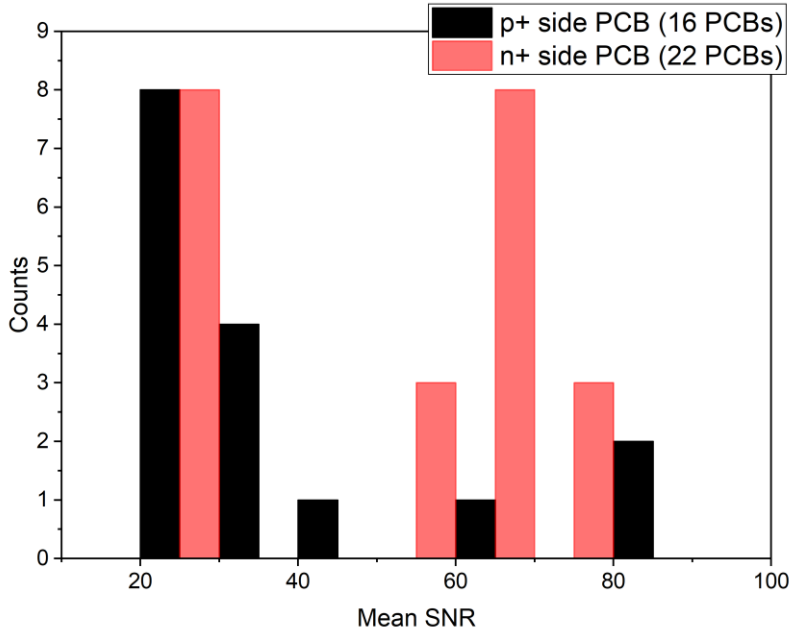
FEE test results current status

38 from 84 PCBs were tested (13.04.2021)

Note: channel marked as bad if it has
$ENC_{Ch} > (3*<ENC_{PCB}>)$ OR $ENC_{Ch} < (<ENC_{PCB}>/3)$
(i.e. it does NOT dead channel!)

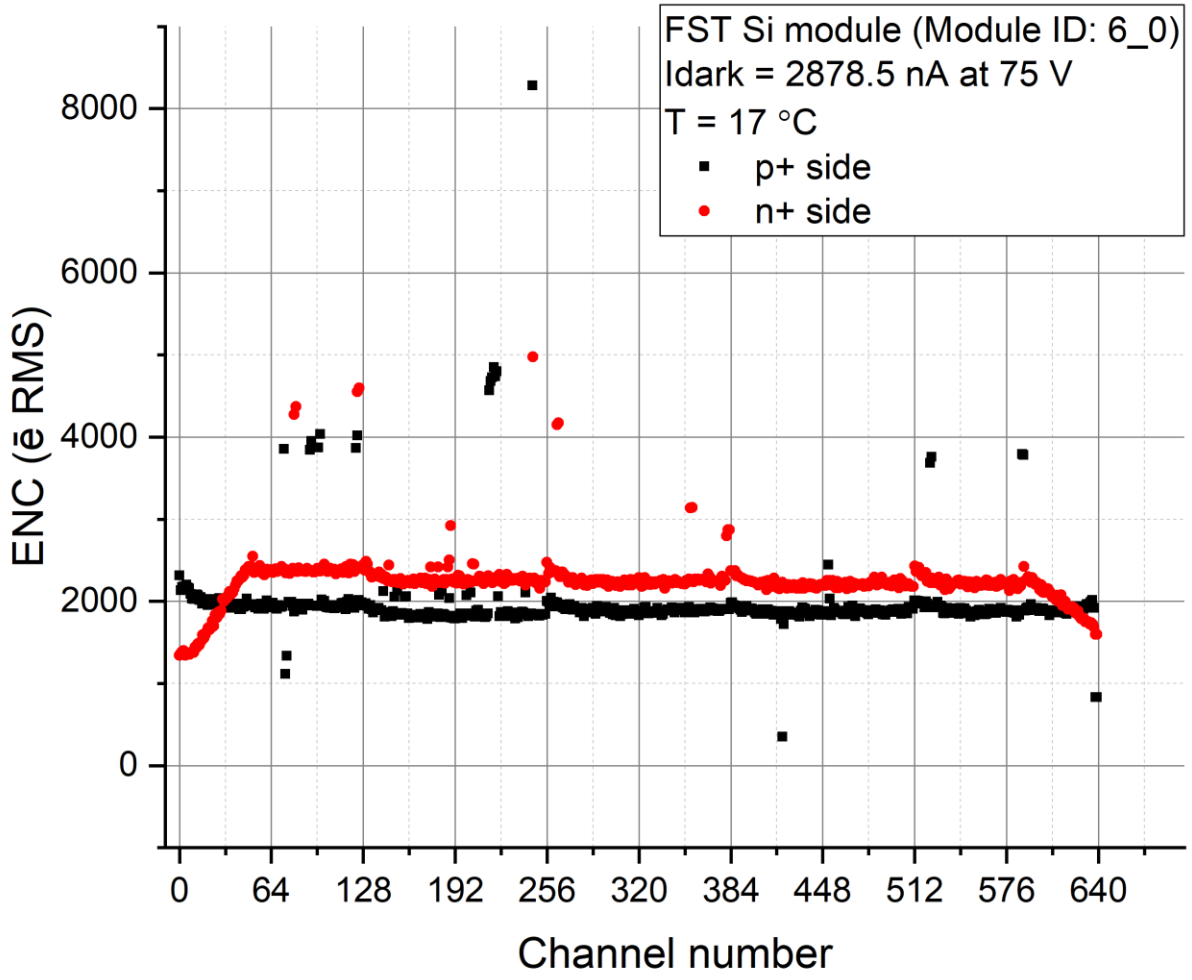






Summary parameters of tested PCBs bad channels ratio (left), $<ENC_{PCB}>$ (center) and $<SNR_{PCB}>$ (right)

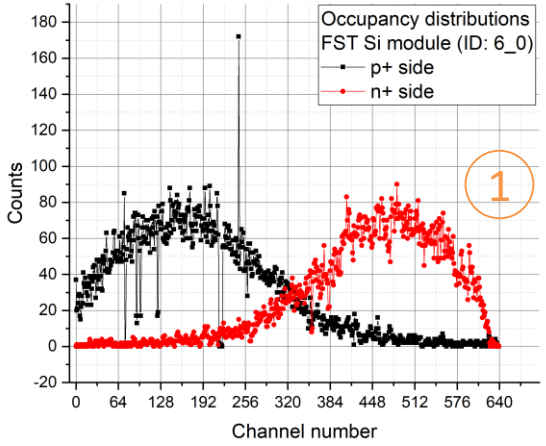
FST Si module test results

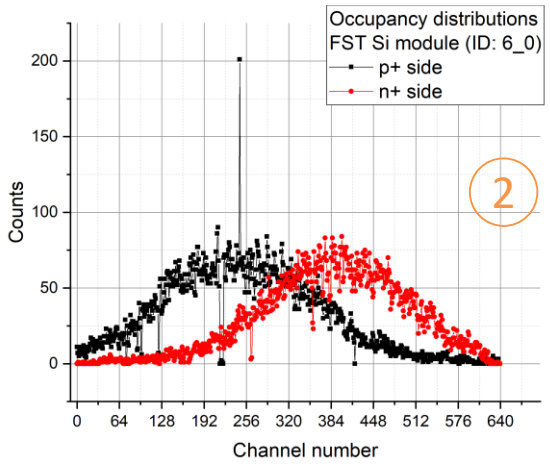


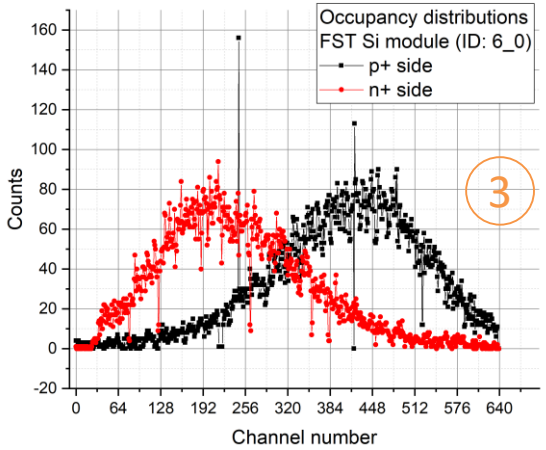
For example FEE PCB for Si module (ID 6_0):
p+ side PCB (Board ID: 32_0);
n+ side PCB (Board ID 24_1)
Pedestal run at 75 V HV and read-out frequency 3.6 MHz (numeration starts from 0th channel)

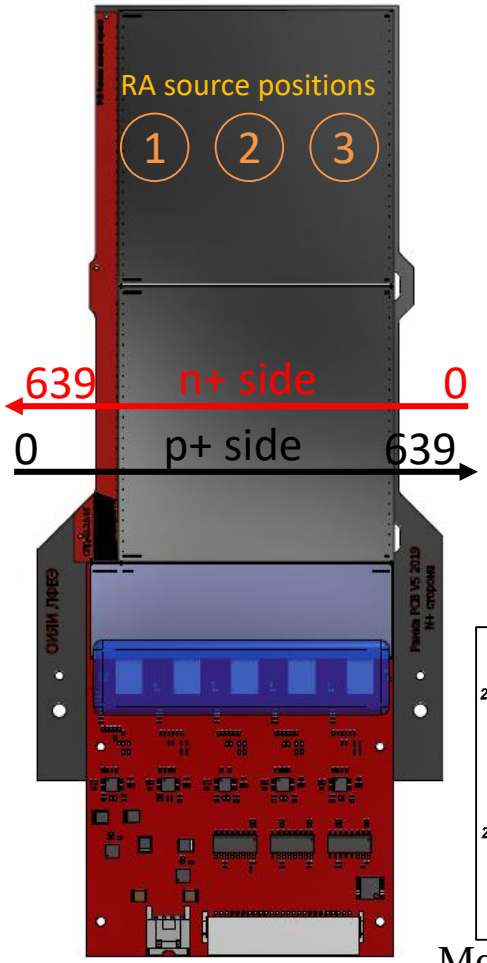
ENC per Si module channels
<ENCp+> = 1964 ē RMS
<ENCn+> = 2238 ē RMS

FST Si module test results

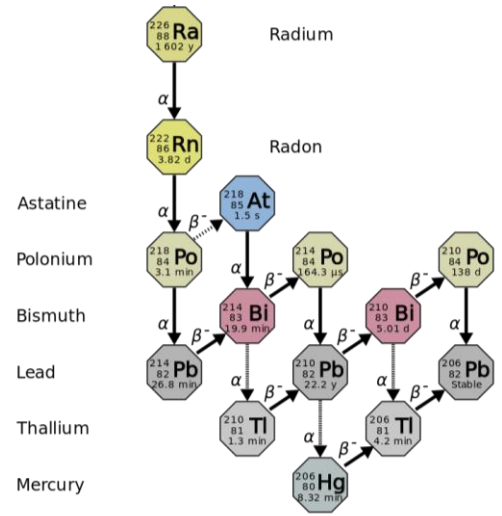




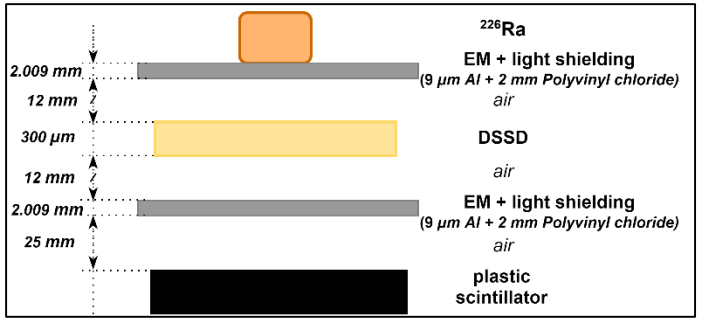




Ufd = 30 V

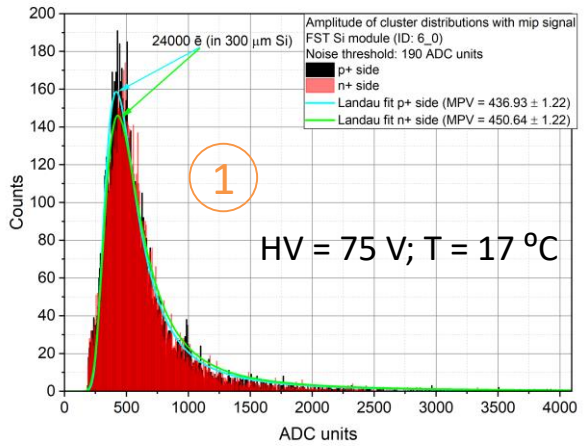


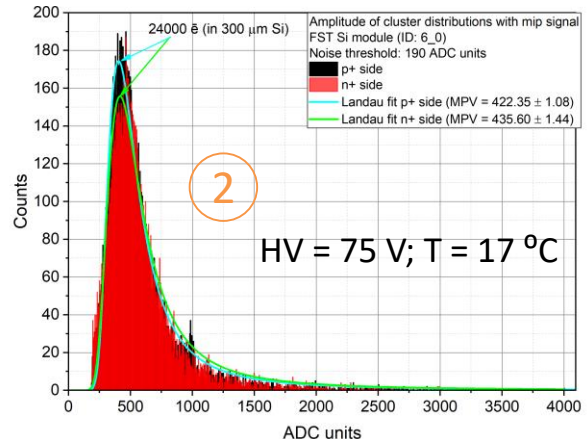
Electron end-point energy up to 3.27 MeV ($^{214}_{83}Bi$)

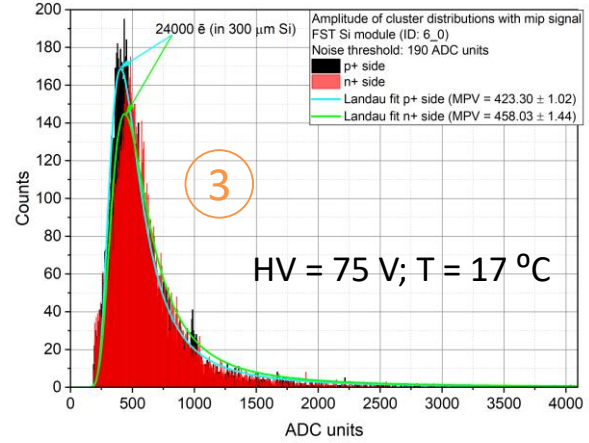


Measurement with RA source cross-section
(trigger rate: 150 Hz)

Module ID	<ENCp+> ē RMS	<ENCn+> ē RMS	SNR p+ side	SNR n+ side	Bad channels ratio, %
6_0	1963.60	2 237.88	12.22	10.72	1.25



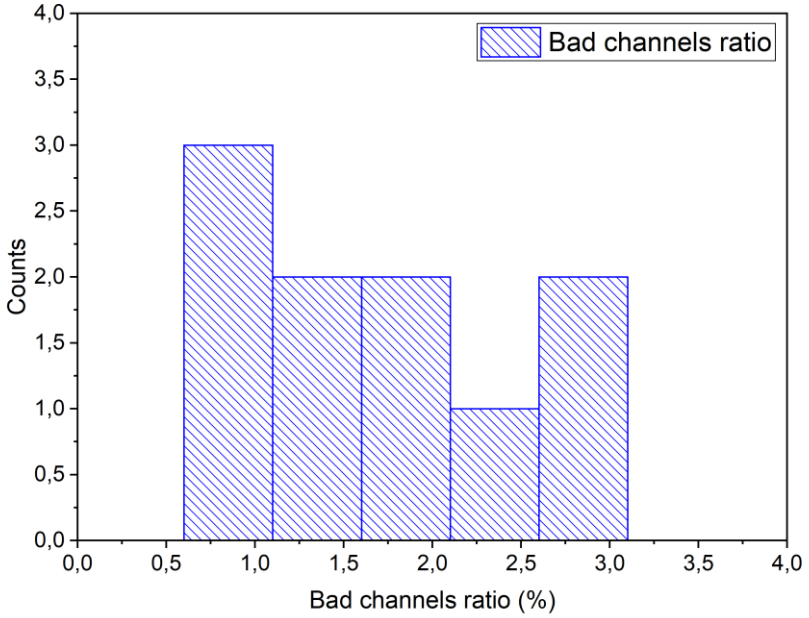


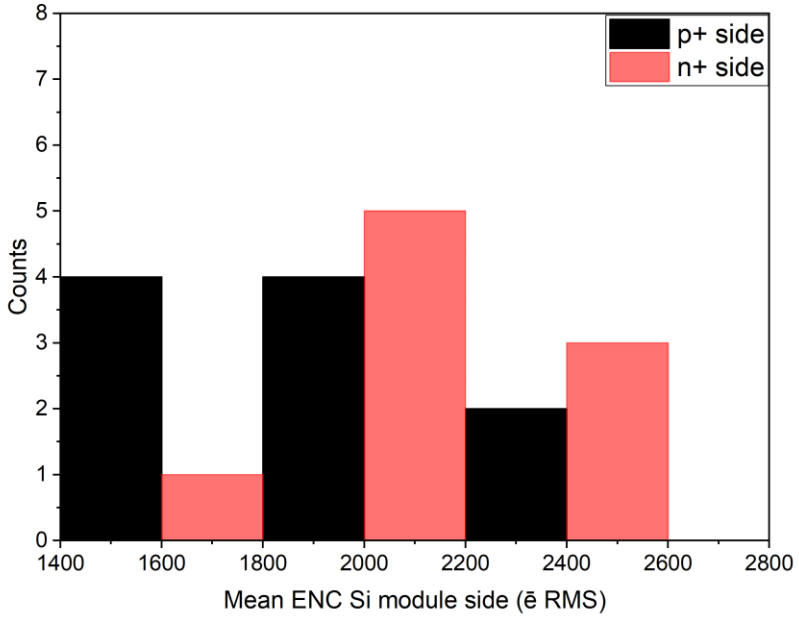


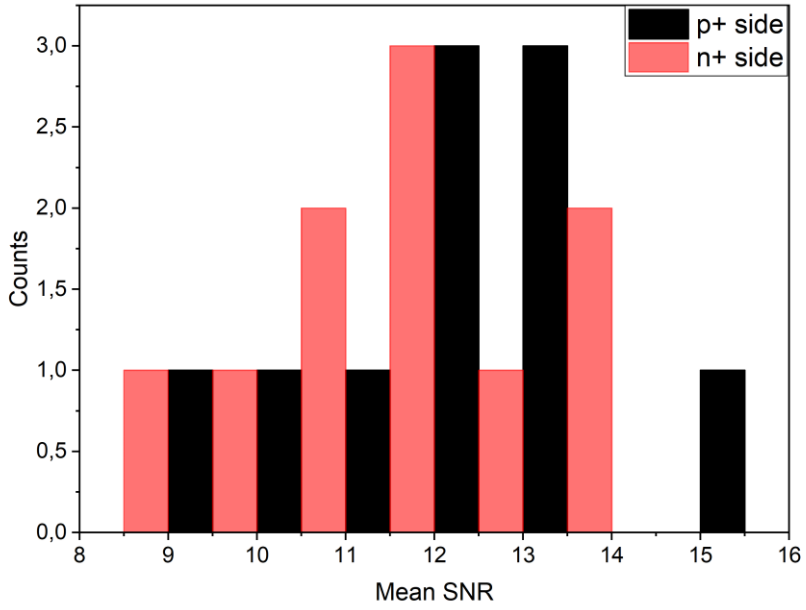
FST Si module test results current status

10 from 42 Si modules were tested (13.04.2021)

Note: channel marked as bad if it has
$ENC_{Ch} > (2*<ENC_{side}>)$ OR $ENC_{Ch} < (<ENC_{side}>/2)$
(i.e. it does NOT dead channel!)

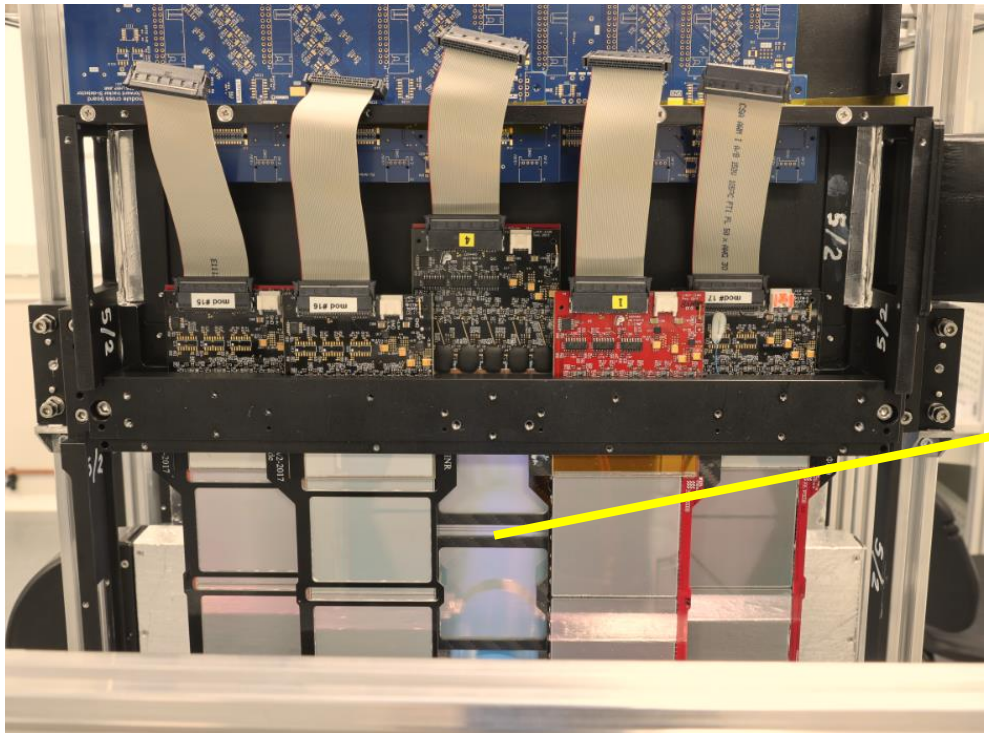




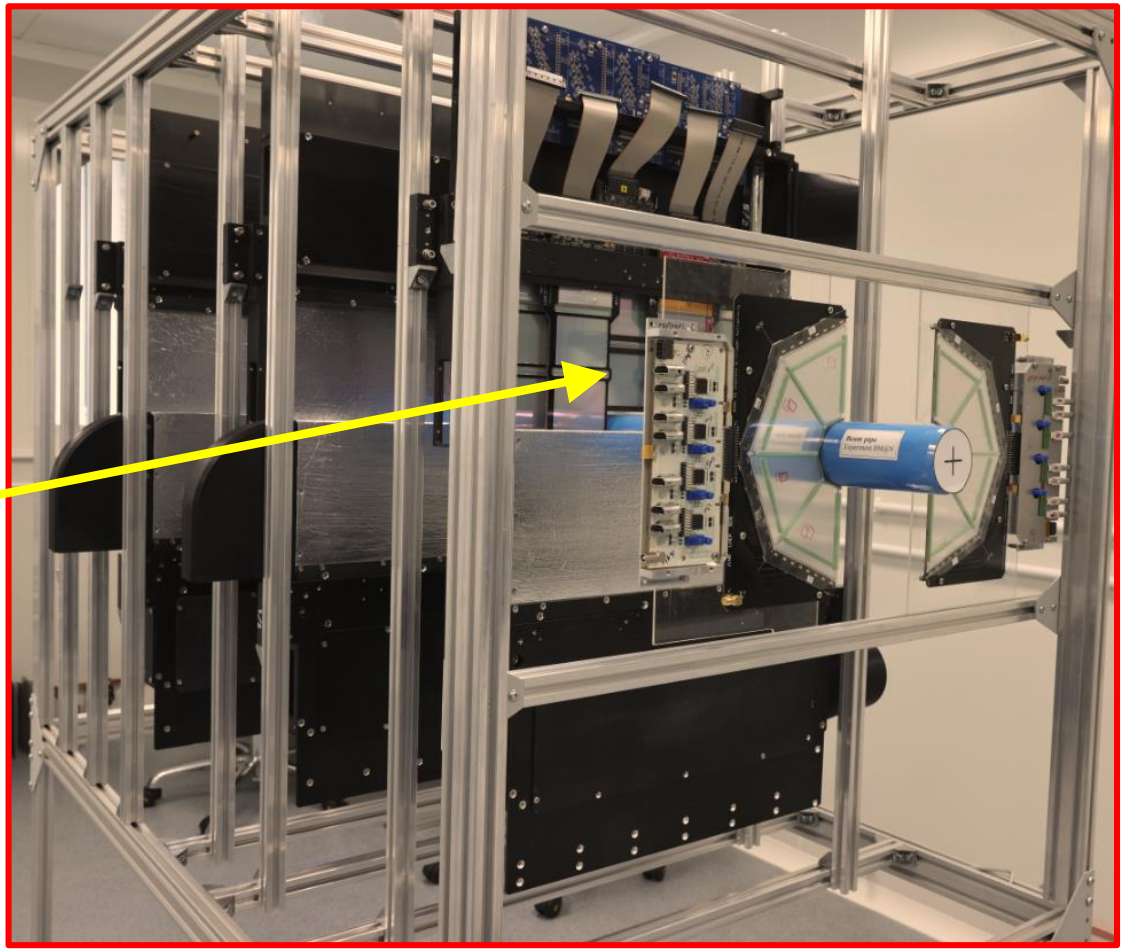


Summary parameters of tested Si module bad channels ratio (left), $<ENC_{side}>$ (center) and <SNR> (right)

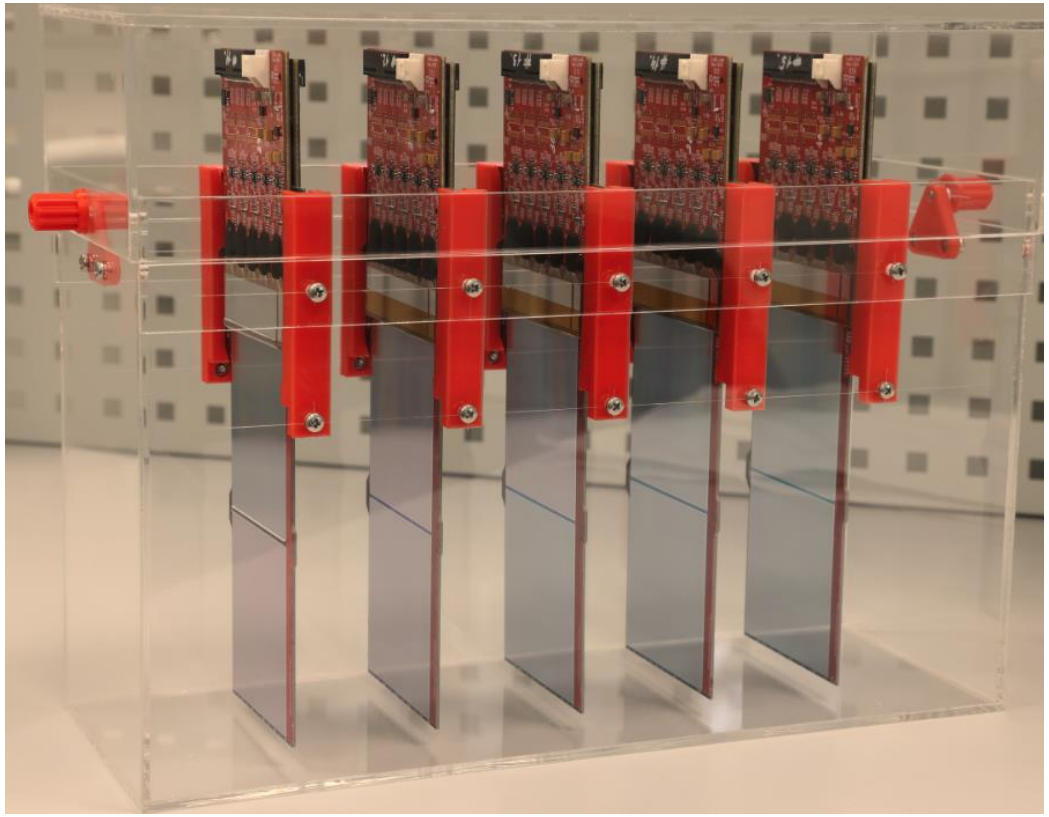
Forward Silicon Tracker



Upper half-plane without EM + light shielding (5 modules)



Forward Silicon Tracker status summary



- Forward Silicon Tracker FEE and Si modules test bench is designed and assembled;
- All 84 FEE PCB fully assembled (100%);
- 38 from 84 FEE PCB are tested (45 %);
- All tested PCB have $<ENC_{PCB}>$ less than 1500 ē RMS;
- 36 from 38 tested PCB have bad channels ratio ≤ 3%;
- 12 from 42 FST Si modules fully assembled (29%);
- 10 from 42 FST Si modules are tested (24%);
- All tested modules have $<ENC_{side}>$ less than 2500 ē RMS;
- Most Si modules have mean SNR_{side} > 10 (mip signal amplitude distribution is separated from noise);
- All Si modules have bad channels ratio ≤ 3%;
- FST half-planes assembling are started.

Forward Silicon Tracker and beam detectors team

In the photo (from left to right):

Zubarev Evgeny
Streletskaya Ekaterina
Topko Bogdan
Topko Yulia
Tarasov Oleg
Kopylov Yury

Beyond the camera:

Khabarov Sergey
Smirnov Alexander
Sheremeteva Anastasiia
Zamyatin Nikolay