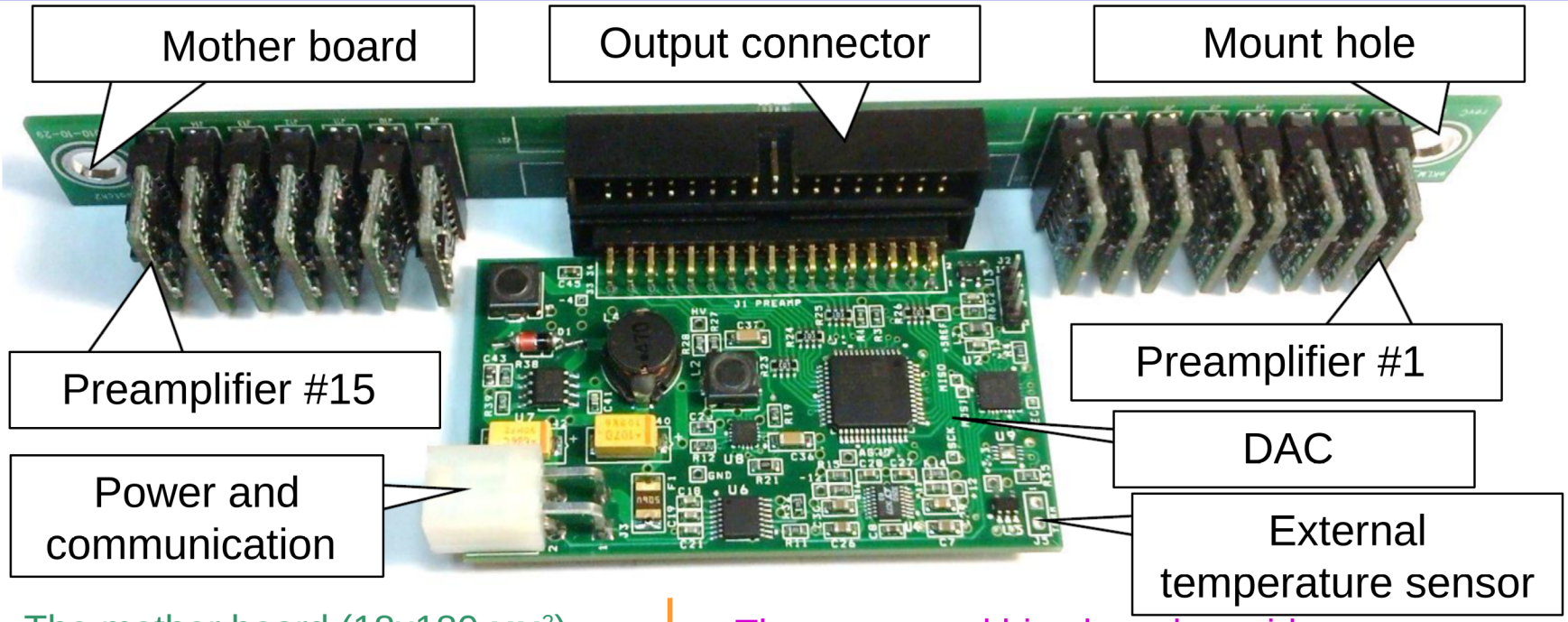
ZDC FE and DAQ (year 1)

SiPM bias and preamplifiers



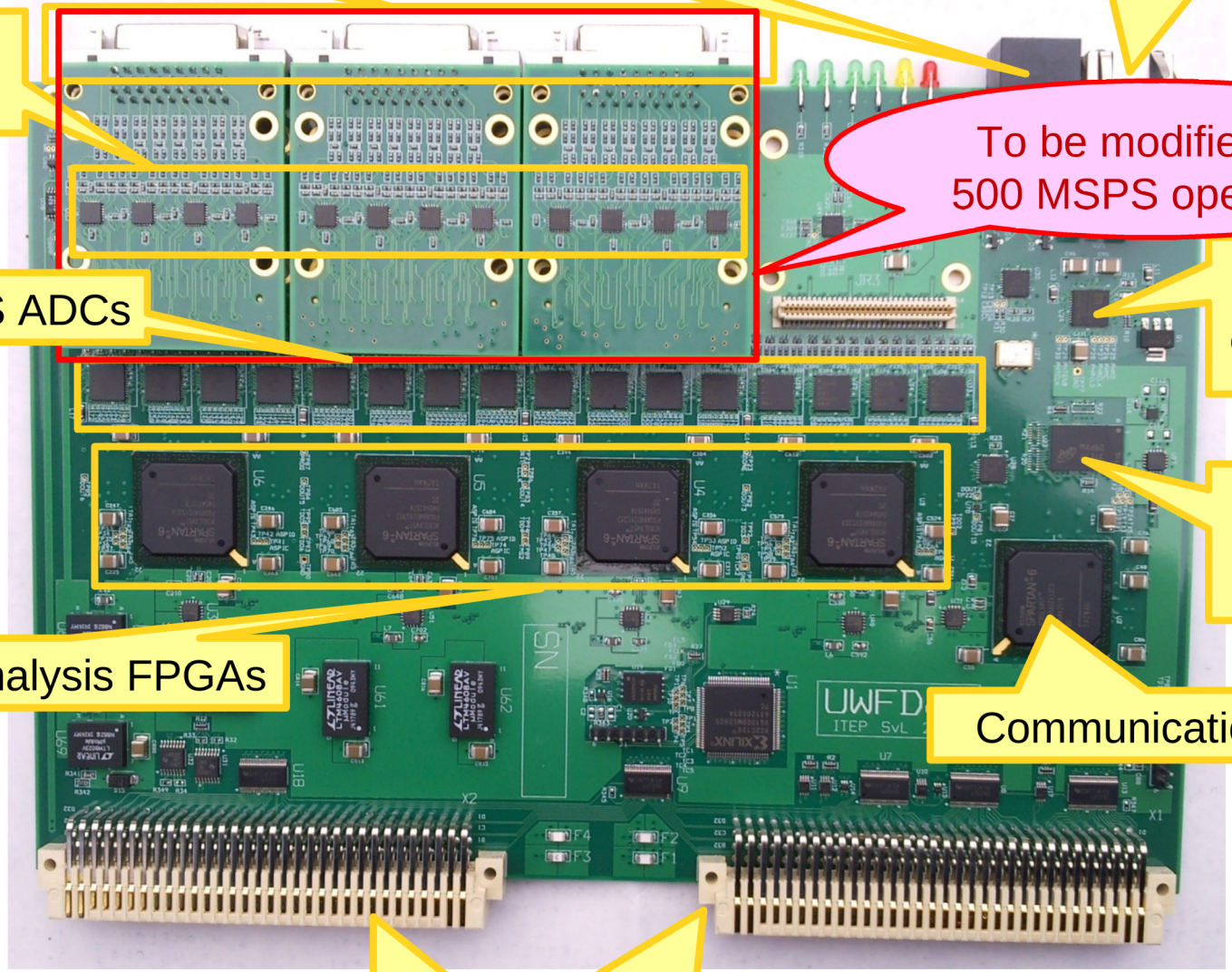
The mother board (18x180 мм^2) hosts:

- 15 preamplifiers with twisted pair differential current input
- Diffirential output
- Power and bias board
- Output connector

The power and bias board provides:

- Power for preamplifiers and its control
- Common cathode voltage for SiPMs, its precise setting and measurement in the range 10-65 V
- Setting and monitoring of the individual anode voltages in the range ±10V
- Readout of common bias current
- Readout of the external temperature sensor as well as onboard CPU and DAC temperatures

64-channel WFD



Igor Alekseev (ITEP)

64-channel WFD

- 64 channels of 125 MSPS 12 bit flash ADCs
  - 16 channels of 500 MSPS
- VME 64x standard 6U single slot width board
- 64-bit block transfer support
- Xilinx Spartan-6 FPGAs for digital signal processing and communication
- 4 Gbit of SDRAM for data storage
- 1 Gbit Ethernet connection for faster readout
- Multitrigger and triggerless operation
- Base line subtraction and zero suppression for wave form storage
- Selftrigger with prescale for SiPM noise measurements
- Internal or external clock operation
- Deadtimeless operation

Instruments and Experimental Techniques, 2018, Vol. 61, No. 3, pp. 349–354.

Performance at DANSS