Electronics FE/DAQ/DCS

Leonid Afanasyev

Compilation of presentations at SPD Hardware meetings on 25 March and 29 April 2021

Estimation of raw data flow

Bunch crossing each 80 ns; crossing rate 12.5 MHz,
Collision rate ~3–4 MHz →
Triggerless DAQ to avoid any hardware biases

Data flux was estimated for the maximum luminosity $L = 10^{32}$ $cm^{-2}c^{-1}$ and maximum energy $\sqrt{s} = 27$ GeV.

Within simplified simulation and some safety margin the data flux is estimated as 20 GBytes/s.

Front-end electronics for the free-running DAQ-SPD

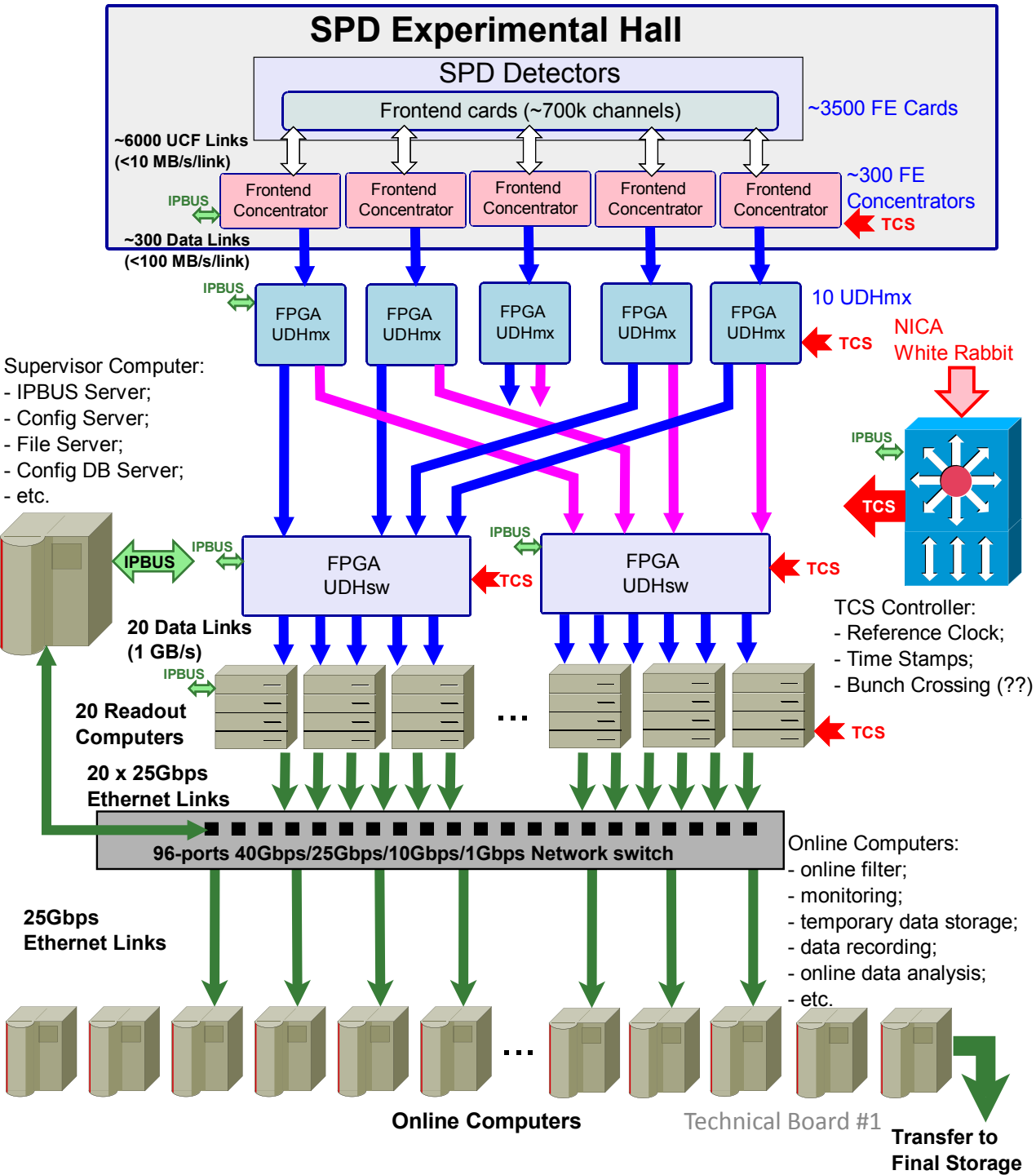
Front-end electronics of the detectors has to meet the requirements of a free-running DAQ

General FEE requirements from the DAQ system:

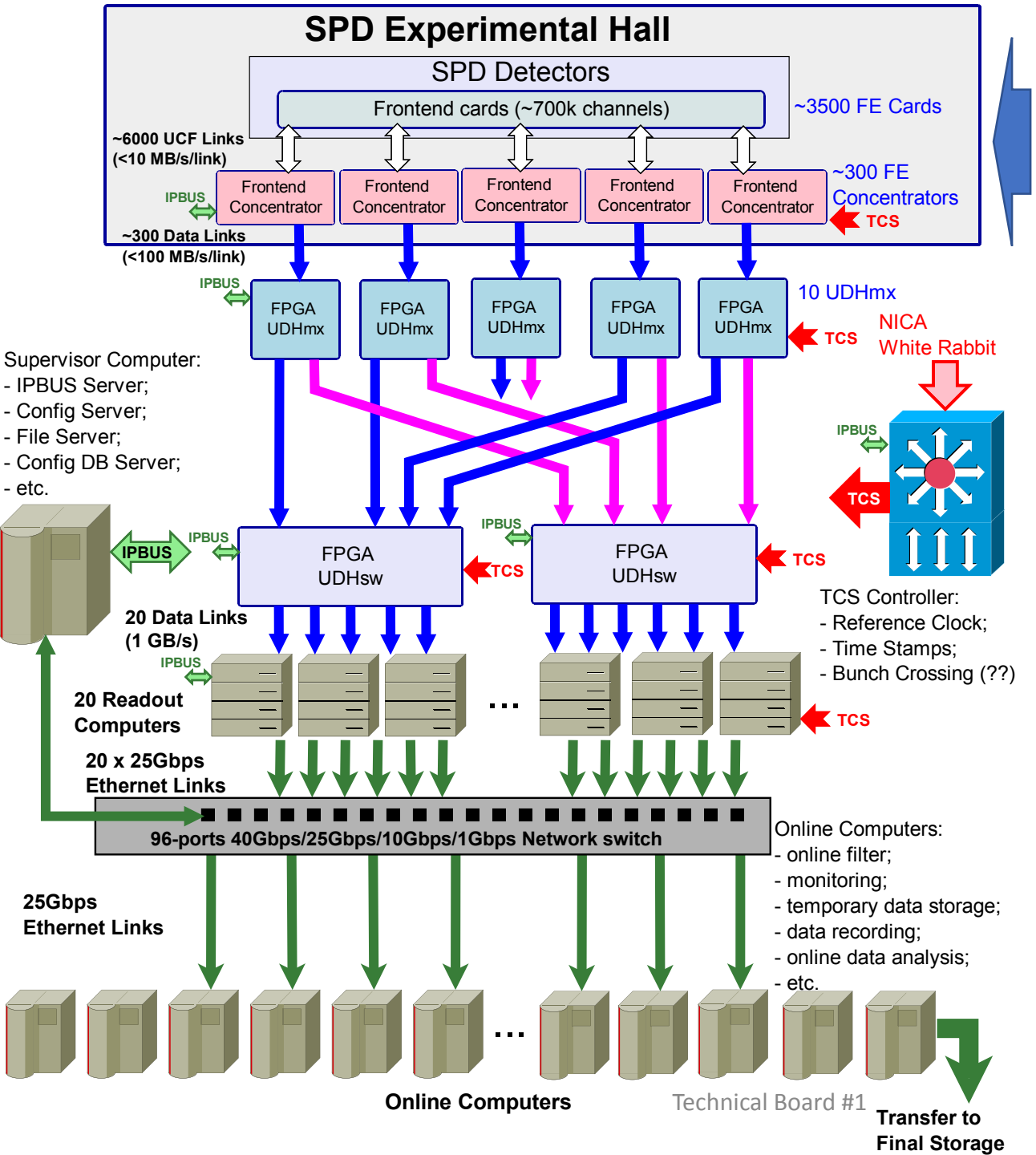
- Self-triggered (*trigger-less*) FEE operation
- Digitizing on-board
- Zero suppression
- Large memory to store the data accumulated in a time slice
- Timestamp included in the output format

Compatibility with DAQ (AMBER/NA64)

- Optic output
- Protocols: S-link, Aurora, UCF
- White Rabbit input (option)

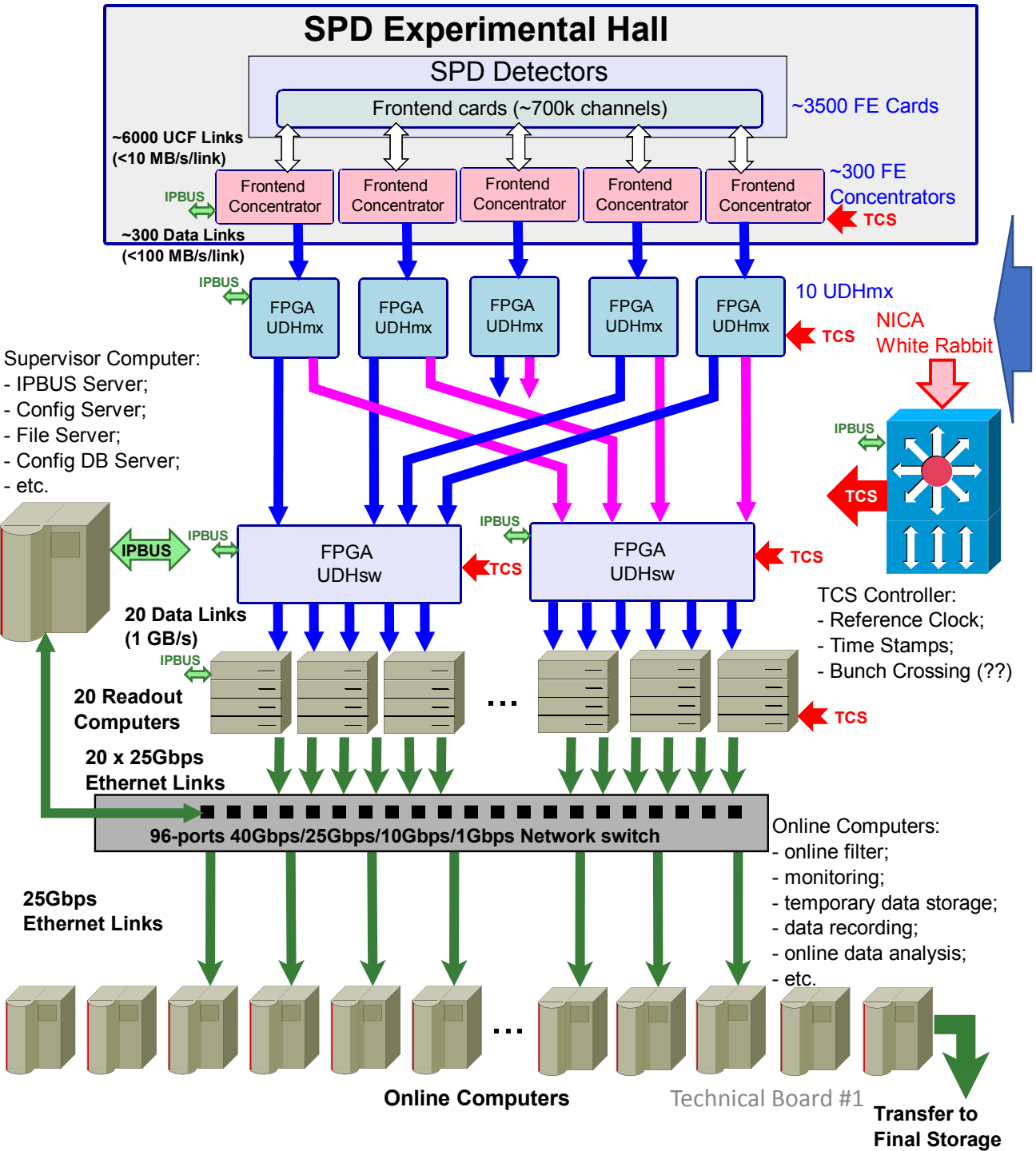


In DAQ of SPD we are planning to employ the ideas developed for the modernized DAQ of COMPASS/AMBER/NA64 by Igor Konorov group from the Technische Universität of München (TUM). His conception of SPD DAQ is accepted with minor modifications.



Slow control accesses FE cards via the FE Conccentrators using UDP-based IPBus protocol.

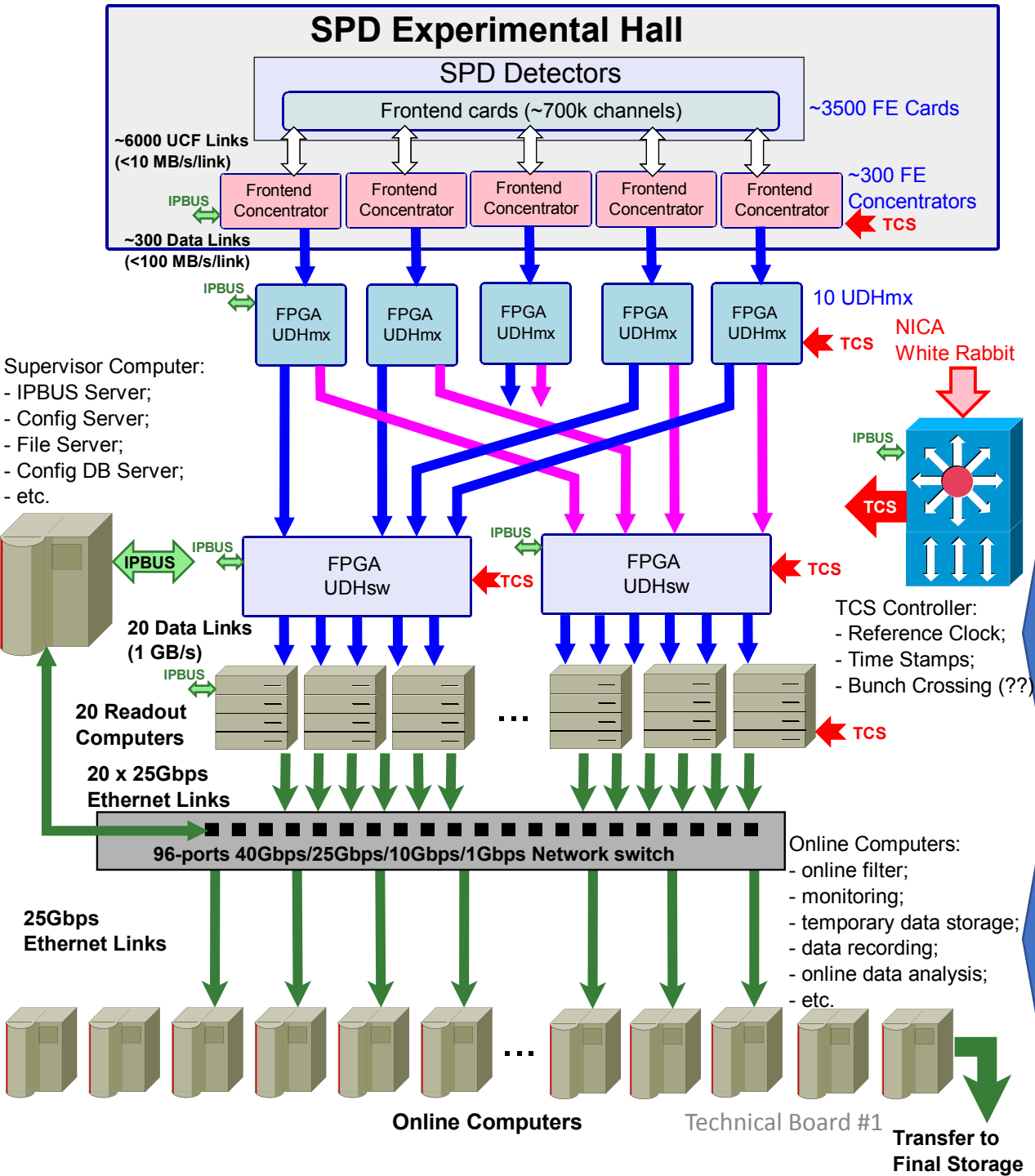
FE Conccentrators retransmit clock signals to FEE and convert detector information to a high speed serial interface running over an optical link.
UCF (*Unified Communication Framework*) protocol will be a standard high speed link protocol within the DAQ.



The multiplexer (UDHmx) modules receive detector information via serial links, verify consistency of data, and store them in DDR memories.

The multiplexer is equipped with 32 GBytes of memory.

All accepted data are assembled in sub-slice and distributed to two switches. Each multiplexer has a bandwidth of 2 GBytes/s.



The switches (UDHsw) perform the final level of slice building and distribute the assembled slices to 20 (?) on-line computers.

Finally, the continuous sequence of slices is built with Network Switch in each PCs

DAQ hardware

Near detector

Mechanics:

- 374 Front End Concentrators - VME 6U double width 12(15) inputs, 1 outputs
- 43 VME crates, 0.5kW ⟶ 9-10 racks
- Option with ATCA crates < 20

Cables:

- From detectors to DAQ: 4436 optic links
- From DAQ to the control room: 374 optic links (double), max 480 links

In barrack

3 VME crates (1kW)
20 DAQ computers (1kW) ⟶ 3-4 racks

Migration to ATCA (Igor Konorov 08-02-2021)

ATCA Carrier Card :

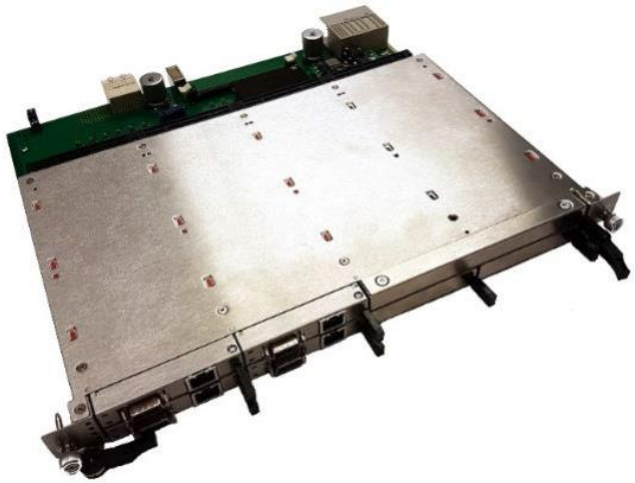
- 4 DHmx/DHsw modules
- 4 Optical interface AMC cards
- 16 links between A & B connectors

Rear interfaces

- 8 x Ethernet for IPBus
- USB for JTAG
- SFP+ for TCS interface + 1:8 fanout

Optical Interface AMC card

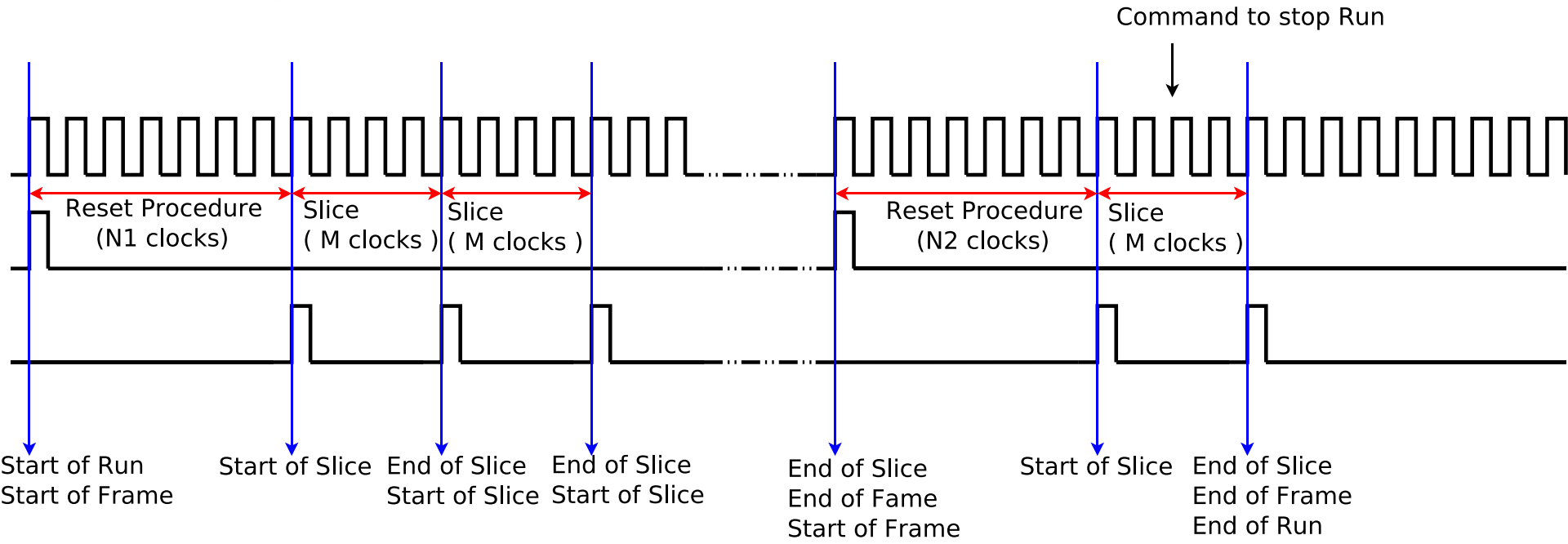
- 8 + 4 FireFly Transceivers



Computer input / PCI Express buffer

- Based on commercial hardware
  – Nereid Kintex 7 PCI Express
  – Trenz FMC – SFP adapter
  Kintex 7 XC7K160T FBG676
- 4x PCIe-Gen2 interface
- 4 GB DDR3 memory
- No dedicated TCS interface

Time diagrams



Tclock = 8ns (125 MHz) from White Rabbit;
Reset Procedure <= 300 ms (depends on electronics);

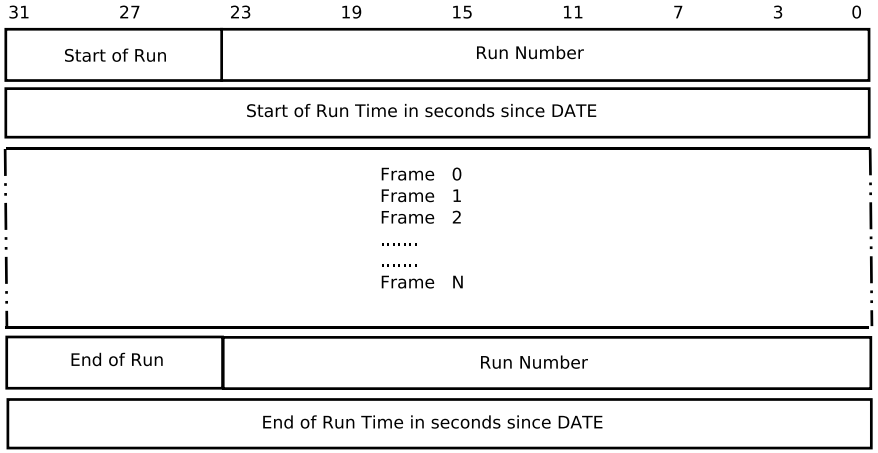
Slice Number: 24 bits (1 us - 8.3ms)
Data Size: max 16GB (real size < 160MB (20GB/s limit));

Frame: starts by Reset procedure, width 16 bits (min: 65ms, max: 549.7s),
Data Size: max 1PB (real size < 10TB (20GB/s limit))

Data Format

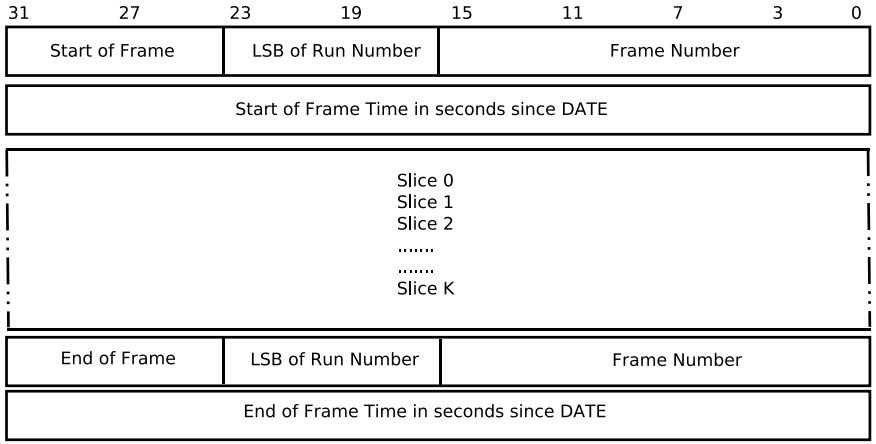
SPD Data Format

Run Structure:



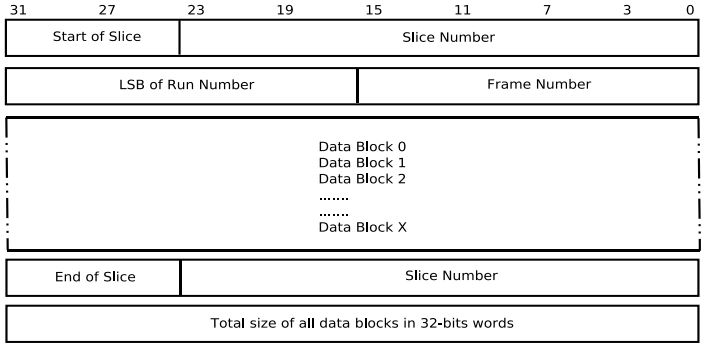
Number of Frames in the Run: 1-N, where N is maximal number of frames in the Run (assigned by TCS Controller)

Frame Structure:



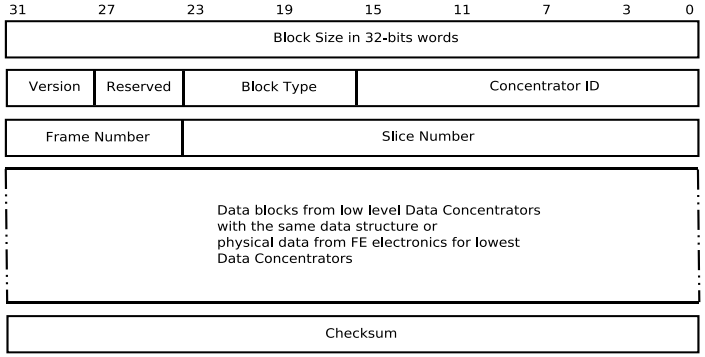
Number of Slices in the Frame: 1-K, where K is maximal number of slice in the Frame assigned by TCS Controller

Slice Structure:

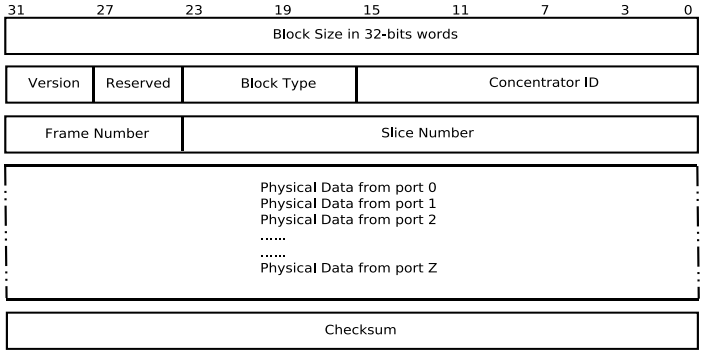


Number of Blocks in the Slice depends on DAQ configuration and data flux.

Data Block Structure of High Level Data Concentrators (Switches, Multiplexers etc.):



Data Block Structure of Lowest Level Data Concentrators (FE Concentrators):



Number of ports depends on FE Data Concentrator Type.
For instance, Igor Konorov ifTDC Multiplexer has 15 input ports.

Status

- AMBER/NA64 DAQ is scheduled to start to start 2-3 year before SPD. Its current status allows us to consider it as the good developed and tested prototype for SPD at the level of CDR.
- AMBER/NA64 DAQ consists of dedicated modules of 3 types only: two types of Data Handling multiplexer (DHmx and UDHmx), and Time Control System (TCS).
- We already have in Dubna 2 DHmx multiplexers and TCS module. That is enough for testing of Straw Tracker modules ONLY.

Problems

- We need to formalize our relations with developers of AMBER/NA64 DAQ modules from Technische Universität of München (TUM). In the best case they should join SPD collaboration in some way. In the worst case we need to find a group which will support these modules with a help of the TUM developers, or develop their own compatible modules.
- We start negotiation with a group from St.Petersburg Polytechnic University (SPbPU) as the candidate for such group. SPD relation with this group need to be formalized. The problem of technical documentation transfer form TUM to SPD and SPbPU becomes very actual.

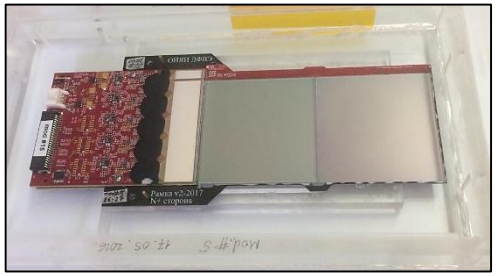
Silicon Vertex Detector Front-end electronics

25.03.2021

Relevant FEE DAQ numbers

# layer	1 (MAPS)	2 (MAPS)	3 (MAPS)	4 (DSSD)	5 (DSSD)	Total
Sensor numbers /layer	448	840	1736	228	368	596(DSSD) + 3024(MAPS)
Ladder numbers	11	20	28	19	23	101
Sensor numbers /stave (module)	28	28	28	2	2	
Numbers stave (modules)/layer	16	30	62	114	184	
Numbers e-links/stave	8	8	8			
Numbers analog MUX-OUT/module				10	10	
Read-out channels / layer	128 e-links	240 e-links	496 e-links	1140	1840	864 e-links + 2980 analog MUX-OUT

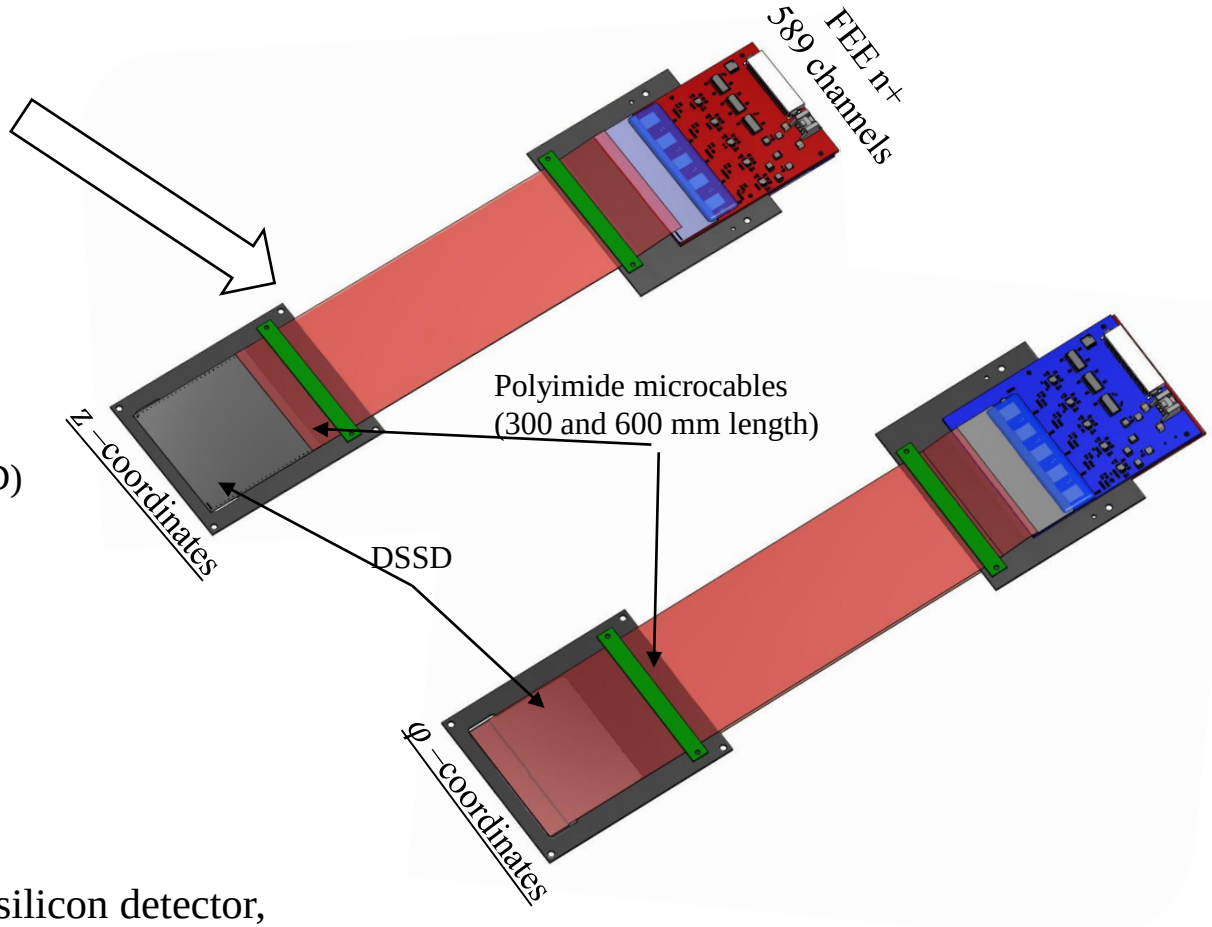
Current SPD Si module prototype



BM@N Si-Module

DSSD parameters:

- Size: 63x63x0.3 mm^3 (on 4" – FZ-Si wafers)
- Topology: double side microstrip (DSSD) (DC coupling)
- Pitch p^+ strips: 95 μm;
- Pitch n^+ strips 103 μm;
- Stereo angle between p^+/n^+ strips: 2.5^0
- Number of strips: 640 (p^+)× 614(n^+)

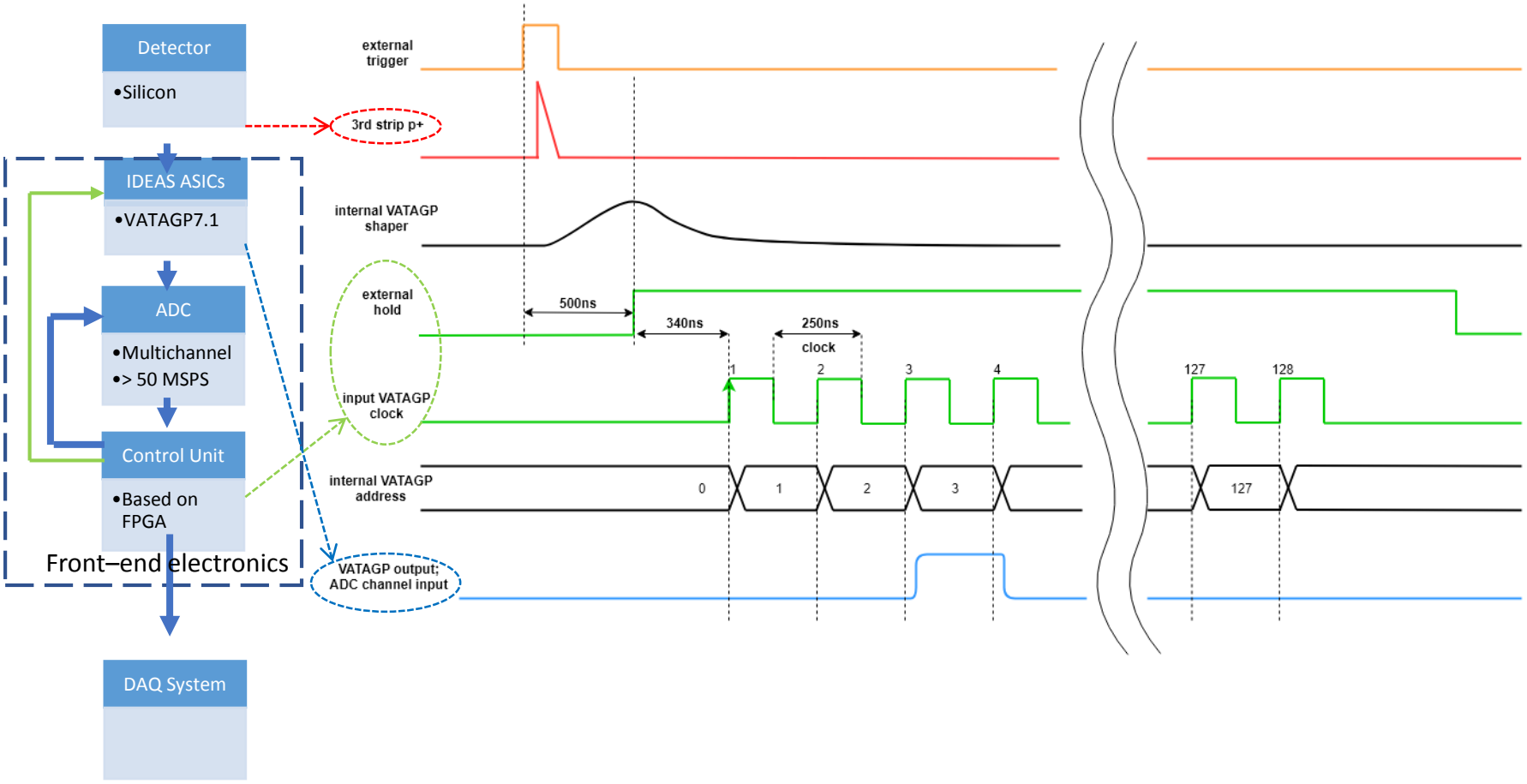


The module consists of one silicon detector, glued to the frame and connected with front-end electronics via thin polyimide cable. FEE based on VATAGP7.1 ASICs

Parameters of read-out chips

	ASIC VATAGP7.1
Number of CSA	128 channels
Input charges (dynamic range)	±30 fC
Peaking time (slow shaper)	500 ns (typ.)
Peaking time (fast shaper)	50 ns
Noise (ENC)	70e +12e/pF (typ.)
Lowest threshold (no capacitance)	0.12 fC
Voltage supply	+1.5V, -2.0 V
Gain from input to output buffer (diff. output currents)	16.5 μA/fC
Output Serial analog multiplexer clock speed	3.9 MHz
Power dissipation per channel	2.2 mW

Serial read-out diagram



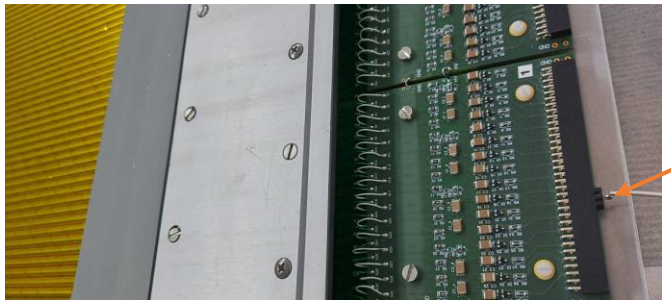
Possible solutions for ASIC read-out

ASIC	APV25	VATAGP7.3	n-XYTER	TIGER	ToASt
Channels number	128	128	128	64	64
Dynamic Range	-40fC ÷ 40fC	-30fC ÷ 30fC	Input current 10nA Polarity - and+	1÷50fC	1÷40fC
Gain	25mV/fC	20µA/fC	59.4 mV/fC	10.35mV/fc	ToT gain 40ns/fC
Noise	246e^-+36 e^-/pF	70e^-+12 e^-/pF	900e^- at 30pF	2000e^- at 100pF	1500e^-
Peaking time	50ns	50ns/500ns	30ns/ 280ns	60ns/ 170ns	50 / ≥ 100ns
Power consumption	1.15mW/ch.	2.18mW/ch.	10mW/ch.	12mW/ch.	4mW/ch.
ADC	No	No	16fC, 5 bit	10-bit Wilkinson ADC	8 bit
TDC	No	No	Timestamp resolution < 3.125ns	Timestamp resolution < 5ns	Timestamp resolution < 6.25ns

- Optimal choice of DSSD module ASIC should be done after ongoing R&D
- Choice of MAPS detector is not done.

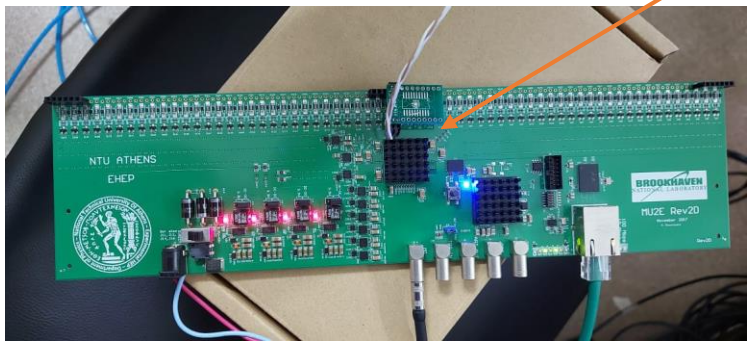
Straw tracker

Signals from STRAW chambers with ^{55}Fe



Adapter to get the signal from STRAW chamber

Adapter to delivery signal from STRAW chamber into the VMM3 board



Monitor output

Signal from monitor output.
^{55}Fe is attached to the STRAW chamber

Straw tracker. iFTDC

I.Konorov developed so-called “iFTDC” which is a TDC module built using FPGA chip.
iFTDC can work both in triggered or trigger-less mode (this has been tested and confirmed), has precision down to 150 ps: well above the requirements of the straw tracker.

5 card of iFTDC now is used for tests.

Straw tracker group is studying also other options for FEE.

iFTDC

Specification

- ARTIX7 FPGA XC7A-35
- 64 channels,
- Programmable signal edge or both edges
- **Bin size : 1 ns, 0.5 ns, 0.25 ns (32 channels)**
- **Time resolution : 300ps, 170 ps, 10 ps**
- **Differential nonlinearity : 10%, 20%, 40%**
- **Trigger less capable data flow**

Applications

- MWPC(tested), Drift Chambers
- Scintillation Counters with limited requirements for time resolution

TRACKER ELECTRONICS DUNA

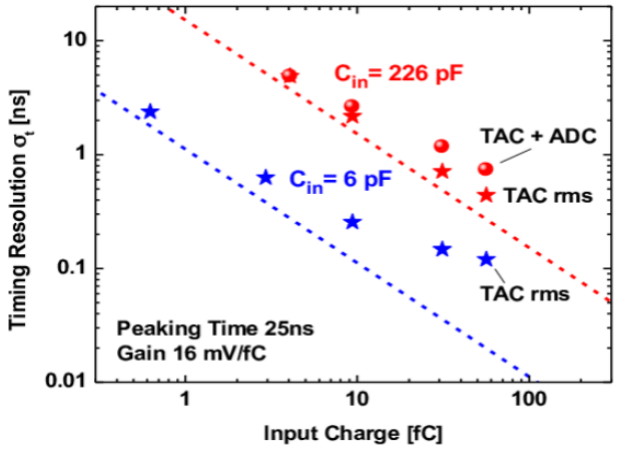


Figure 4: VMM3a time resolution as a function of input charge. Better than ns time resolution is obtained for suitably large deposited charge signals. [4]

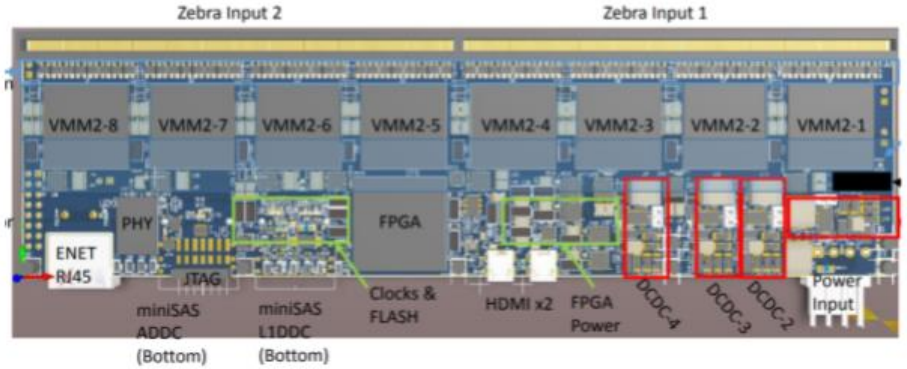
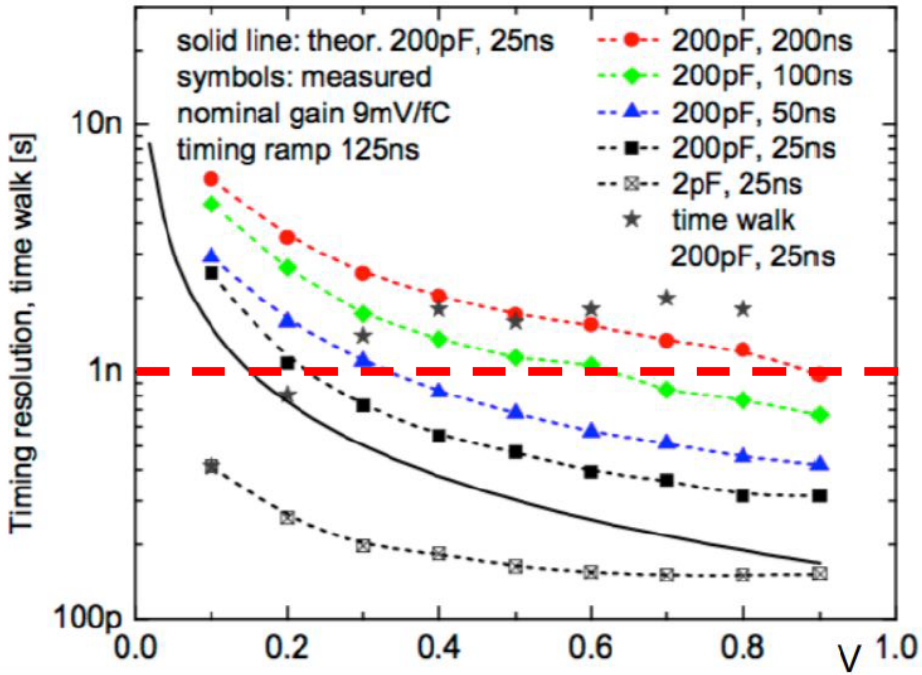


Figure 5: MMFE-8 readout board implements 8 VMM ASICs, equivalent to 512 channels, in a board with dimensions 215mm x 60mm x 2.54mm.

VMM3 Meets STT Readout Requirements

- Readout requirements:
  - Measure deposited charge & time t;
  - Timing resolution << 1ns;
  - Low threshold: charge from single ion pair;
  - Dynamic range > 1000 on charge;
  - Max width of readout board: 5cm;
  - Max length of readout board: 16 cm every 64 channels for double readout

VMM3 Time Resolution



- VMM3 satisfies required <1ns timing
- Measures Q + T for each input
- Built-in pulser for accurate electronic response calibration
- Compact 64-ch ASIC well suited to tight spatial constraints

G. Iakovidis, BNL

ECAL Front End Readout

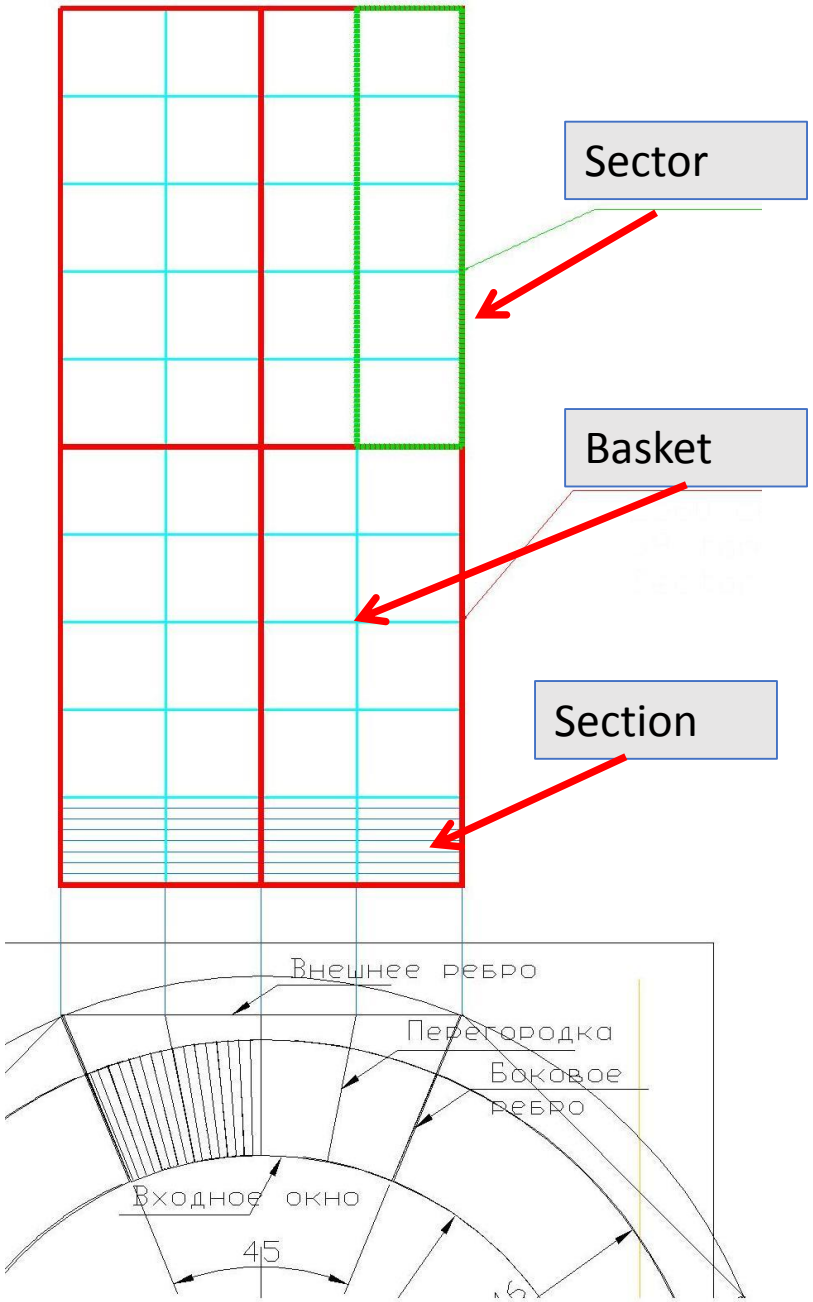
Front End electronic for SPD ECAL based of:

1. ADC-64 – 14 bit digitizer, 64 MHz – 64 channels

2. 16 channels Front END card with Power control for SiPms

3. 16 SiPM board + 1 Temperature sensor

Current version used for tests!!!



One Sector = 1/8 ECAL
The Frame divided on 8 Sectors

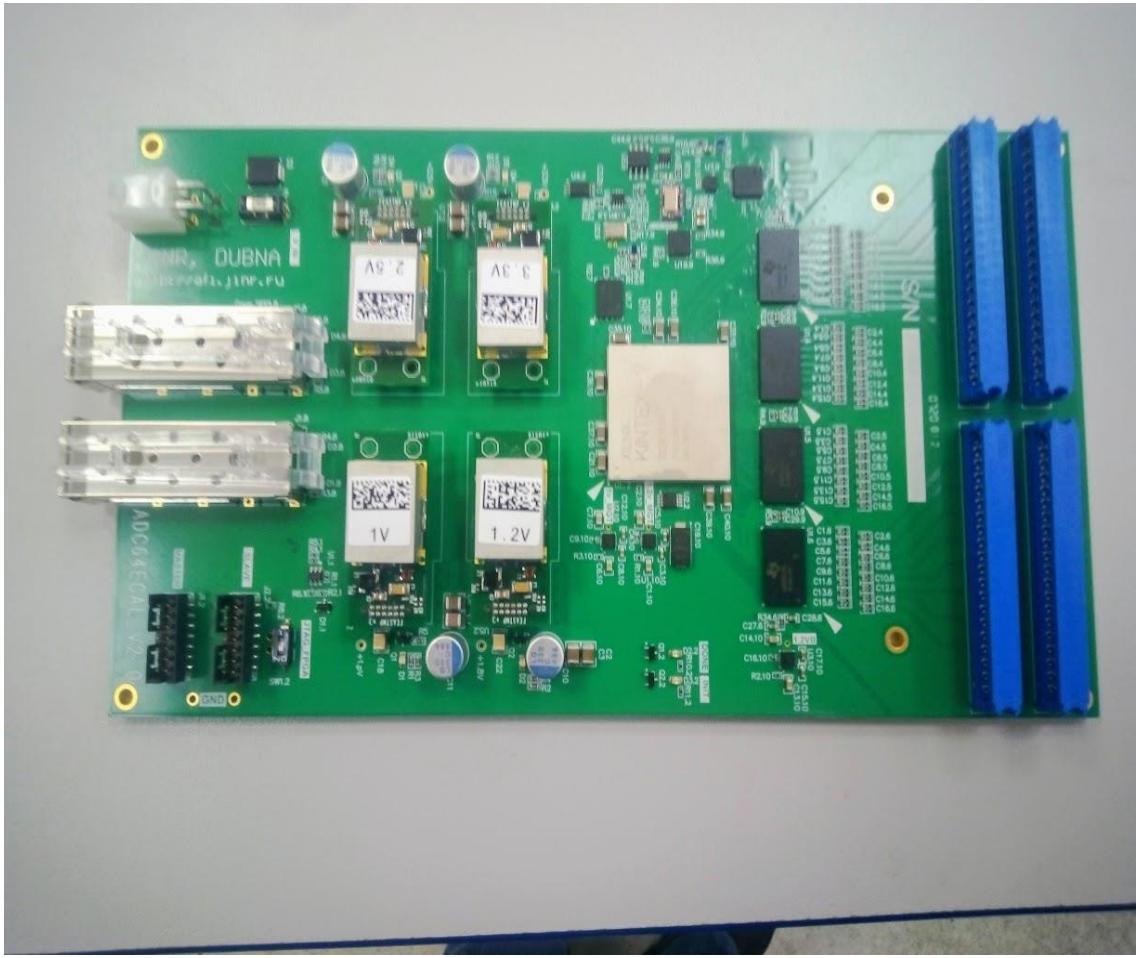
Each sector has 4 Gaskets
Each Gasket has 10 Sections
One Sector – consist of 64 cells
64 cells readout of one ADC-64

ADC-64 Numbers for:
One Sector = 40
One Barrel of 8 Sect.= 40x8=320
Two End Cups = 75x2=150

N_Front_End_Card=4 x N_ADC

64 channel Wave form digitizer Specially designed for ECAL

ADC_64Ecal – https://afi-project.jinr.ru/projects/adc64ecal/wiki

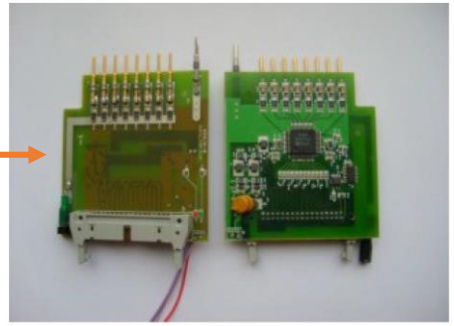


1. 64 MHz – samples frequency
2. 14 – bit/per sample
3. White Rabbit provides sub-nanosecond synchronization accuracy
4. Zero suppression mode
5. Can operate in Streamer mode – Trigger less DAQ
6. Water cooling
7. **Can operate** in Magnetic Field
8. Power : ~ 50 Wt.
9. Total heating: 470*50=23.5kW

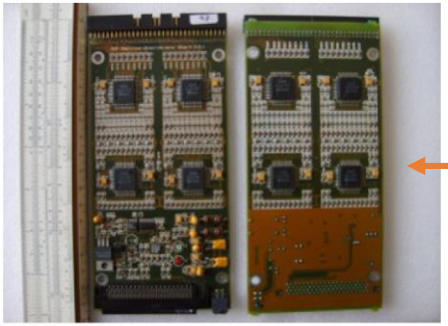
Muon (Range) System Front-End Electronics (analog & digital, FPGA-based)

Main FEE prototype cards (for test in BTZ)

Analog FEE card HVS/A-8 -> HVS/AD-8
(LVDS outputs to be implemented)



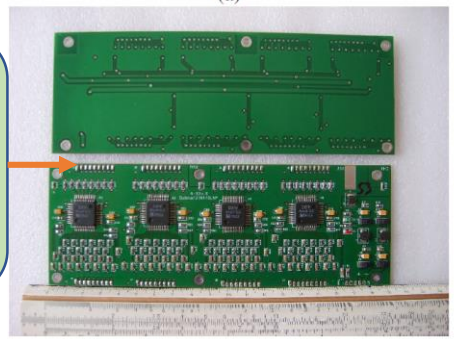
(a)



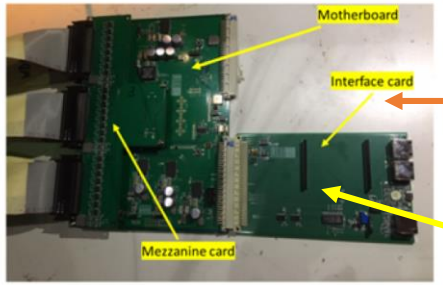
(b)

Analog FEE card ADB-32 for wire R/O
(no modifications)

Analog FEE card for strips R/O A-32 -> 2AD-32
(LVDS outputs to be implemented)



(c)



(d)

Digital FEE cards MFDM-192
(interface card for SPD/DAQ need to be developed

FE electronics of SPD RS (analog and digital)

Alekseev G., 25.03.2021

- **Analog electronics** based on two 8-channel chips: Ampl-8.3 и Disk-8.3, used in D0/FNAL и COMPASS/CERN
- It is paled to replace by: Ampl-8.51, Ampl-8.11R (will be ready by end of 2021) и Disk-8.15 (ready)
- **Digital electronics** based on FPGA chip Xilinx/Artix7. 192-channel VME units was developed and have been ordered (7pcs) for readout wires and strips (totally 1344 channels) from RS prototype (delivery - autumn 2021.)
- **RS Prototype test at Nuclotron** is fully covered with existing FEE. Analog cards ADB-32 should be delivered from CERN during this summer. The digital VME unit MFDM-192 need to be tested in the ideal case in autumn/winter 2021.

Front-End electronics summary

- Silicon vertex detector – TDC/ADC: few promising options is developing for PANDA and ALICE front-end electronics. No final decision yet.
- Electromagnetic calorimeter (SiPMs) – ADC: No final decision yet.
- Straw tracker: iFTDC developed for COMPASS, NA64 is planned for SPD or VMM3 based TDC/ADC.
- Range system – TDC: The SPD range system closely follows the design of the range system of PANDA, which is in a well-advanced state. The digital part of the PANDA front-end electronics is very closed to what we want for the SPD-DAQ.

SPD DCS & BTZ

29.04.2021 Tow talks:

- **SPD detector control system and Beam Test Zone, A. Chepurnov & D. Gribkov, SINP MSU: WinCC Open Architecture**

- **DCS of the miniSPD, Kirill Salamatin & Temur Enik, JINR: Tango**

DCS very short summery

Tango:

+ free system with open code
+ widely used in JINR
+ implemented at miniSPD

WinCC OA:

+ commercial system Simatic
+ standard for CERN
+ under consideration as standard for JINR !!!
+ gateway for Tango
+ will be implemented for RS in SPD beam test zone

- high price of the system and stuff education
- still not widely used in JINR

Thank you for attention