Vertex Detector SPD

B. Topko behalf Vertex Detector SPD team

SPD collaboration meeting

10 June 2021

Contents

- Performance requirements of the Vertex Detector (VD)
- VD general layout
- MAPS based layers
- DSSD based layers
- DSSD module layout
- DSSD module prototype
- Summary

Performance requirements of the Vertex Detector

From general conditions:

Close to 4π geometry;

Number of coordinate layers: ;

Vertex Detector (Version-1, CDR) based on two types Si-sensors

- Double Side Silicon Detector (DSSD) – outer 2 layers;
- MAPS (Monolitic Active Pixel Sensor) – inner 3 layers

Material budget of 1 layer DSSD include:

- Si (300 μm)= $0{,}003X_0$;
- Polyimide cable = $0{,}0016X_0$ (1 cable) ÷ $0{,}0048\ X_0$ (3 cables);
- Carbon frame=$0{,}005X_0$;

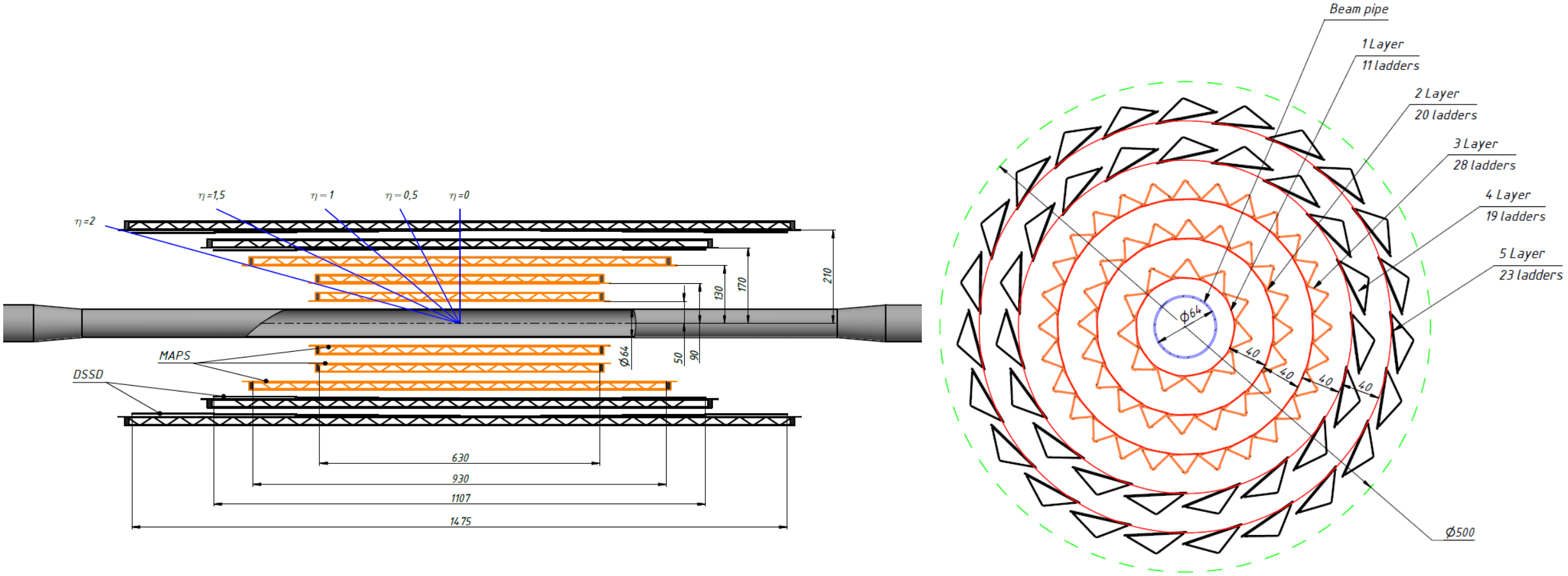
Barrel cover up to |η| =2;

End-cap cover up to |η| =2,5;

Track reconstruction efficiency for muons >99% at p≤ 13 GeV/c (for 0≤|η|≤2,5);

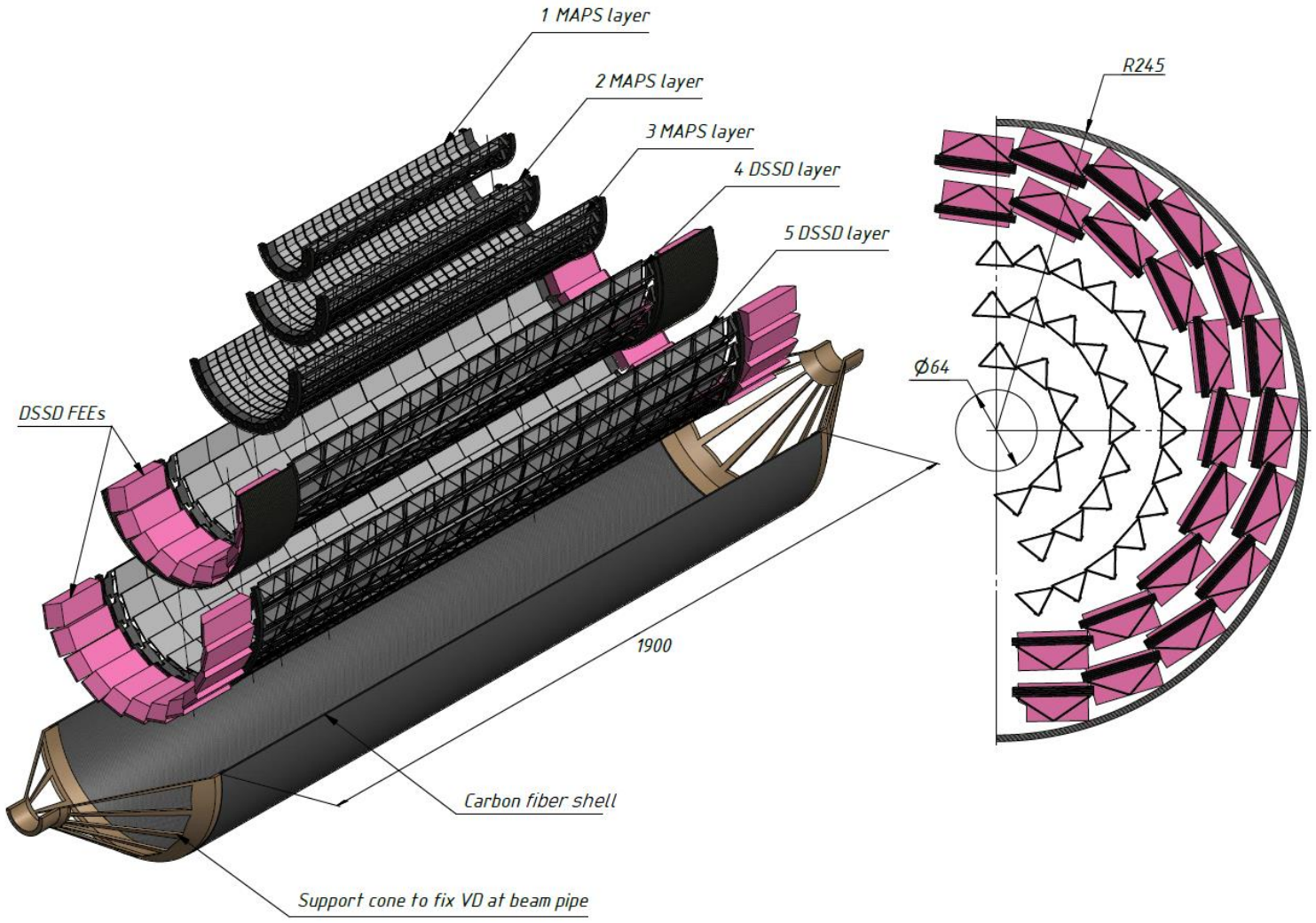
Coordinates resolutions: $\sigma_{r\varphi}$< 50 μm, σ_z < 100 μm.

VD general layout

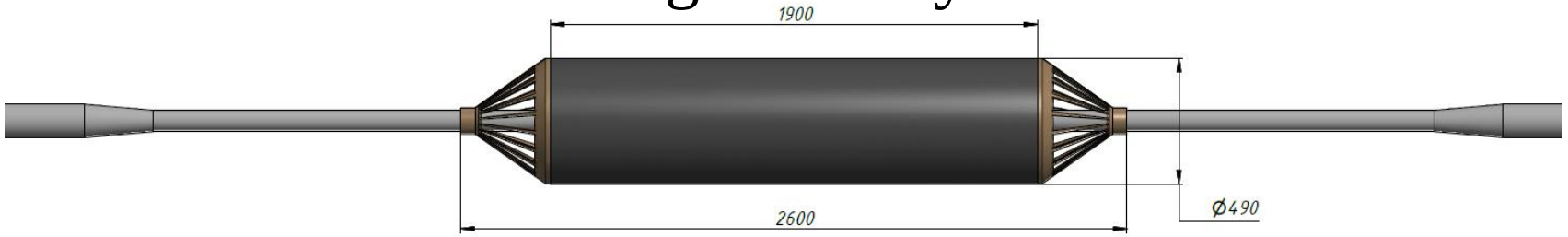


Longitudinal (left) and transversal (right) cross-sections of the DSSD+MAPS Vertex Detector barrel part

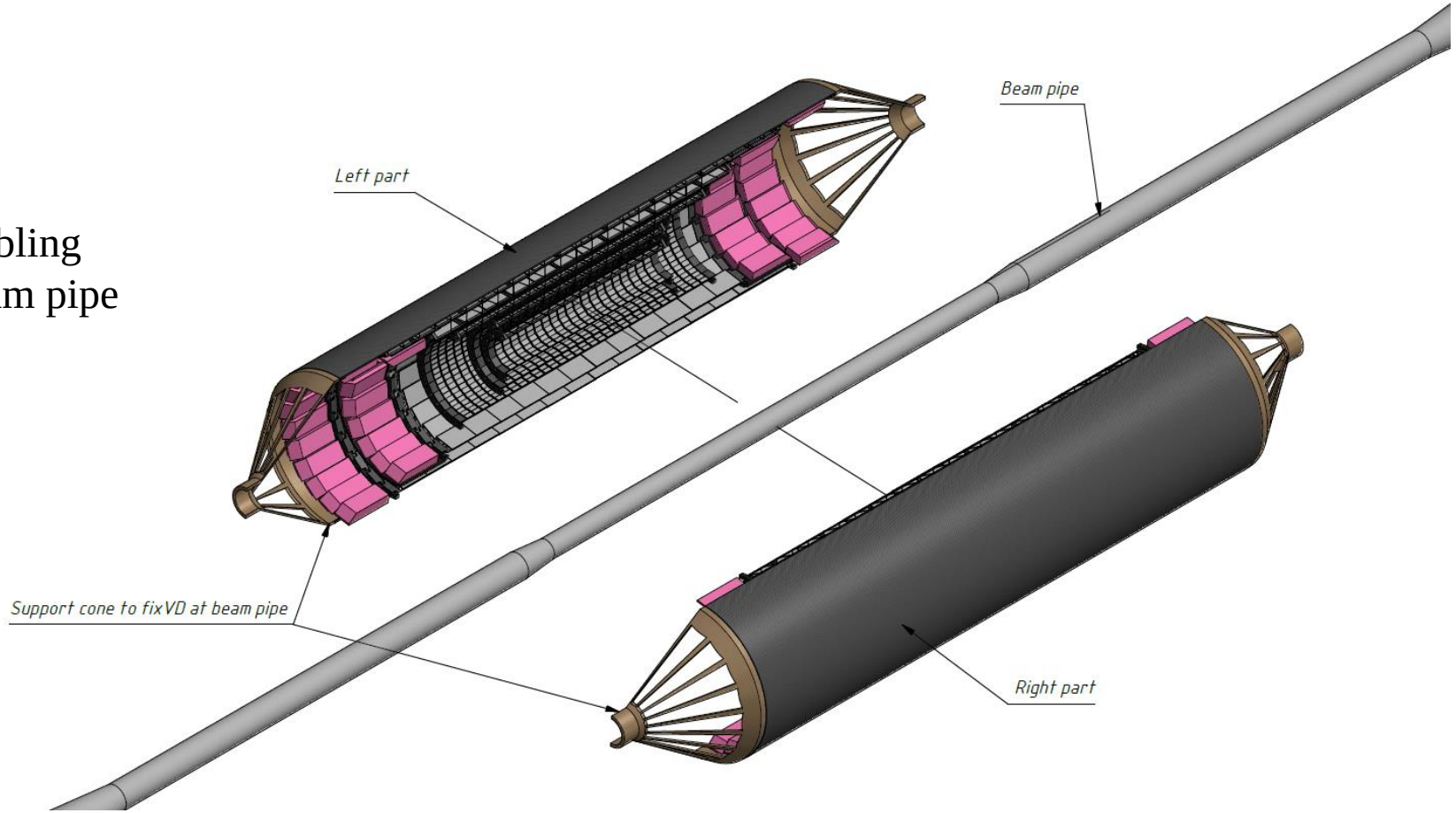
VD general layout



VD general layout

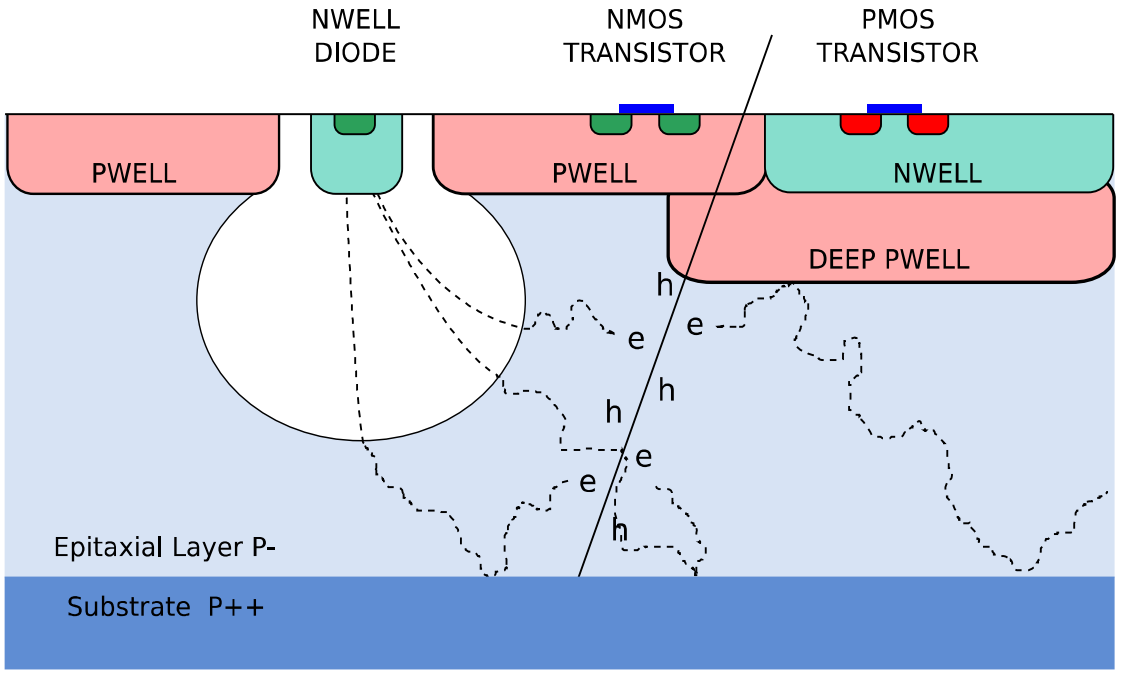


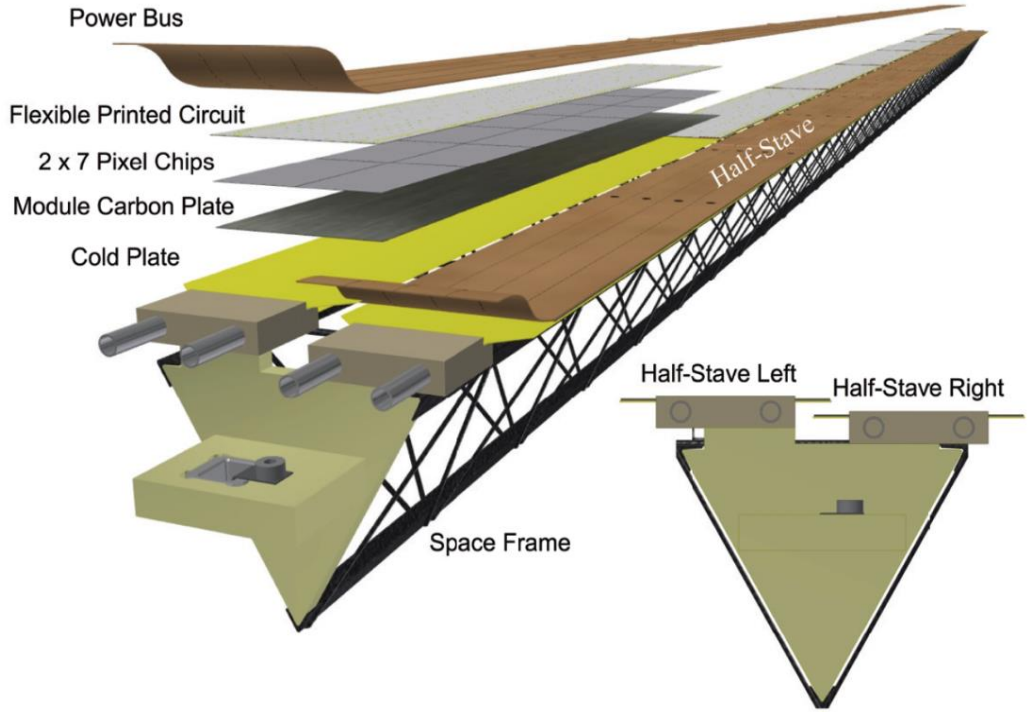
Possible VD assembling solution around beam pipe



MAPS based layers

Sensors will planned to be assembled to ladders such as ALICE outer barrel (OB) staves with two chips rows.

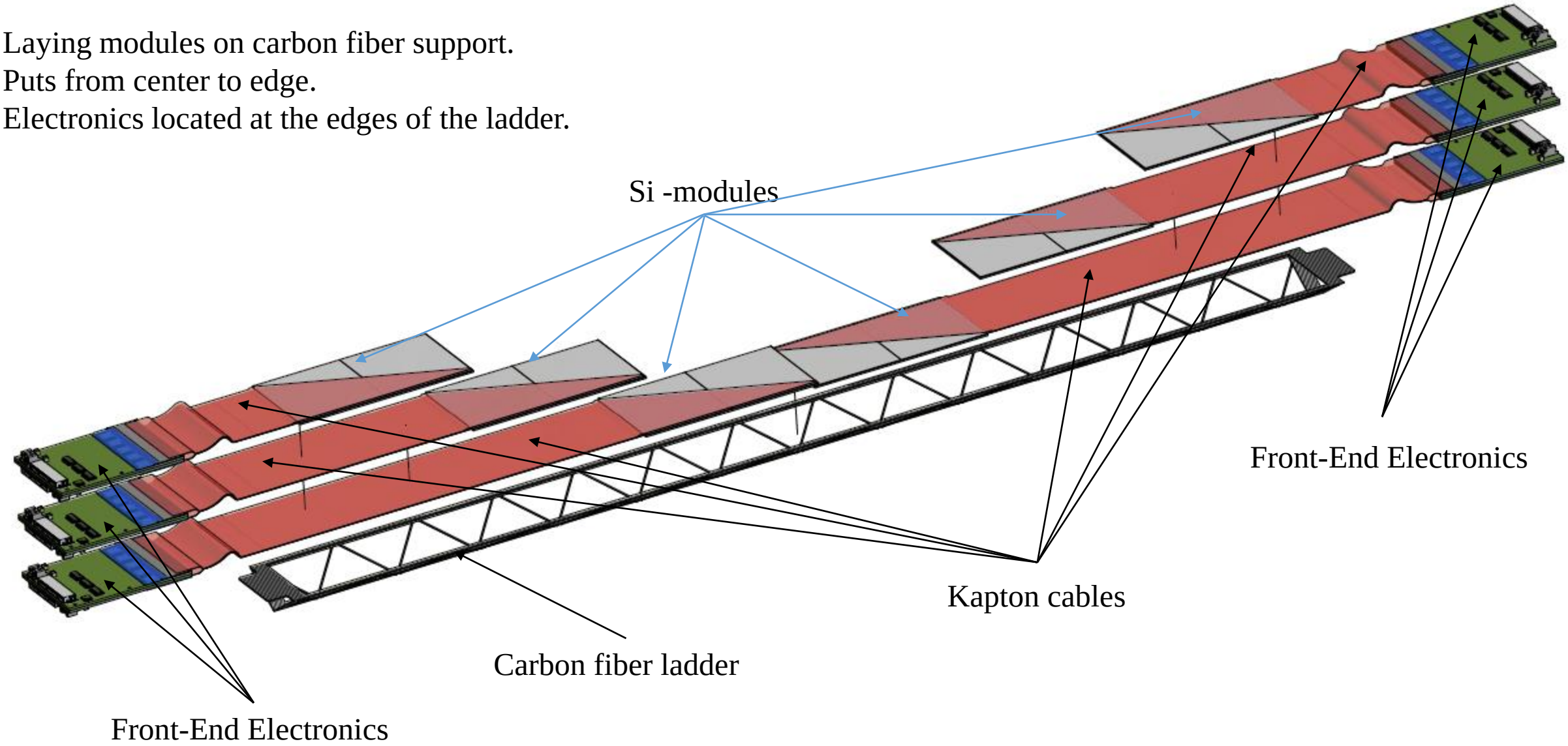




Schematic of MAPS pixels in imaging CMOS (left) and Schematic exploded view and cross section of the ALICE OB Stave (right) [ALICE Collaboration, TDR for the Upgrade of the ALICE Inner Tracking System Journal of Physics J. Phys. G 41 (2014) 087002]

DSSD based layers

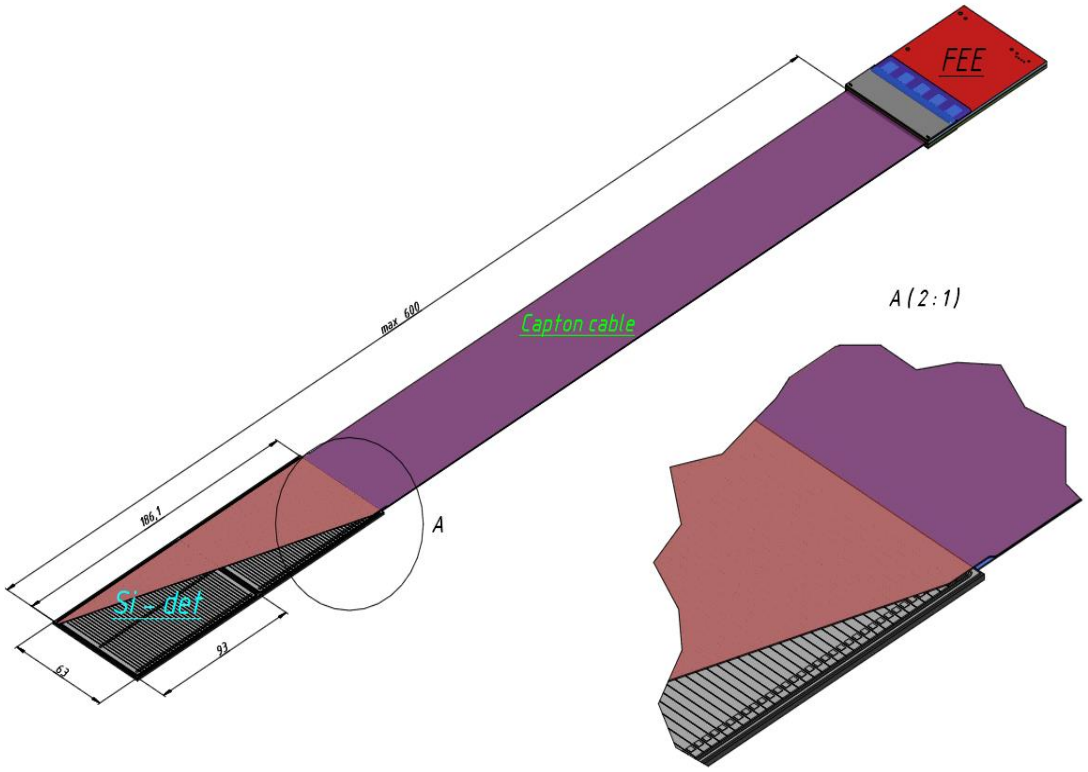
Laying modules on carbon fiber support.
Puts from center to edge.
Electronics located at the edges of the ladder.



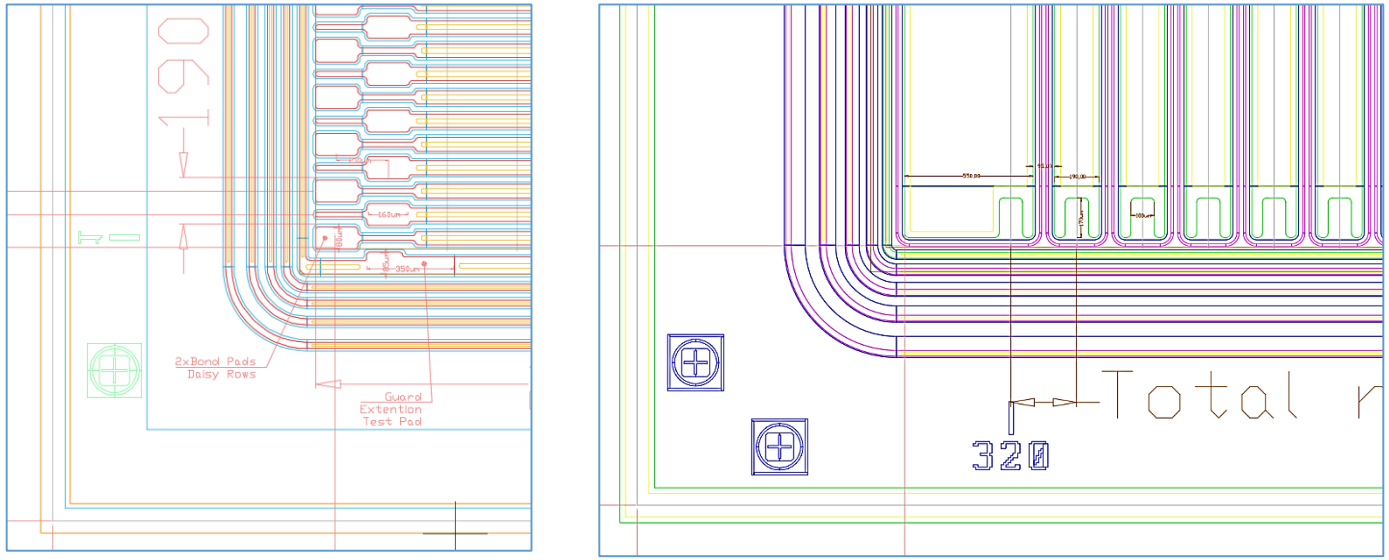
Barrel DSSD module concept

DSSD parameters:

- Size: 63x93x0.3 mm^3 (on 6” – FZ-Si wafers)
- Topology: double side microstrip (DSSD) (DC coupling)
- Pitch p^+ strips: 95 μm;
- Pitch n^+ strips 281.5 μm;
- Stereo angle between p^+/n^+ strips: 90^0
- Number of strips: 640 (p^+)× 320(n^+)
- Number of strips per module: 640 (p^+)× 640(n^+)



Barrel DSSD module 3D model



Low left corner of detector photomask p+ side (left) and n+ side (right) (ZNTC, Zelenograd, Russia)

Low-mass microcables

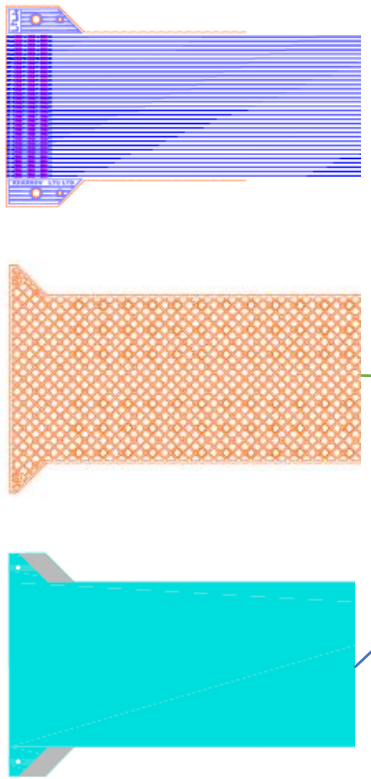
Manufacturing: LED Technologies Ukraine. Ukraine, Kharkiv
viatcheslav.borshchov@cern.ch, maksym.protsenko@cern.ch

Maximum cable length 600 mm

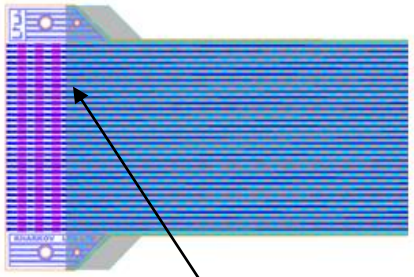
FDI-A-24
Signal layer
Al 14 µm ($x/X0=2,46\cdot10^{-5}$)
Polyimide 10 µm ($x/X0=5,83\cdot10^{-5}$)

Polyimide layer
(perforated or solid)
Polyimide 50÷100 µm
($x/X0=(1,23\div2,46)\cdot10^{-4}$)

Shielding layer
Al 14 µm ($x/X0=1,2\cdot10^{-4}$)



The combination of signal and shielding layers



Additional holes for combining layers

Possible solutions for ASIC read-out

ASIC	APV25	VATAGP7.3	n-XYTER	TIGER	ToASt
Channels number	128	128	128	64	64
Dynamic Range	-40fC ÷ 40fC	-30fC ÷ 30fC	Input current 10nA Polarity - and+	1÷50fC	1÷40fC
Gain	25mV/fC	20μA/fC	59.4 mV/fC	10.35mV/fc	ToT gain 40ns/fC
Noise	246e^-+36 e^-/pF	70e^-+12 e^-/pF	900e^- at 30pF	2000e^- at 100pF	1500e^-
Peaking time	50ns	50ns/500ns	30ns/ 280ns	60ns/ 170ns	50 / ≥ 100ns
Power consumption	1.15mW/ch.	2.18mW/ch.	10mW/ch.	12mW/ch.	4mW/ch.
ADC	No	No	16fC, 5 bit	10-bit Wilkinson ADC	8 bit
TDC	No	No	Timestamp resolution < 3.125ns	Timestamp resolution < 5ns	Timestamp resolution < 6.25ns

FEE ASIC R&D

TIGER ASIC specification → ToASt ASIC specification

Parameter	*Value*		*Value*
Number of channels	64		64
Input dynamic range	2-50 fC		1-40 fC
Input capacitance	up to 100 pF		2-17 pF
ENC	< 2000 e^-		1500 e^-
Maximum event rate	60 kHz/channel		40 kHz/channel
Serial links	4		2
Pads position	around the chip		on two sides only
Trigger-less	✓		✓
Power consumption	10-12 mW/channel		4 mW/channel

ToASt ASIC advantages:

- ✓ not necessary to be redesigned – ASICs could be placed on PCB tighter;
- ✓ based on simulations input dynamic range is up to 50 fC;
- ✓ available at the beginning of next year.

**based on discussions with Maxim Alexeev (INFN, Torino)*

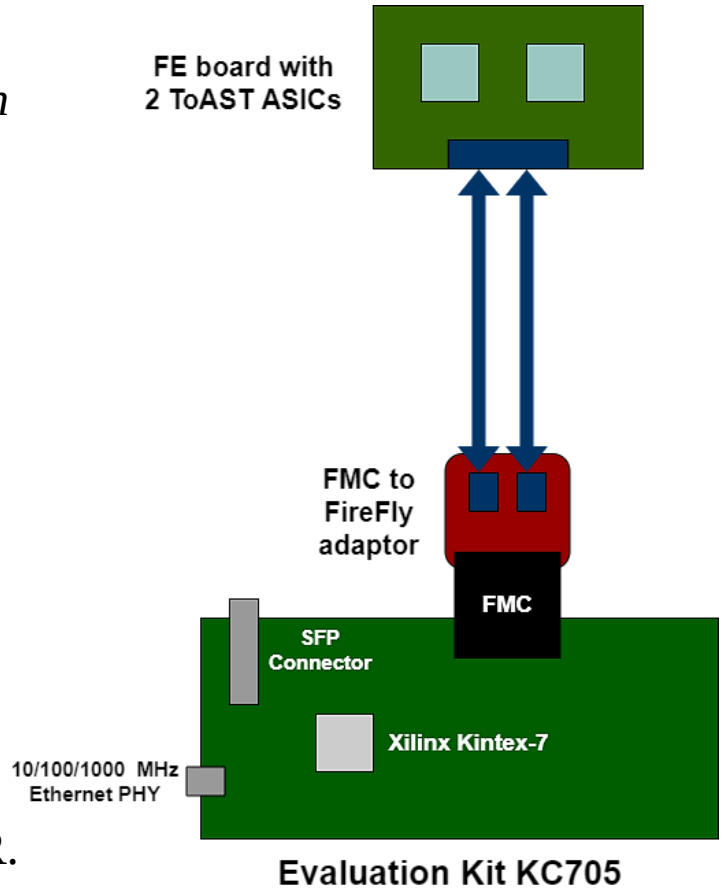
FEE ASIC R&D

FEE ToAST tests are foreseen at the beginning of next year

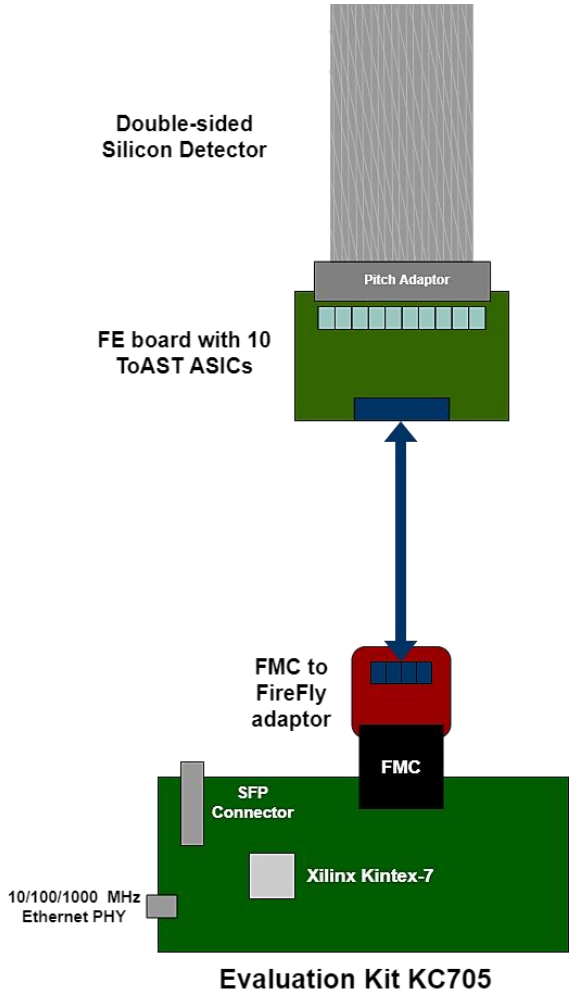
First stage:

Test preparation scenario:

- design PCB for 2 ToAST ASICs *(in JINR)*;
- Wire bonding (*in Torino / JINR)*;
- FPGA design for slow control and data acquisition *(in JINR)*;
- PC application to send ASIC settings and analyze data *(in JINR)*;
- Run tests in JINR.



Second stage:



Test preparation scenario:

- design PCB for 10 ToAST ASICs *(in JINR)*;
- Wire bonding ToAST to Pitch Adapter (*in Torino / JINR)*;
- Wire bonding FEE board to DSSD (*in JINR*);
- Run tests in JINR.

**based on discussions with Maxim Alexeev (INFN, Torino)*

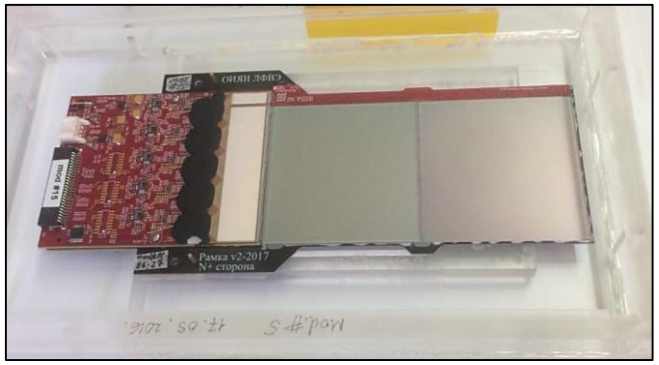
Relevant VD SPD numbers

Parameter	Layer 1 (MAPS)	Layer 2 (MAPS)	Layer 3 (MAPS)	Layer 4 (DSSD)	Layer 5 (DSSD)	Total for layer 1,2,3	Total for layer 4,5	Total
N_{MAPS}/mod	1	1	1	0	0	-	-	-
N_{DSSD}/mod	0	0	0	2	2	-	-	-
R_{layer}, mm	50	90	130	170	210	-	-	-
L_{layer}, mm	600	630	930	1107	1475	-	-	-
$N_{ladders}$/layer	11	20	28	19	23	59	42	101
N_{MAPS}/layer	448	840	1736	0	0	3024	0	3024
N_{DSSD}/layer	0	0	0	228	368	0	596	596
N_{ASIC}/mod	0	0	0	10	10	-	-	-
N_{ASIC}/layer	0	0	0	1140	1840	-	2980	2980
$N_{read\text{-}out\ channel}$/ layer	128 e-links	240 e-links	496 e-links	1140 analog MUX-OUT	1840 analog MUX-OUT	864 e-links	2980 analog MUX-OUT	864 e-links + 2980 analog MUX-OUT
S_{active}, m^2	0.20	0.38	0.78	1,34	2.16	1.36	3.5	4.86

Barrel DSSD module prototype

From general conditions of SPD facility it's necessary to minimize material budget over the track paths. That's why the main goal of prototype is to study possibility of production double-sided silicon strip detector (DSSD) module which connects to front-end electronics via thin low-mass microcables and test it for satisfaction m.i.ps detection (noise, cross-talks, common noise).

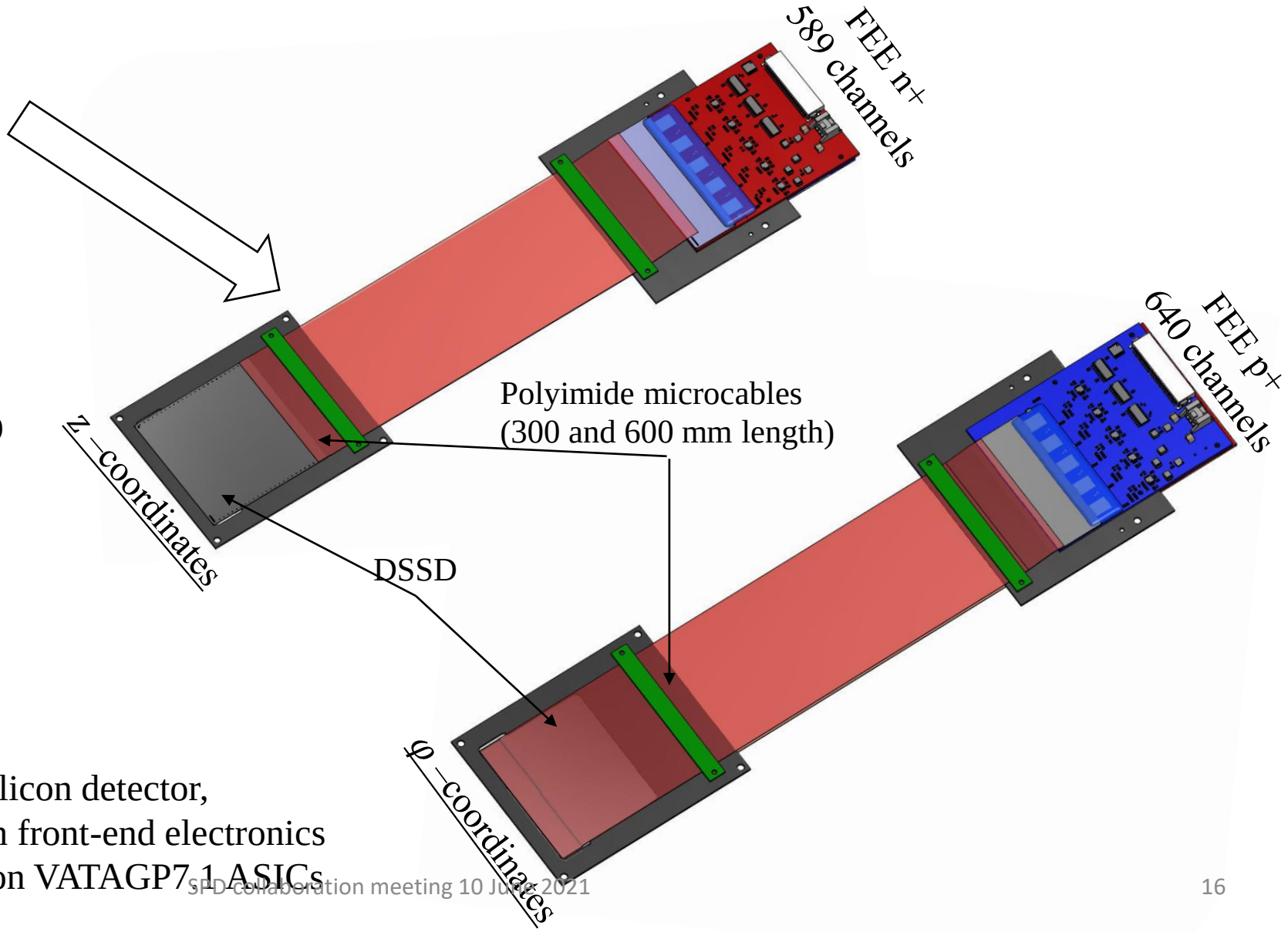
Barrel DSSD module prototype



BM@N Si-Module

DSSD parameters:

- Size: 63x63x0.3 mm^3 (on 4” – FZ-Si wafers)
- Topology: double side microstrip (DSSD) (DC coupling)
- Pitch p$^+$ strips: 95 μm;
- Pitch n$^+$ strips 103 μm;
- Stereo angle between p$^+$/n$^+$ strips: 2.5^0
- Number of strips: 640 (p$^+$)× 614(n$^+$)



The module consists of one silicon detector, glued to the frame and connected with front-end electronics via thin polyimide cable. FEE based on VATAGP7.1 ASICs

Low-mass microcables for prototype

Manufacturing: LED Technologies Ukraine. Ukraine, Kharkiv
viatcheslav.borshchov@cern.ch, maksym.protsenko@cern.ch

4 different cable topologies had been developed for DSSD barrel module prototype:

- «SPD-600-1»

Cable length is 600 mm. Signal layer consists of 1 conductive layer with meshed gaskets SPD-P-600-1 (for p+ side), SPD-N-600-1 (for n+ side) + 2 shielding layers;

- «SPD-300-1»

Cable length is 300 mm. Signal layer consists of 1 conductive layer with meshed gaskets SPD-P-600-1 (for p+ side), SPD-N-600-1 (for n+ side) + 2 shielding layers;

- «SPD-600-2»

Cable length is 600 mm. Signal layer is splitted to 2 conductive layers with meshed gaskets SPD-P-600-2-bot, SPD-P-600-2-top, SPD-N-600-2-bot, SPD-N-600-2-top + 2 shielding layers;

- «SPD-300-2»

Cable length is 300 mm. Signal layer is splitted to 2 conductive layers with meshed gaskets SPD-P-600-2-bot, SPD-P-600-2-top, SPD-N-600-2-bot, SPD-N-600-2-top + 2 shielding layers;

Photo of SPD-300-2 signal layers (n+ side) at top; Shielding layers at bottom

Low-mass microcables for prototype

Manufacturing: LED Technologies Ukraine. Ukraine, Kharkiv
viatcheslav.borshchov@cern.ch, maksym.protsenko@cern.ch

Signal layer:

Conductive layer – Aluminium 14 mkm;

Insulator layer – Polyimide 10 mkm;

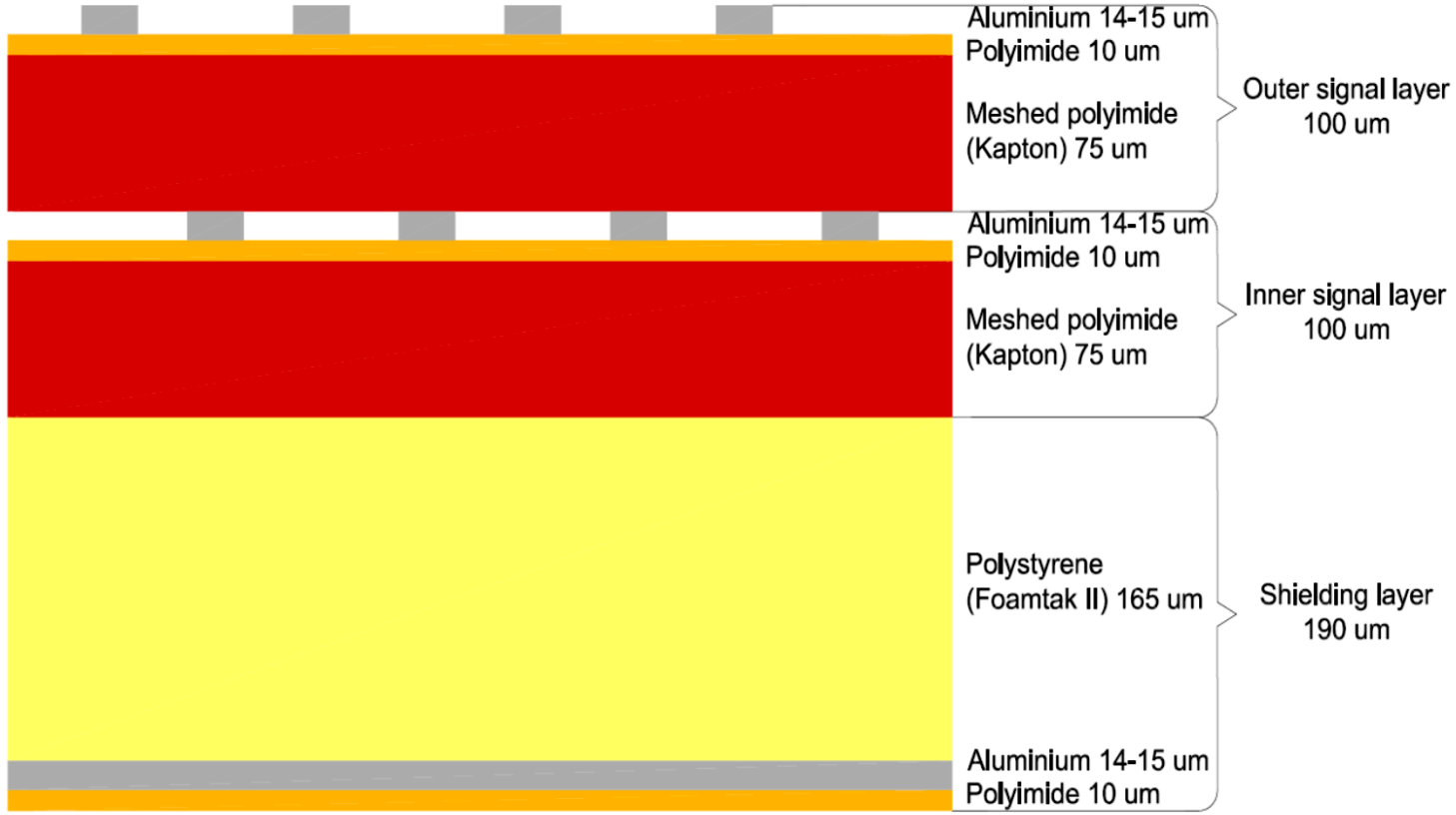
Meshed gasket – meshed Polyimide 75 mkm, (filling 30%).

Shielding layer:

Conductive layer– Aluminium 14 mkm;

Insulator layer – Polyimide 10 mkm;

Gasket – Foamtak (polystyrene) 160 mkm.



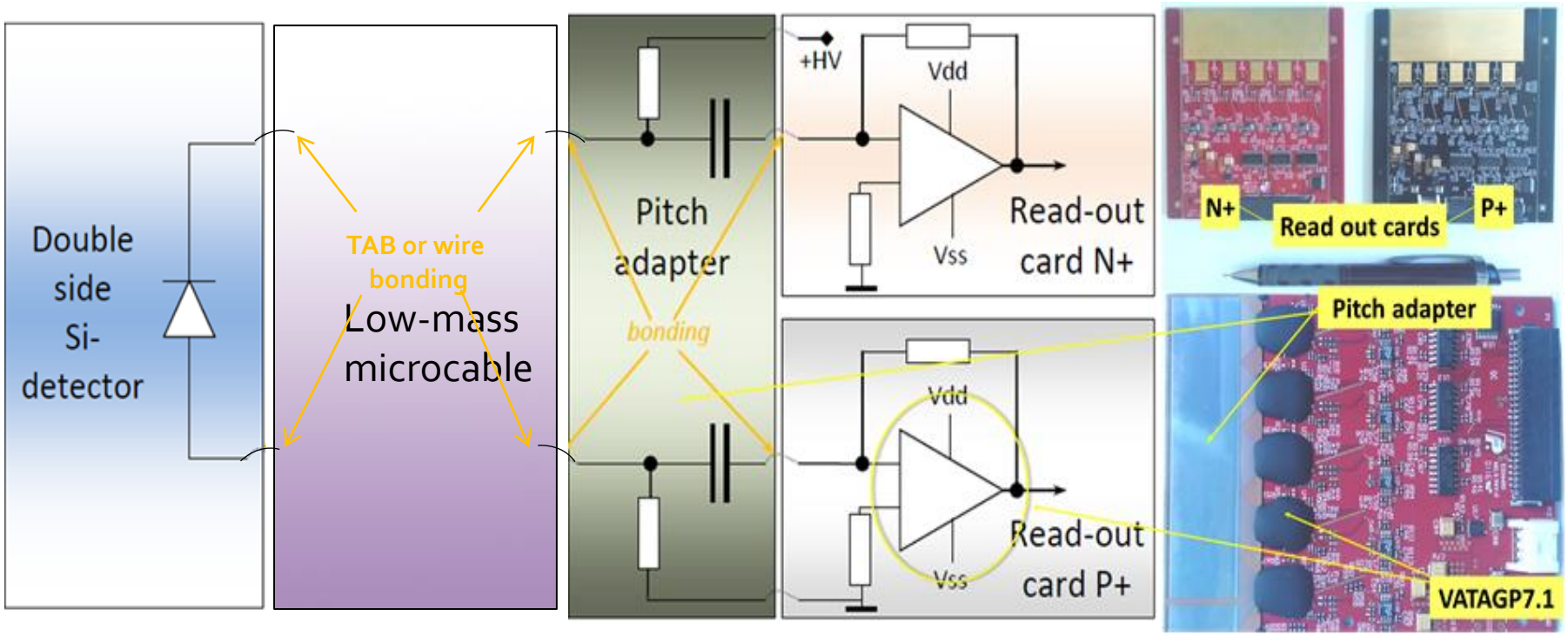
Cable cross-section with splitted signal layer

Low-mass microcables for prototype

Manufacturing: LED Technologies Ukraine. Ukraine, Kharkiv
viatcheslav.borshchov@cern.ch, maksym.protsenko@cern.ch

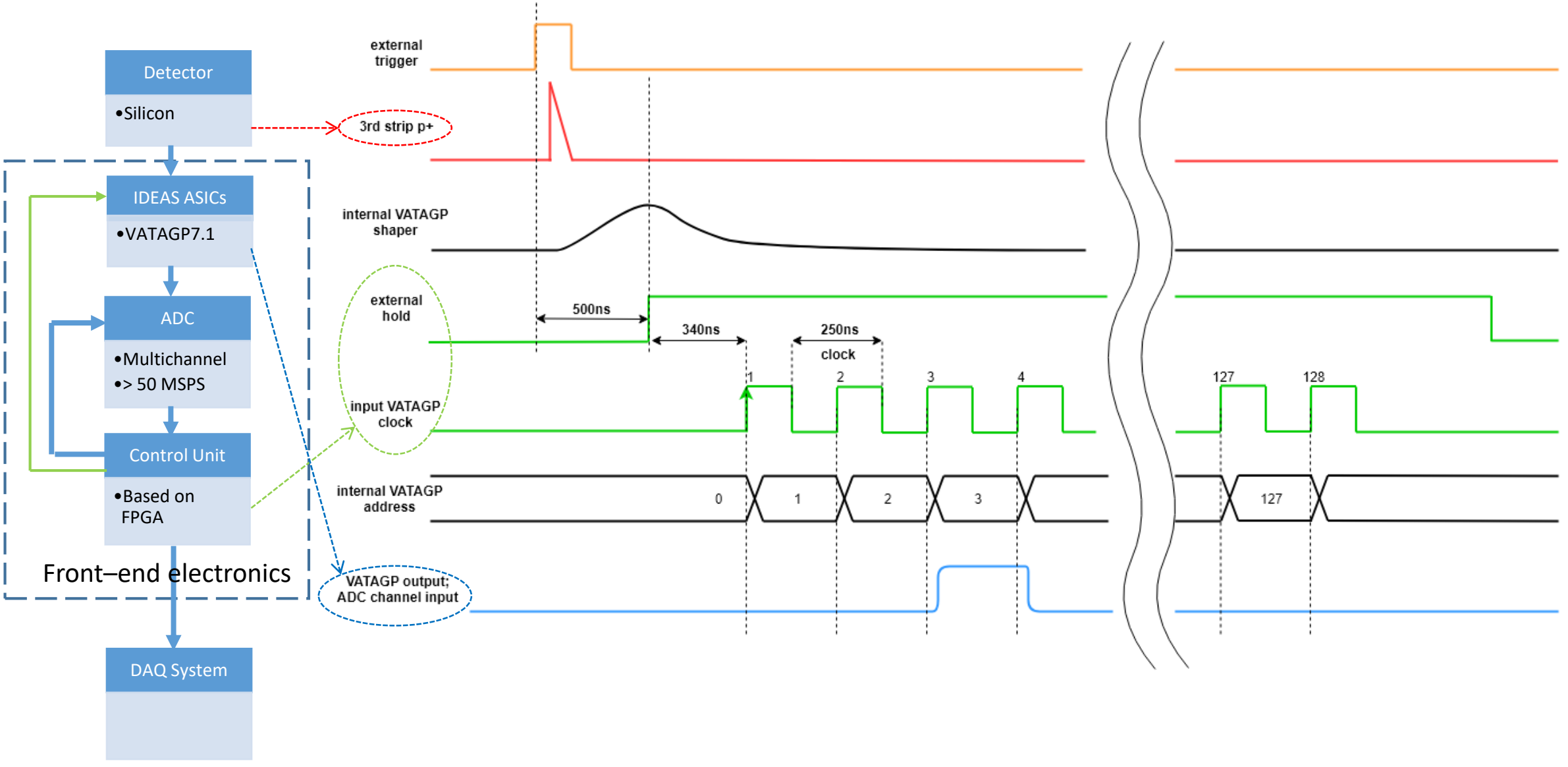
SPD-1		**X0 – radiation length**		
Layer type	**Material**	**X0, mkm**	**Thickness, mkm**	**X0, %**
Signal layer	Aluminium	87000	28	0,032
Signal layer	Polyimide	284000	20	0,007
Signal layer(30%)	Polyimide	284000	45	0,016
Shielding layer	Aluminium	87000	28	0,032
Shielding layer	Polyimide	284000	20	0,007
Shielding layer	Foamtak			
			Total X0, %	**0,094**
SPD-2				
Layer type	**Material**	**X0, mkm**	**Thickness, mkm**	**X0, %**
Signal layer	Aluminium	87000	28	0,032
Signal layer	Polyimide	284000	40	0,014
Signal layer(30%)	Polyimide	284000	90	0,032
Shielding layer	Aluminium	87000	28	0,032
Shielding layer	Polyimide	284000	20	0,007
Shielding layer	Foamtak			
			Total X0, %	**0,117**

Pitch adapter



DSSD with DC topology doesn't contain integrated resistors and capacitors (RC), therefore external R, C are required to supply bias voltage to each strip and to electrically decouple the DC current from the electronic inputs. This role is performed by Pitch Adapter (PA) with a topology of two types for p+ and n+ sides of the detector. In addition, PA has topology of contact pads similar to chips located on the side of electronic chips. PA modules are made on sapphire plates with an epitaxial layer of silicon (SOI). Integrated poly silicon bias resistors have a value of 0.7 – 1.0 MΩ, decoupled capacitors have a value of 140 pF. PA is assembled together with read-out ASICs on the read-out card. Positive polarity signals come from detectors to P+ read-out card (black PCB) while negative signals come to N+ read-out card (red PCB).

Serial read-out diagram



Summary

- First hybrid (3 MAPS layers + 2 DSSD layers) version of barrel part VD SPD conceptual design is done;
- Availability of MAPS in Russia is still open question;
- New DSSDs topology with large sensitive area 63x93 mm^2 is done. Detectors will be delivered at JINR till end of this year;
- At the moment DSSD FEE based on ToASt ASIC is the most promising way (tests are foreseen at the beginning of next year);
- First version of Barrel Silicon Module prototype for Vertex Detector SPD is going to be based on the BM@N modules (DSSD, 300 μm, 2.5° stereo angle between strips, DC coupling). Now there are enough amount detectors, pitch adapters, ASICs and low-mass microcables for the prototype;
- Drawings of prototype support frames and assembly jigs in progress.

Welcome everyone to join the Vertex Detector SPD collaboration!