DAQ for SPD

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on behalf of SPD DAQ group

Estimation of raw data flow

Bunch crossing each 80 ns; crossing rate 12.5 MHz,
Collision rate ~3–4 MHz →
Triggerless DAQ to avoid any hardware biases

Data flux was estimated for the maximum luminosity $L = 10^{32}$ $cm^{-2}c^{-1}$ and maximum energy $\sqrt{s} = 27$ GeV.

Within simplified simulation and some safety margin the data flux is estimated as 20 GBytes/s.

Front-end electronics for the free-running DAQ-SPD

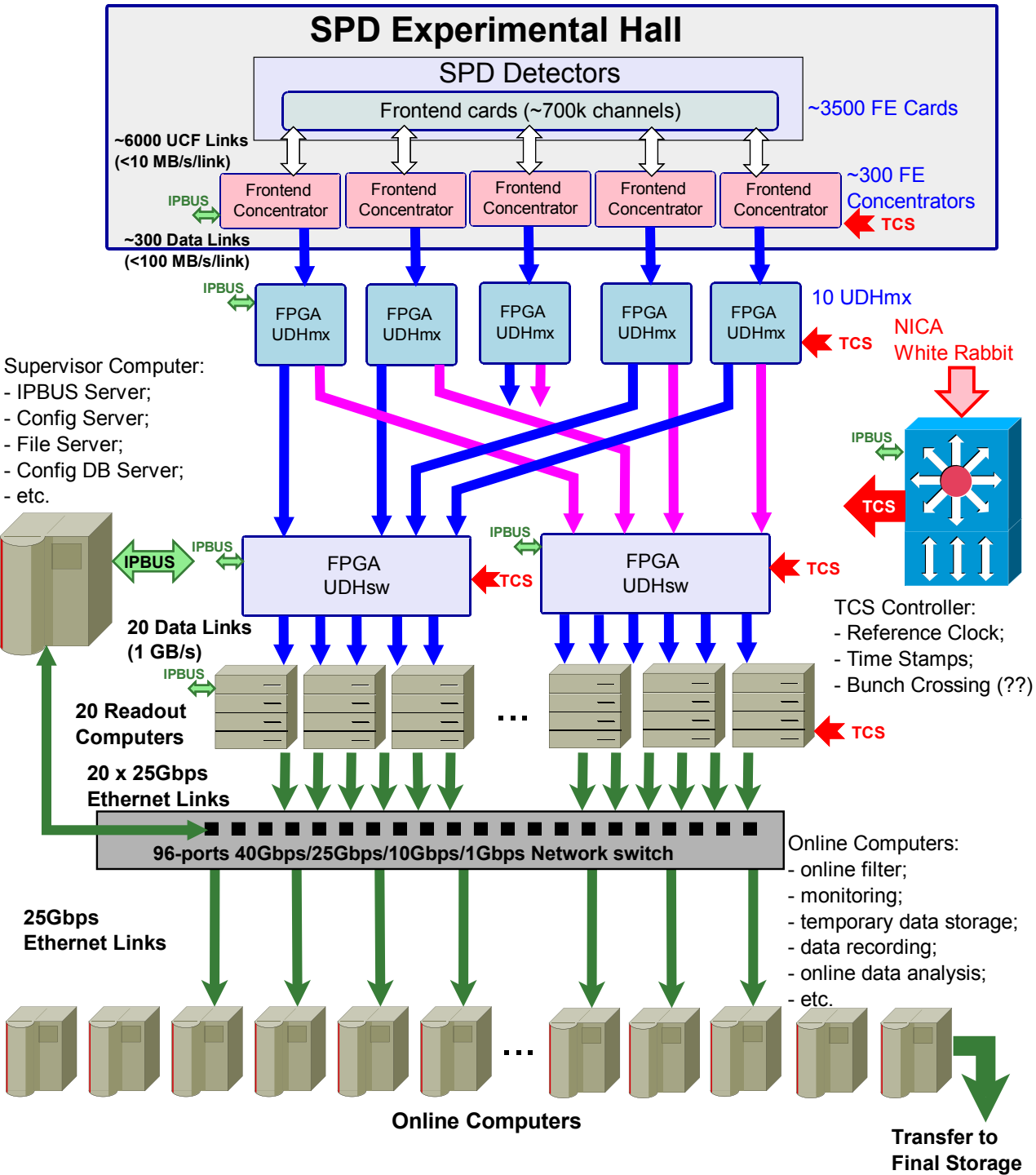
Front-end electronics of the detectors has to meet the requirements of a free-running DAQ

General FEE requirements from the DAQ system:

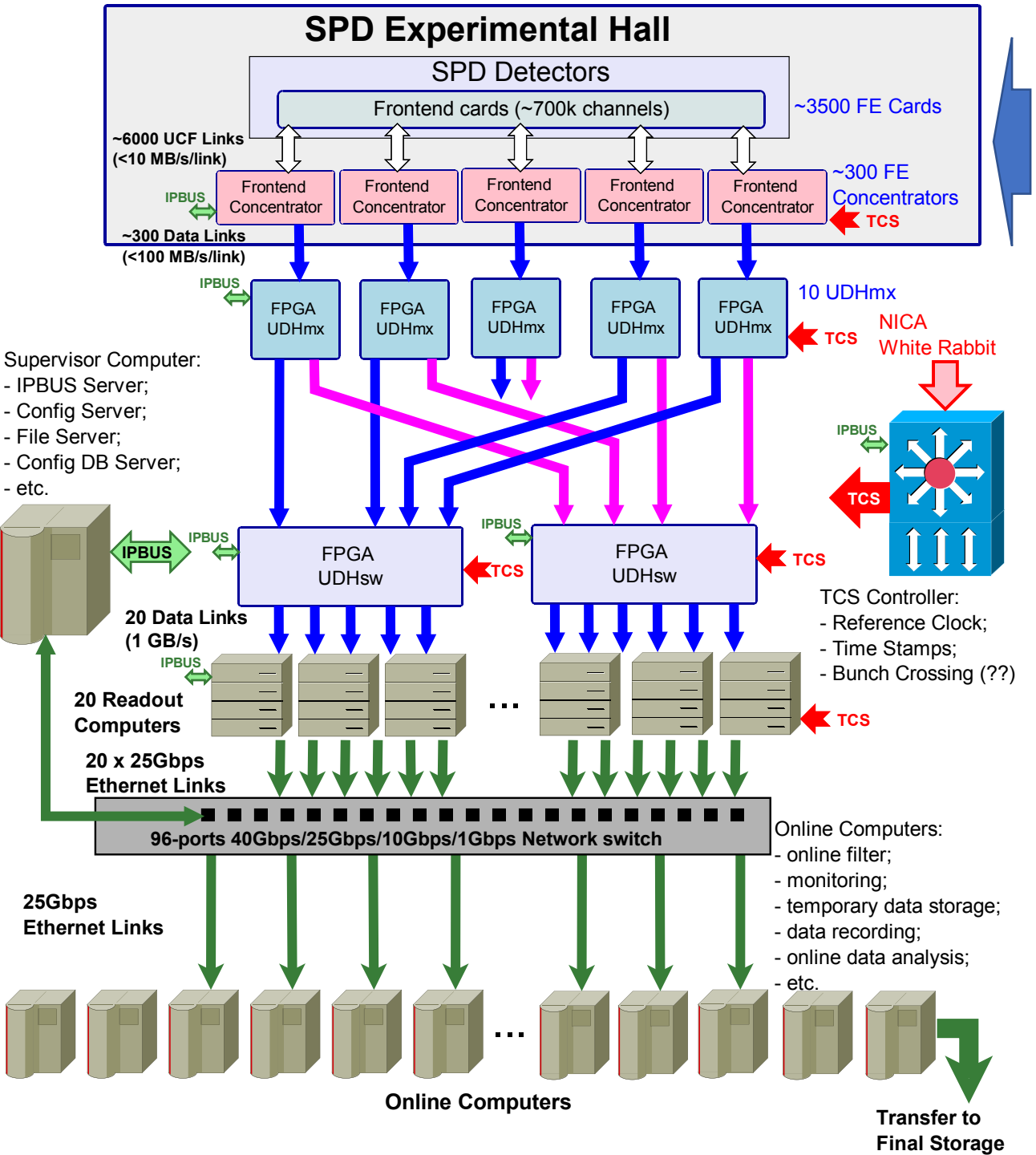
- Self-triggered (*trigger-less*) FEE operation
- Digitizing on-board
- Timestamp included in the output format
- Large memory to store the data accumulated in a time slice
- Zero suppression

Compatibility with DAQ (AMBER)

- Optic output
- Protocols: S-link, Aurora, UCF
- White Rabbit input (option)

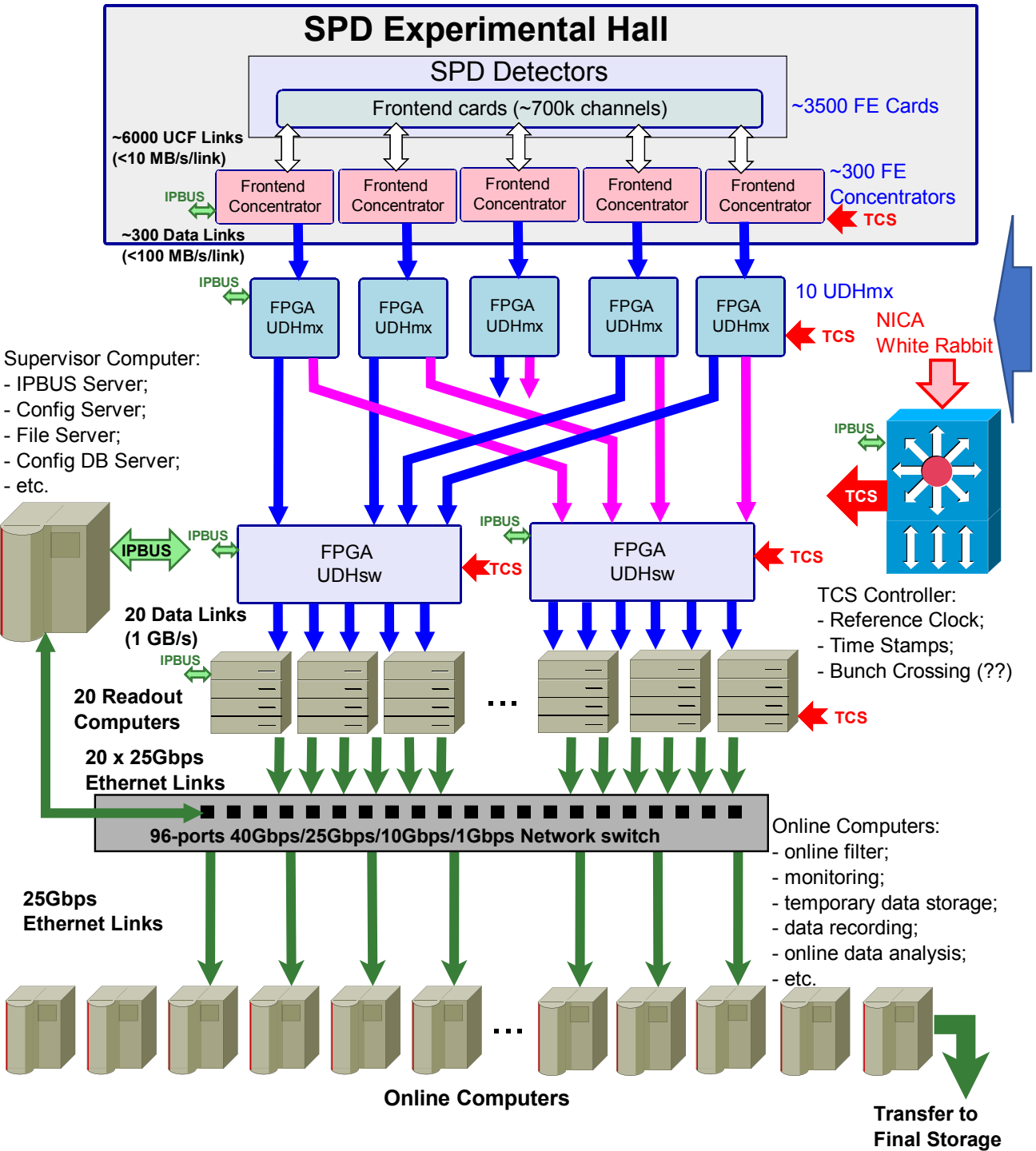


In DAQ of SPD we are planning to employ the ideas developed for the modernized DAQ of COMPASS/AMBER/NA64 by Igor Konorov group from the Technische Universität of München (TUM). His conception of SPD DAQ is accepted with minor modifications.



Slow control accesses FE cards via the FE Conccentrators using UDP-based IPBus protocol.

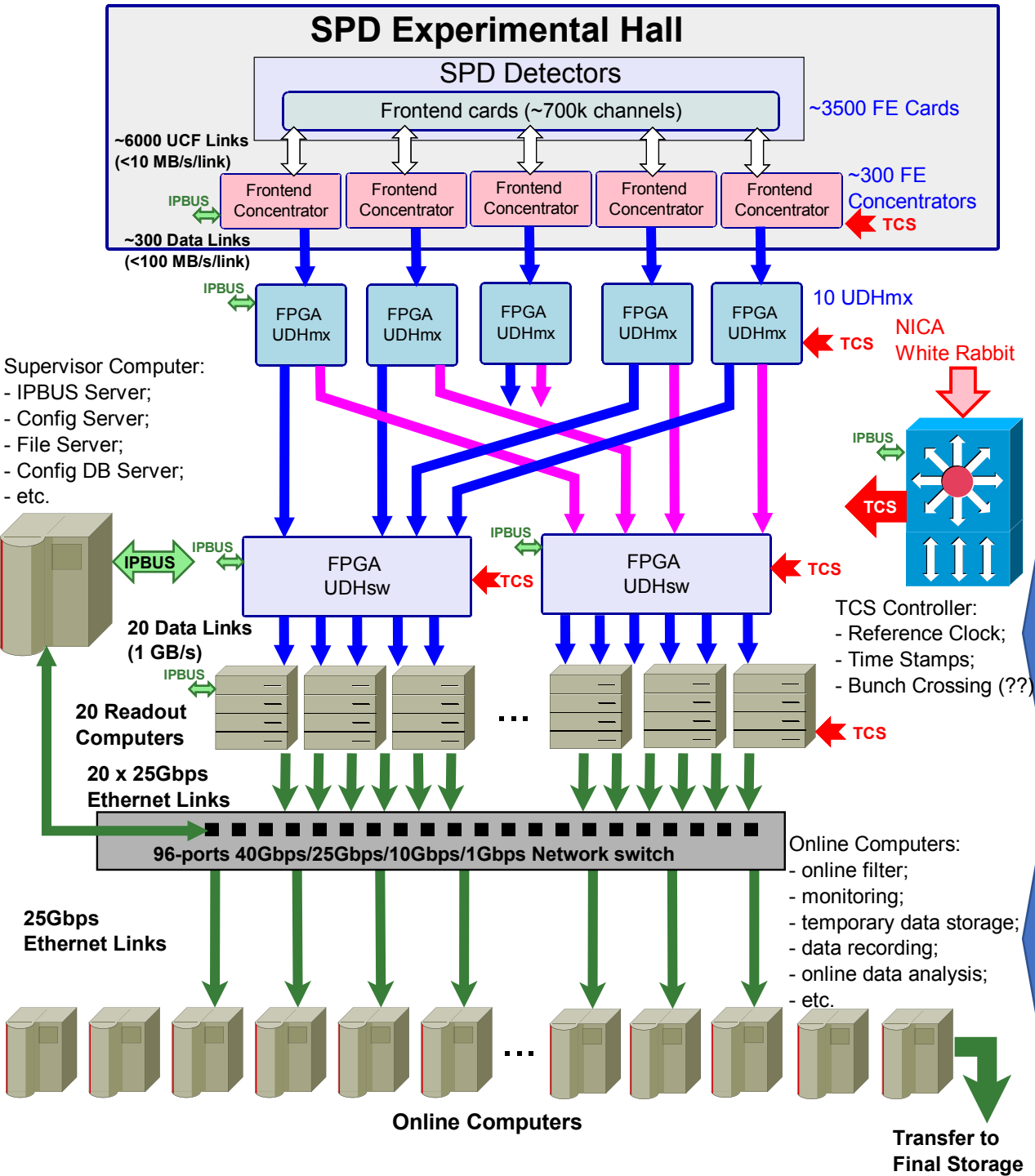
FE Conccentrators retransmit clock signals to FEE and convert detector information to a high speed serial interface running over an optical link.
UCF (*Unified Communication Framework*) protocol will be a standard high speed link protocol within the DAQ.



The multiplexer (UDHmx) modules receive detector information via serial links, verify consistency of data, and store them in DDR memories.

The multiplexer is equipped with 32 GBytes of memory.

All accepted data are assembled in sub-slice and distributed to two switches. Each multiplexer has a bandwidth of 2 GBytes/s.



The switches (UDHsw) perform the final level of slice building and distribute the assembled slices to 20 (?) on-line computers.

Finally, the continuous sequence of slices is built with Network Switch in each PCs

DAQ hardware

Near detector

Mechanics:

- 374 Front End Concentrators - VME 6U double width 12(15) inputs, 1 outputs
- 43 VME crates, 0.5kW → 9-10 racks

Cables:

- From detectors to DAQ: 4436 optic links
- From DAQ to the control room: 374 optic links (double), max 480 links

In barrack

3 VME crates (1kW)
20 DAQ computers (1kW) → 3-4 racks

DAQ hardware

DHmx/DHsw - Front End Concentrator

- Xilinx Virtex-6 VLX130T
- Custom board in AMC form factor
- 16x 6.25 Gb/s links
- 4GB DDR3 Memory
- VME carrier board

Firmware version need to be modified for SPD

Migration to ATCA (Igor Konorov 08-02-2021)

ATCA Carrier Card :

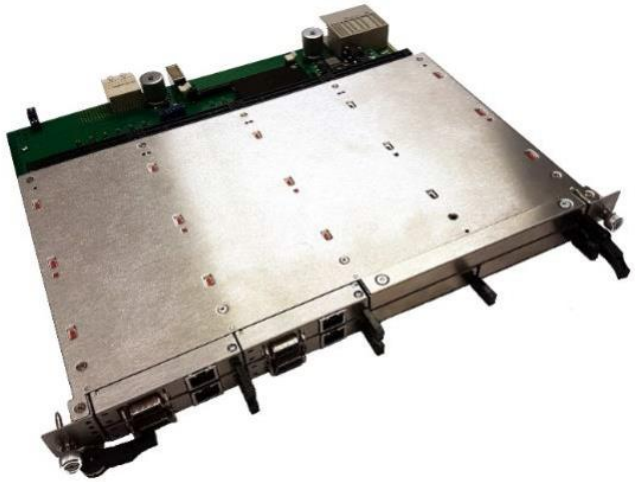
- 4 DHmx/DHsw modules
- 4 Optical interface AMC cards
- 16 links between A & B connectors

Rear interfaces

- 8 x Ethernet for IPBus
- USB for JTAG
- SFP+ for TCS interface + 1:8 fanout

Optical Interface AMC card

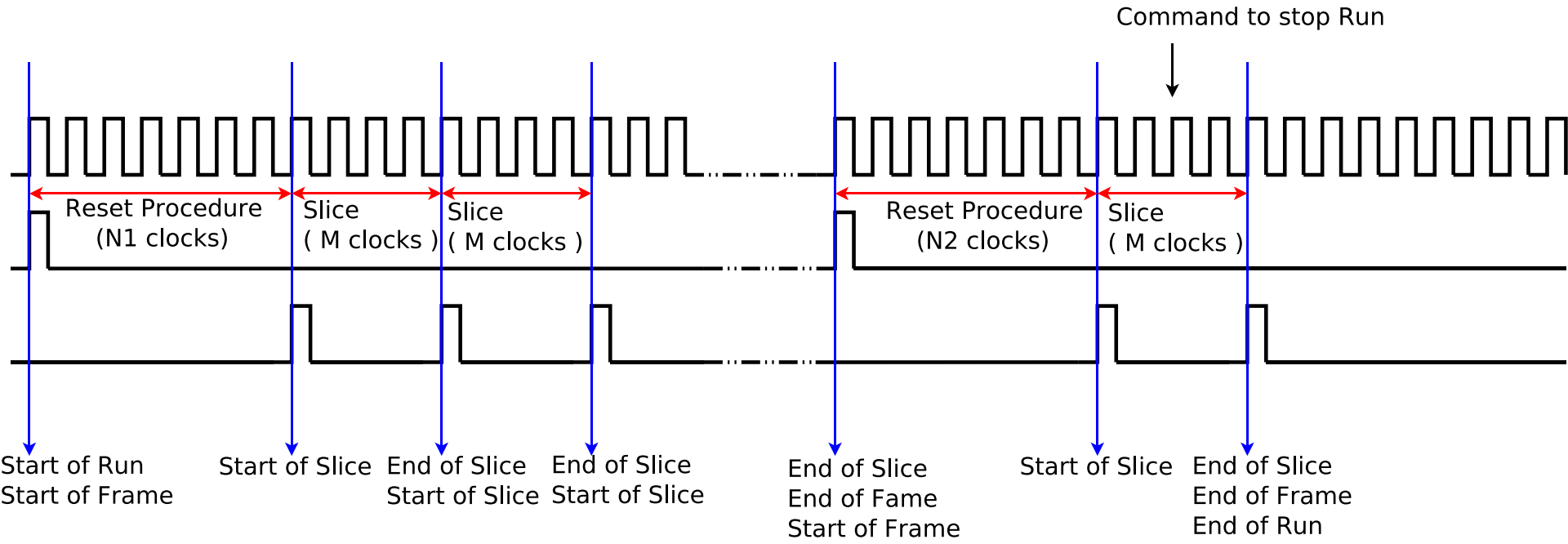
- 8 + 4 FireFly Transceivers



Computer input / PCI Express buffer

- Based on commercial hardware
  – Nereid Kintex 7 PCI Express
  – Trenz FMC – SFP adapter
  Kintex 7 XC7K160T FBG676
- 4x PCIe-Gen2 interface
- 4 GB DDR3 memory
- No dedicated TCS interface

Time diagrams



Tclock = 8ns (125 MHz) from White Rabbit;
Reset Procedure <= 300 ms (depends on electronics);

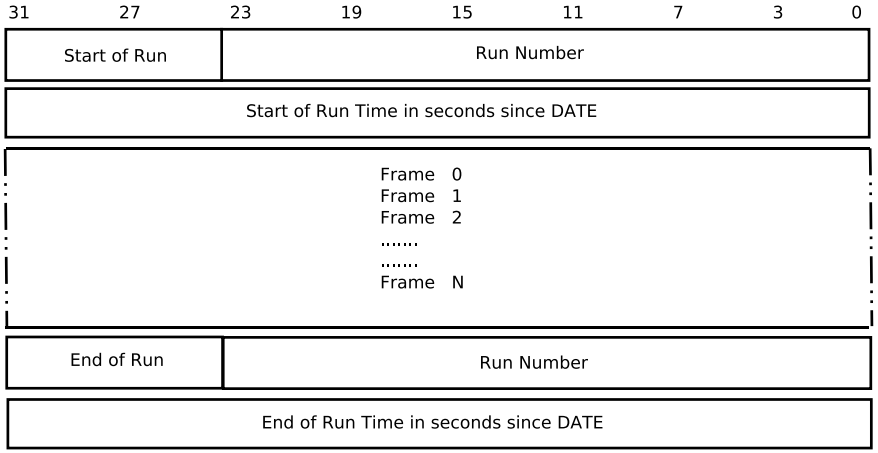
Slice Number: 24 bits (1 us - 8.3ms)
Data Size: max 16GB (real size < 160MB (20GB/s limit));

Frame: starts by Reset procedure, width 16 bits (min: 65ms, max: 549.7s),
Data Size: max 1PB (real size < 10TB (20GB/s limit))

Data Format

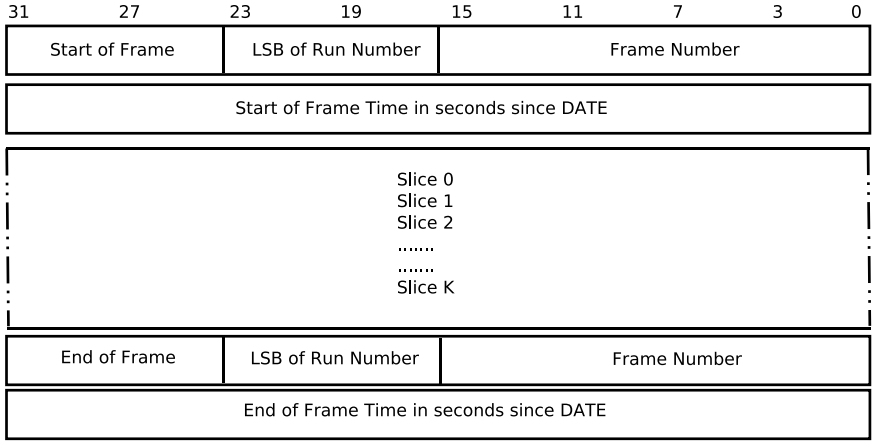
SPD Data Format

Run Structure:



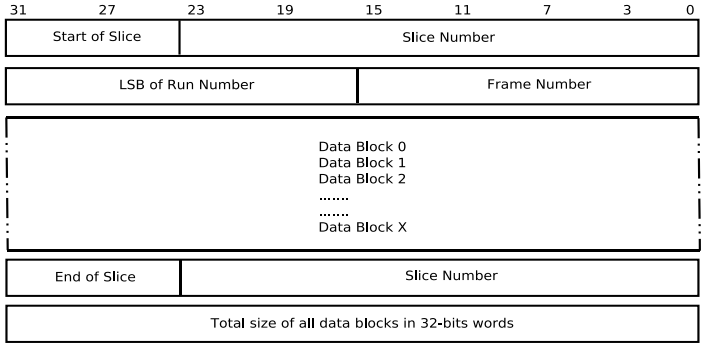
Number of Frames in the Run: 1-N, where N is maximal number of frames in the Run (assigned by TCS Controller)

Frame Structure:



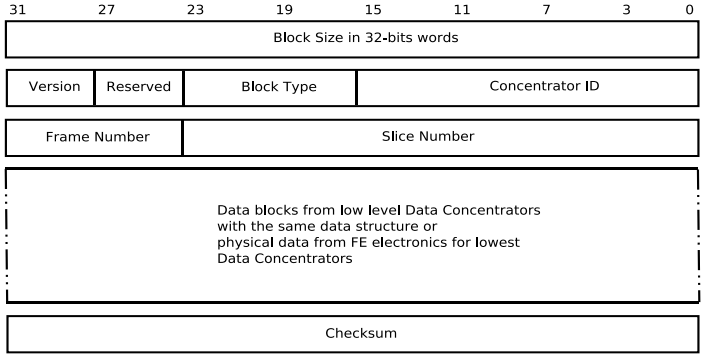
Number of Slices in the Frame: 1-K, where K is maximal number of slice in the Frame assigned by TCS Controller

Slice Structure:

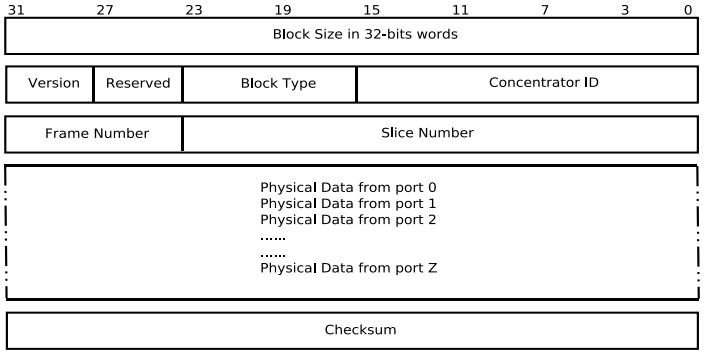


Number of Blocks in the Slice depends on DAQ configuration and data flux.

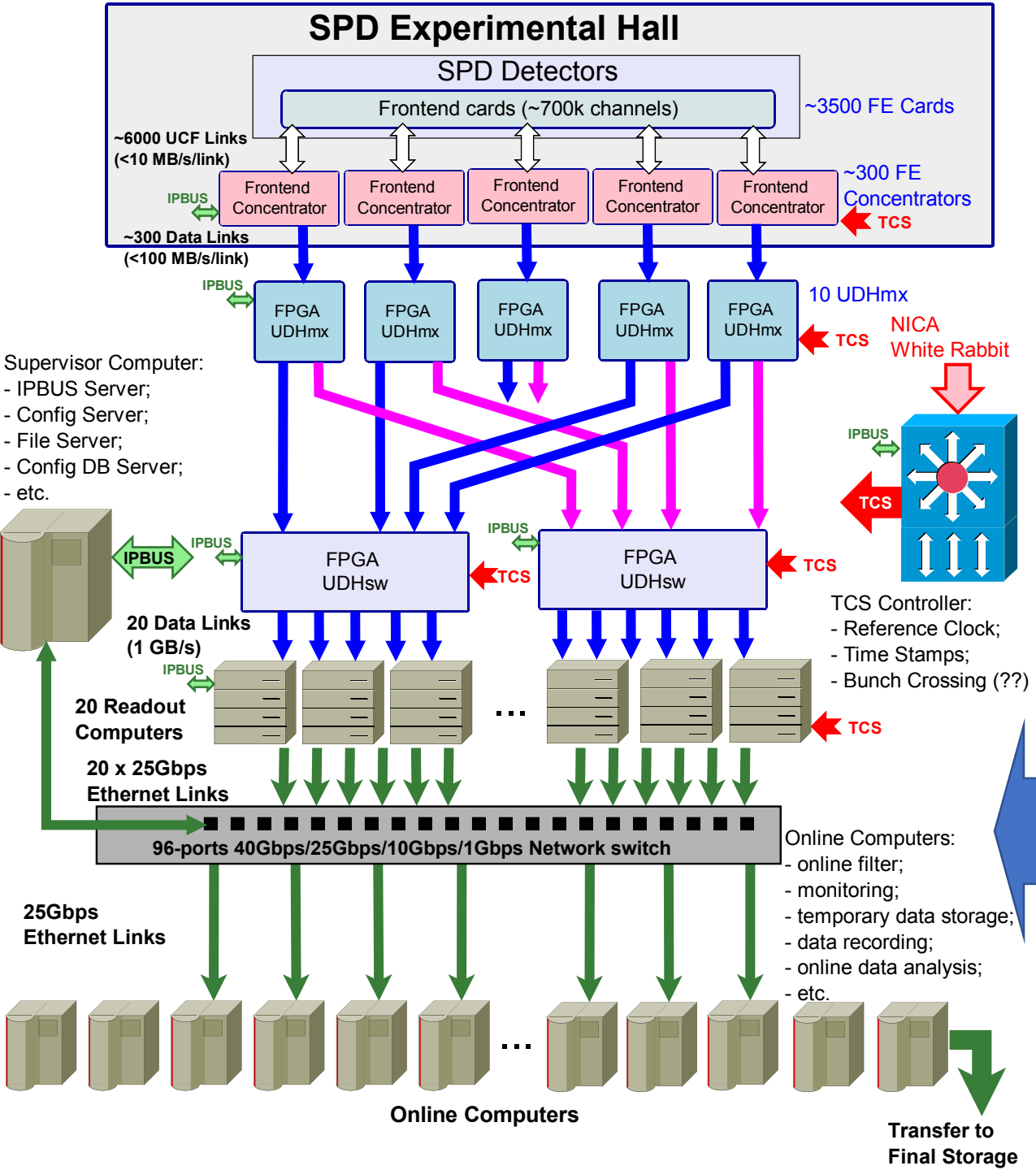
Data Block Structure of High Level Data Concentrators (Switches, Multiplexers etc.):



Data Block Structure of Lowest Level Data Concentrators (FE Concentrators):



Number of ports depends on FE Data Concentrator Type.
For instance, Igor Konorov ifTDC Multiplexer has 15 input ports.



A prototype software for data transfer through the network switch was written. May be we can skip the Highspeed Input Buffer before the Online Filter.

Status

- AMBER DAQ is scheduled to start to start 2-3 year before SPD. Its current status allows us to consider it as the good developed and tested prototype for SPD.
- Now in Dubna we have two Data Handling multiplexers (DHmx), one module of Trigger Control System (TCS) from COMPASS/AMBER DAQ and PCI buffer. That is enough for first testing of some modules.

Perspectives

- We hope for closer cooperation with Technische Universität of München (TUM) as we rely on using their hardware modules.
- Another option is to involve an external group which is capable to develop the needed hardware or support the TUM modules.
- We have started negotiations with a group from St.Petersburg Polytechnic University (SPbPU) as the candidate for such group.
- We need a strong reinforcement of electronics support in SPD, both for detector front-end and for DAQ.

New participants are welcome!

Thank you for attention