# Triggered readout:
# tests on the laser test-bench at JINR

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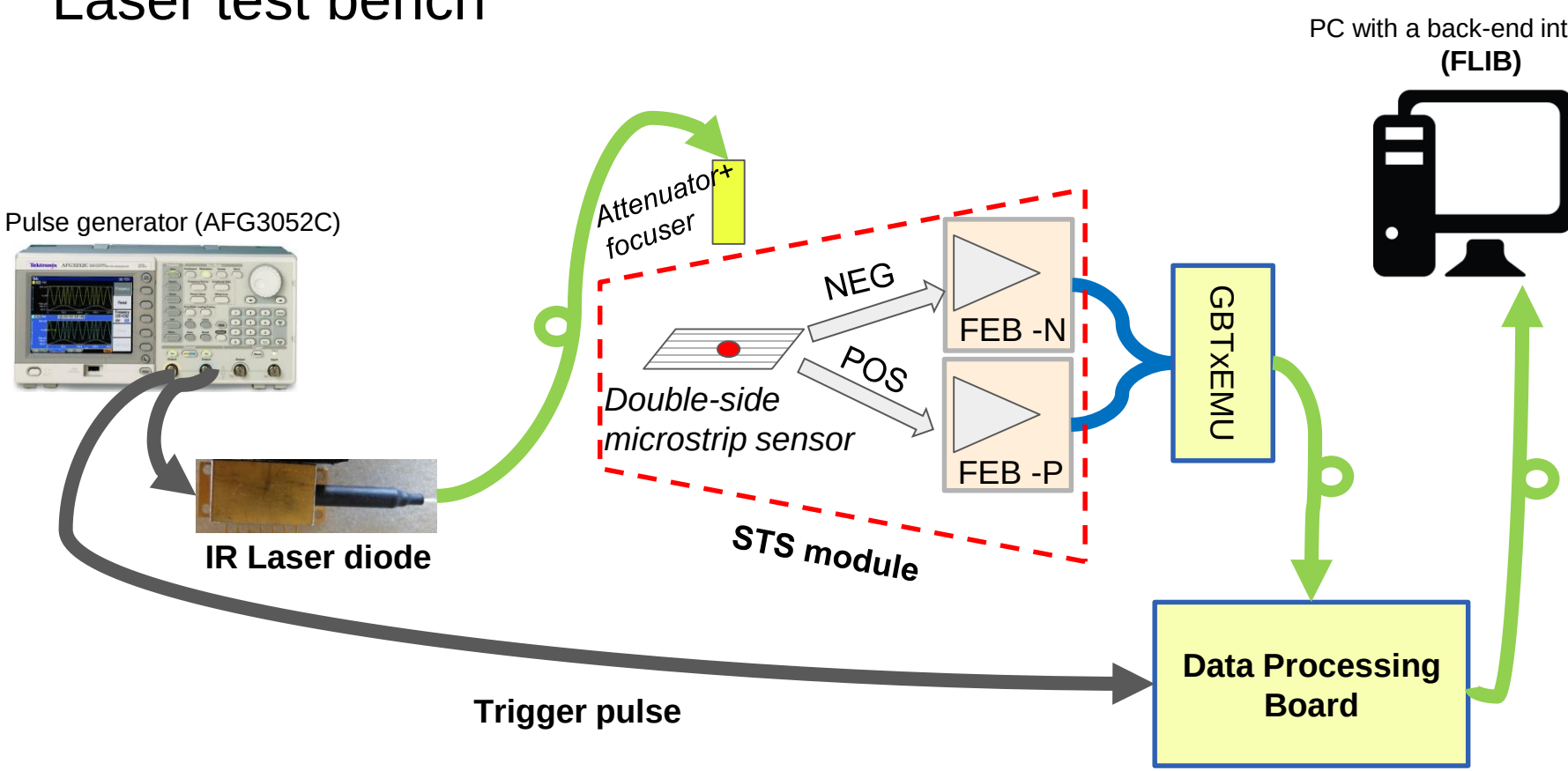
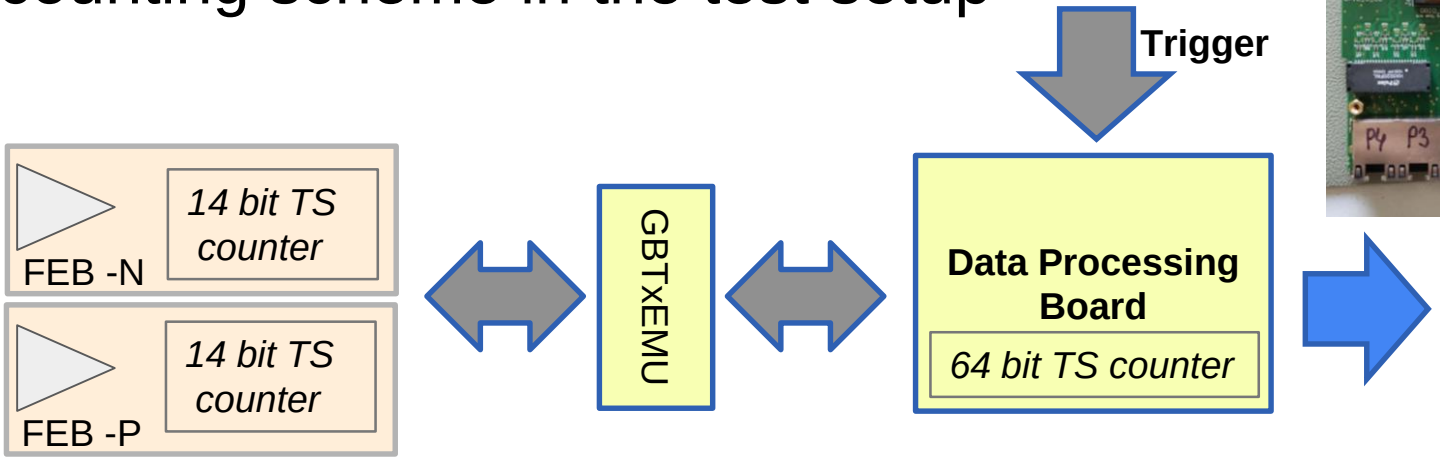
# Laser test bench



# TS counting scheme in the test setup

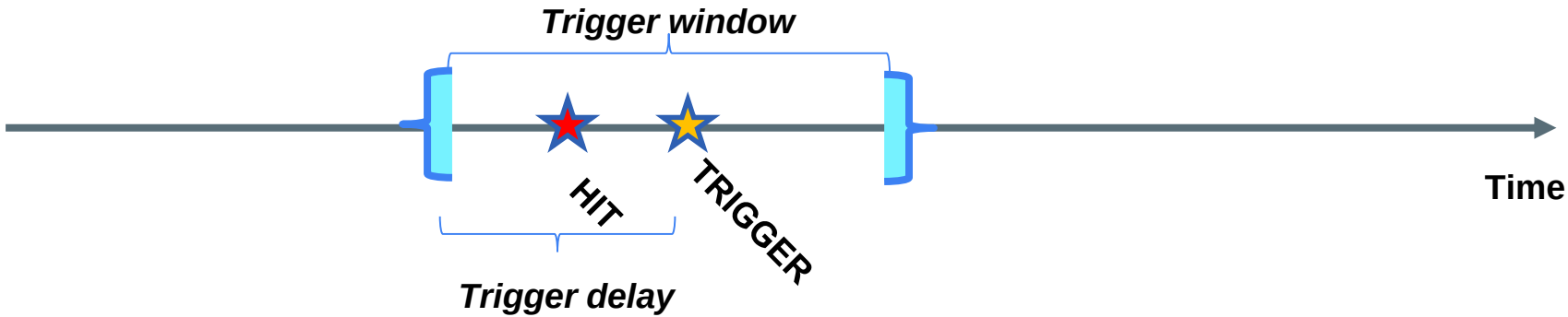




1. TS of the HIT is assigned by the TS counter of SMX;
2. TS of the trigger is assigned by the TS counter of DPB;
3. IF the *hit_ts* is in the *trigger window* event is generated.

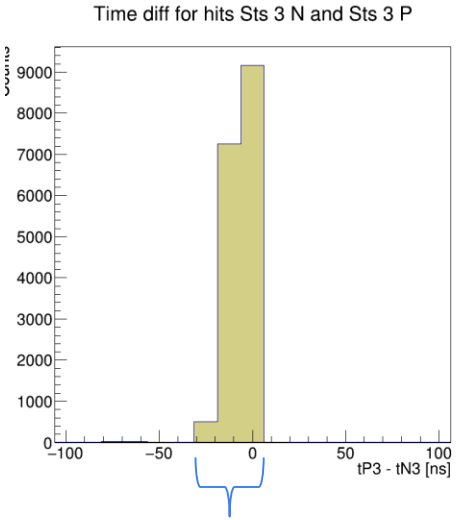
**All TS counters should count synchronously with a constant delays**

# Trigger parameters



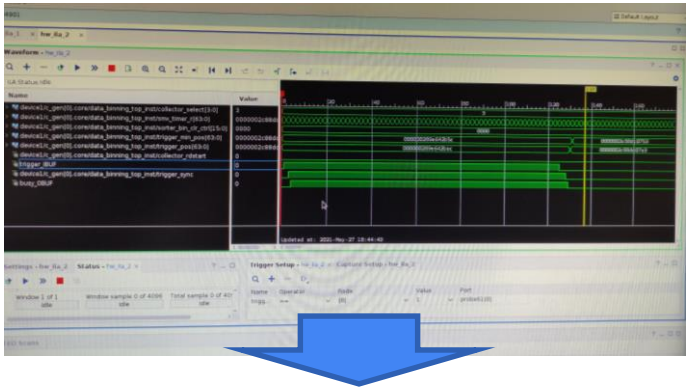

1. *Trigger window & trigger delay* are configurable parameters;
2. *From the discussion with BM@N DAQ group:*
   - *Trigger latency <= 7 us;*
   - *Trigger window <= 7 us;*
   - *Min time between triggers: 20 us.*

# Synchronization




**30 ns**

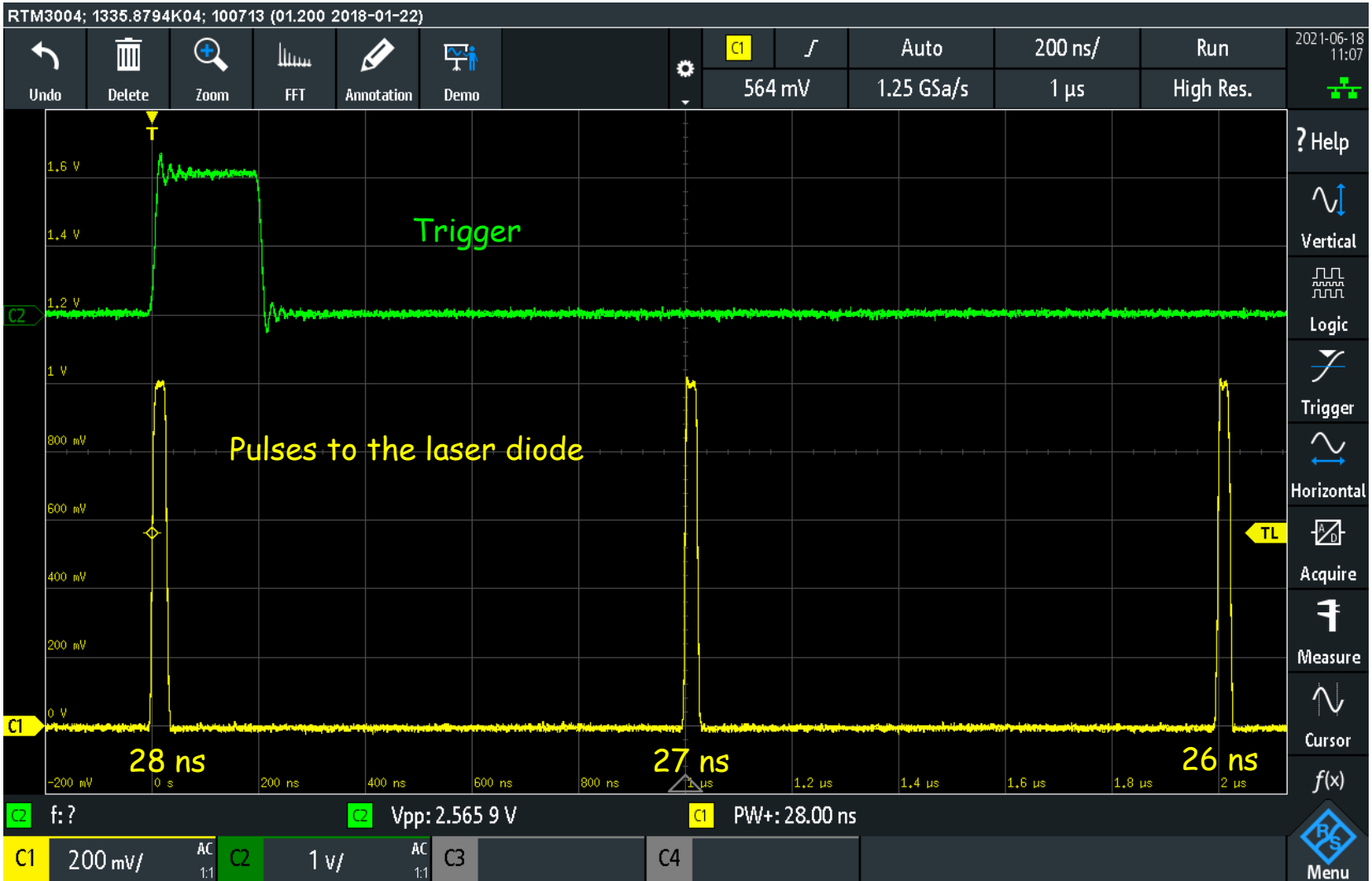
Time difference between Hits on the P and N sides of the sensor produced by the same laser pulse

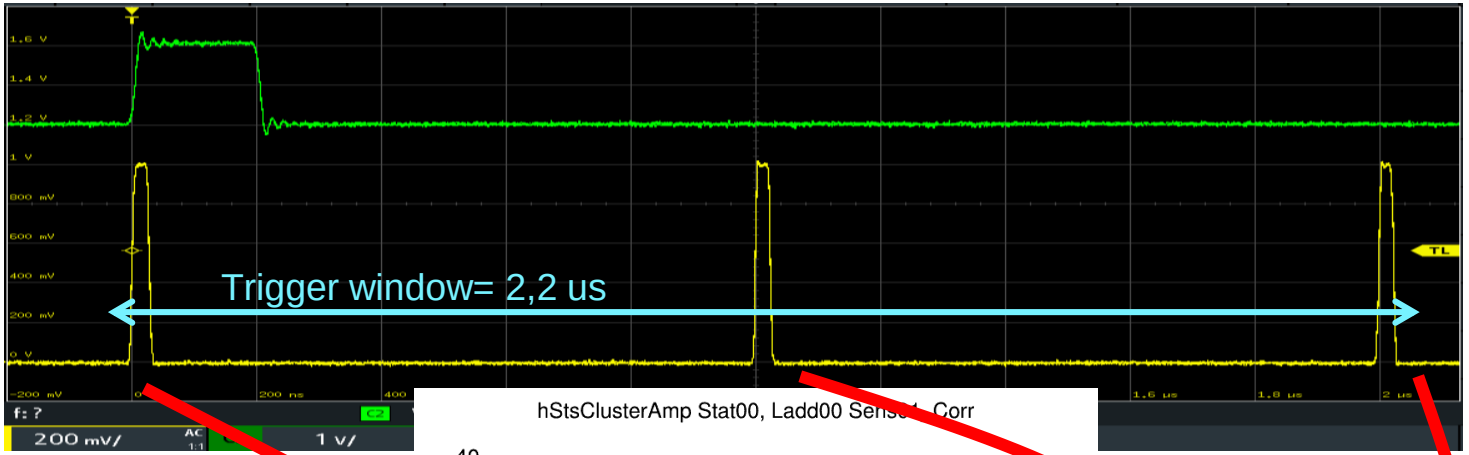


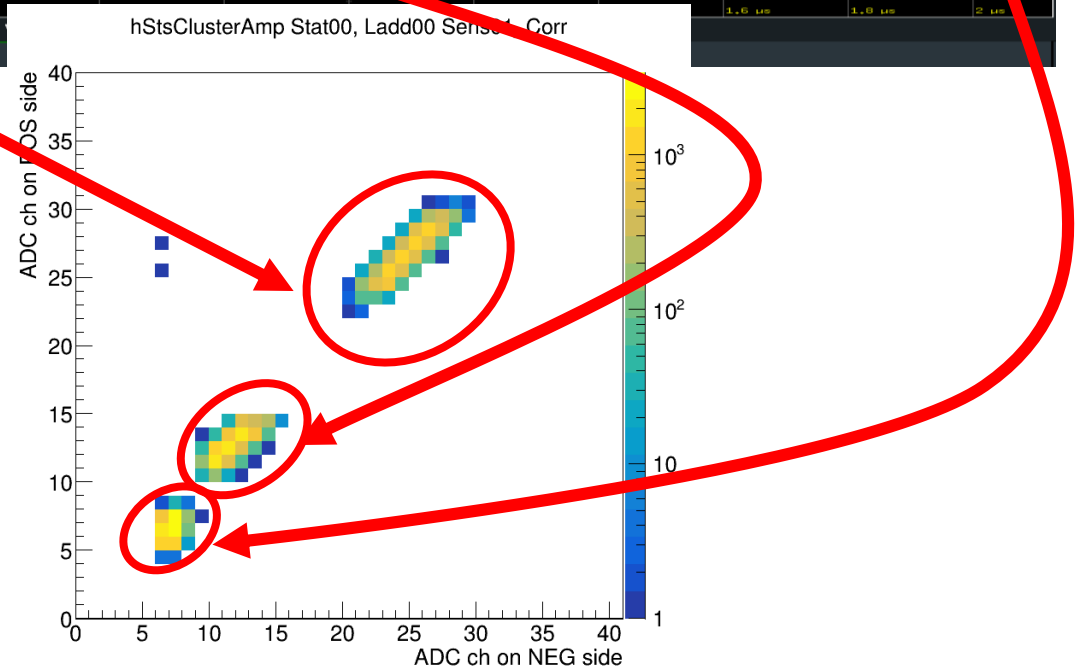
dif_to_trigger = 100 ns; 8 cnt
dif_to_trigger = 87 ns; 7 cnt
dif_to_trigger = 100 ns; 8 cnt

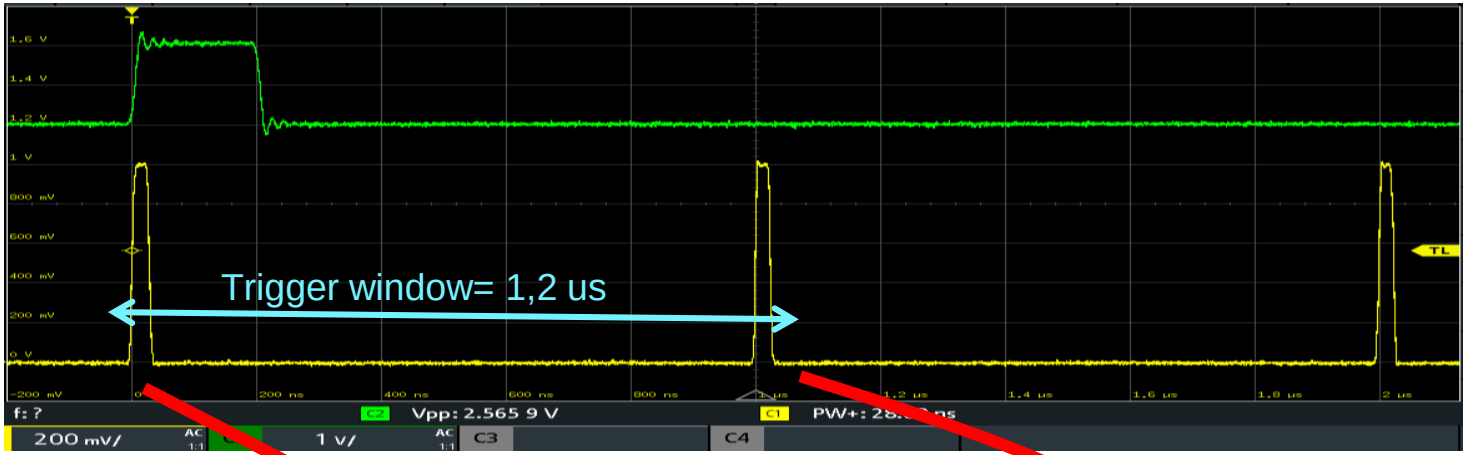
Time difference between Hit and trigger was checked with Chipscope on FPGA. **The latency is stable and does not depend on the resynch & rebooting of the FPGA!**

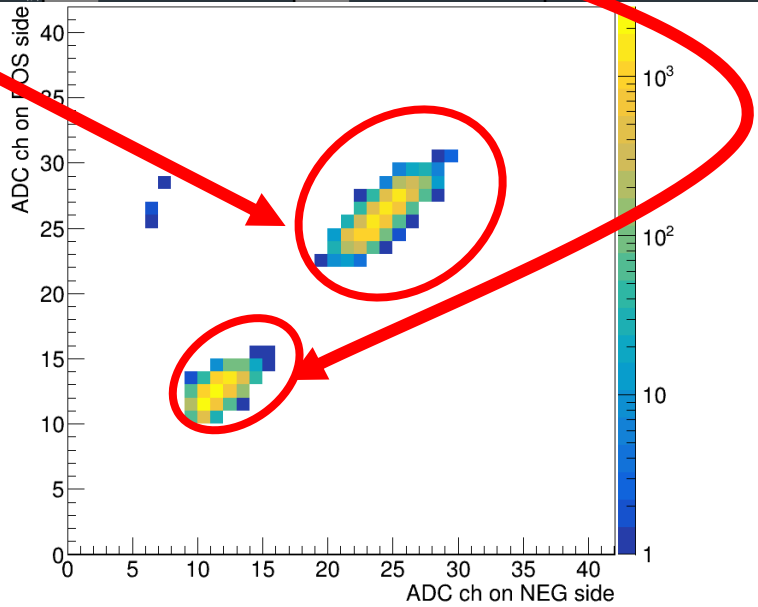
- Synchronization between SMXs is +-1 TS (25 ns);
- Synchronization between SMXs and DPB is +-1 TS (25 ns);
- The latency is stable and does not depend on the resynch & rebooting of the FPGA!

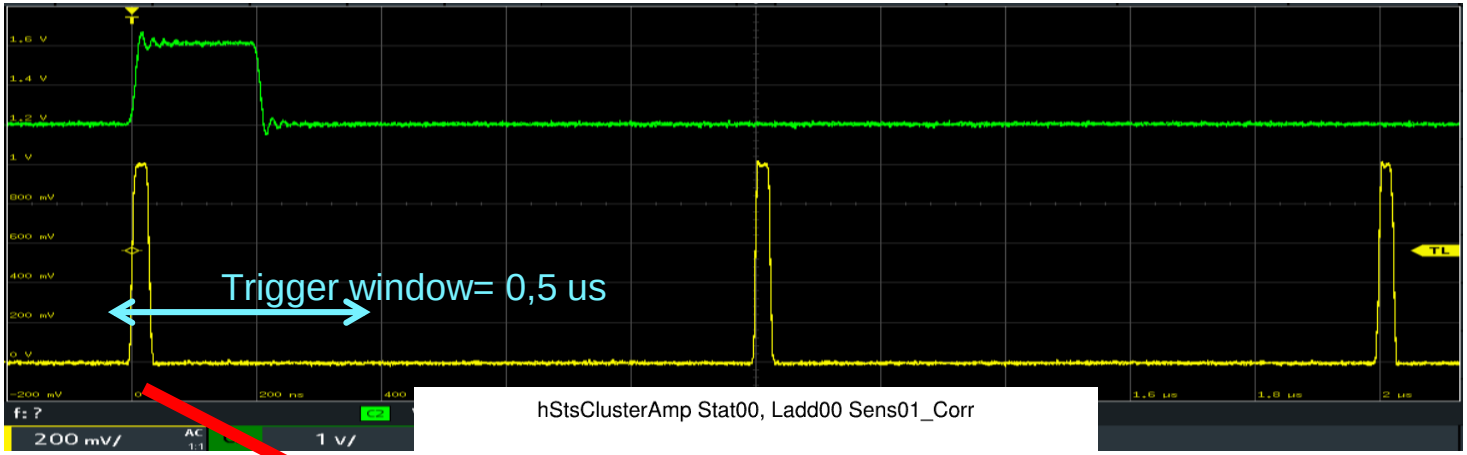

RTM3004; 1335.8794K04; 100713 (01.200 2018-01-22)
Undo
Delete
Zoom
FFT
Annotation
Demo
C1
Auto
200 ns/
Run
564 mV
1.25 GSa/s
1 µs
High Res.
2021-06-18
11:07
Help
Vertical
Logic
Trigger
Horizontal
Acquire
Measure
Cursor
f(x)
Menu
Trigger
Pulses to the laser diode
28 ns
27 ns
26 ns
C2
f: ?
Vpp: 2.565 9 V
PW+: 28.00 ns
C1 200 mV/ AC 1:1
C2 1 V/ AC 1:1
C3
C4

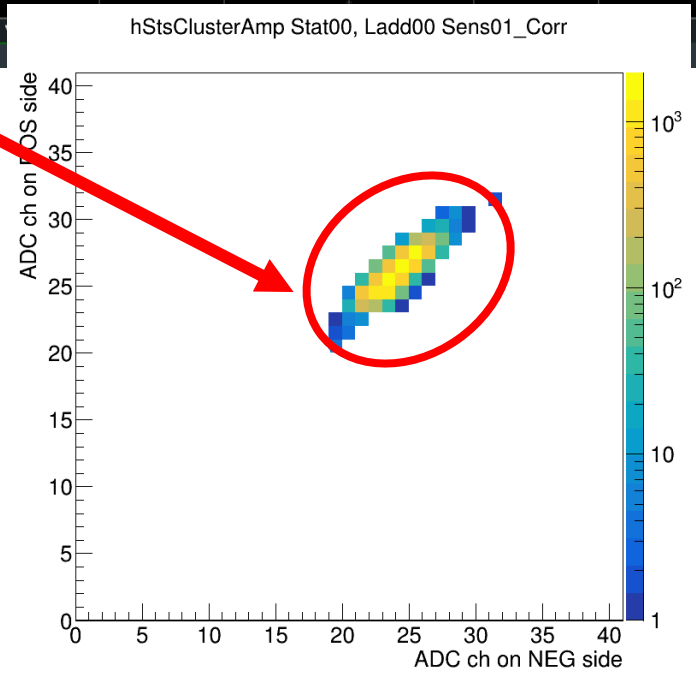

Trigger window= 2,2 us
200 mV/
1 V/


hStsClusterAmp Stat00, Ladd00 Sens
ADC ch on POS side
ADC ch on NEG side
0
5
10
15
20
25
30
35
40
1
10
$10^2$
$10^3$


Trigger window= 1,2 us
f: ?
Vpp: 2.565 9 V
200 mV/
1 V/
C3
C4


ADC ch on POS side
ADC ch on NEG side
0
5
10
15
20
25
30
35
40
$10^3$
$10^2$
10
1


Trigger window= 0,5 us


hStsClusterAmp Stat00, Ladd00 Sens01_Corr
ADC ch on POS side
ADC ch on NEG side

# Conclusion

- Proposed concept of the triggere implementation was proven on the test bench *(special thanks goes to Wojtek and Marek )*
- Further investigations as well as modification of the test bench are needed (measurements of the eff., trigger counting, busy signal )
- Migration to other platforms (GERI and TFC) will be done