Development of a multichannel SiPM power supply for TAO and DUNE experiments

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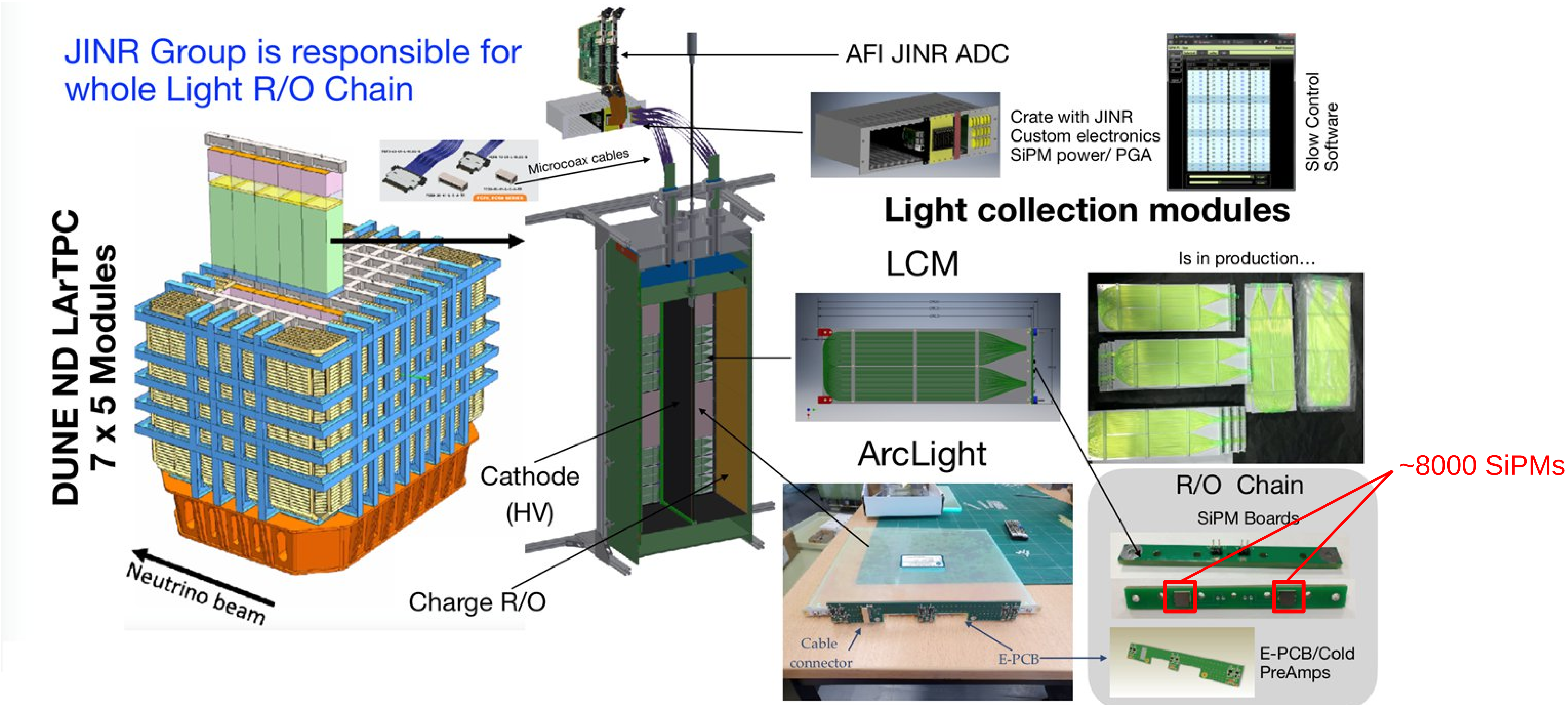
Supported by

Russian Science Foundation

Under grant #21-42-00023

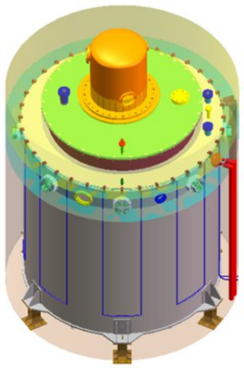
Almaty, 2021

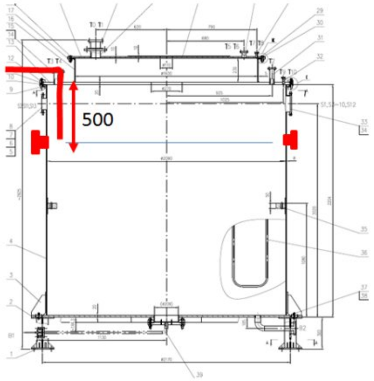
Light R/O for LArTPC of the DUNE ND

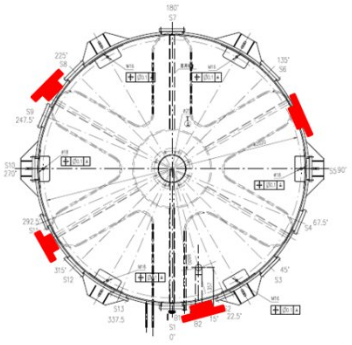


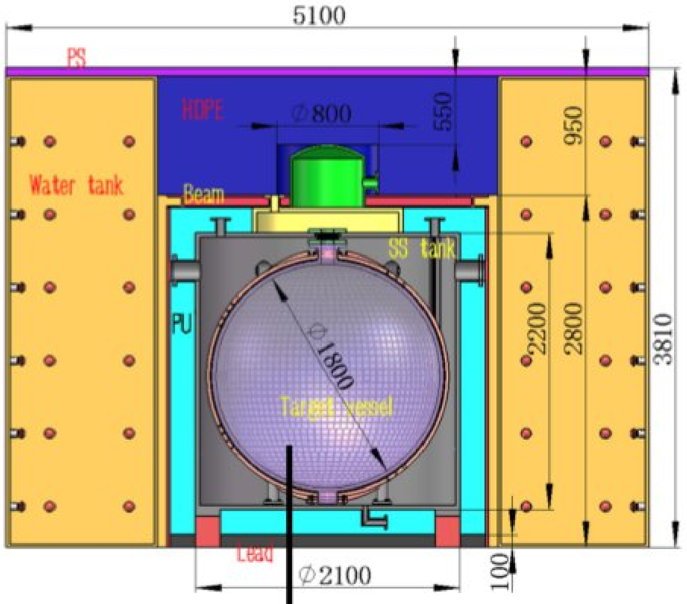
JUNO-TAO experiment

TAO detector

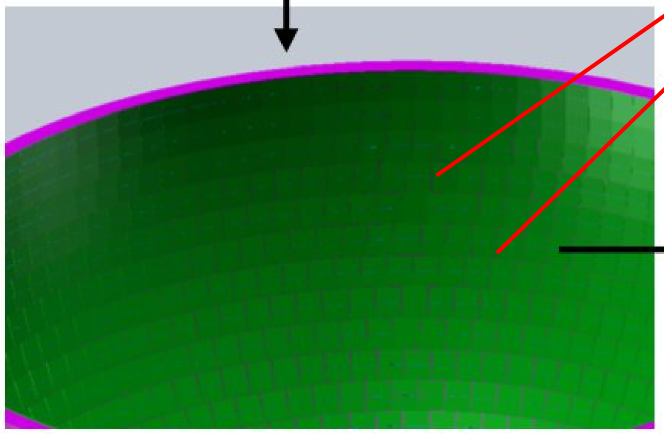




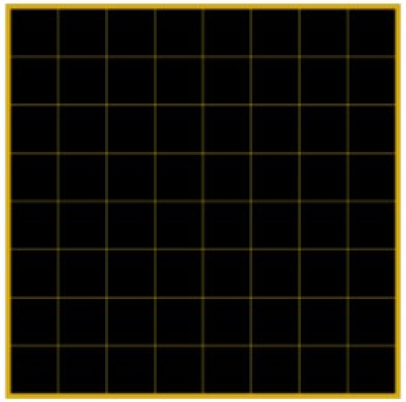




~250000 SiPMs
~4000 arrays



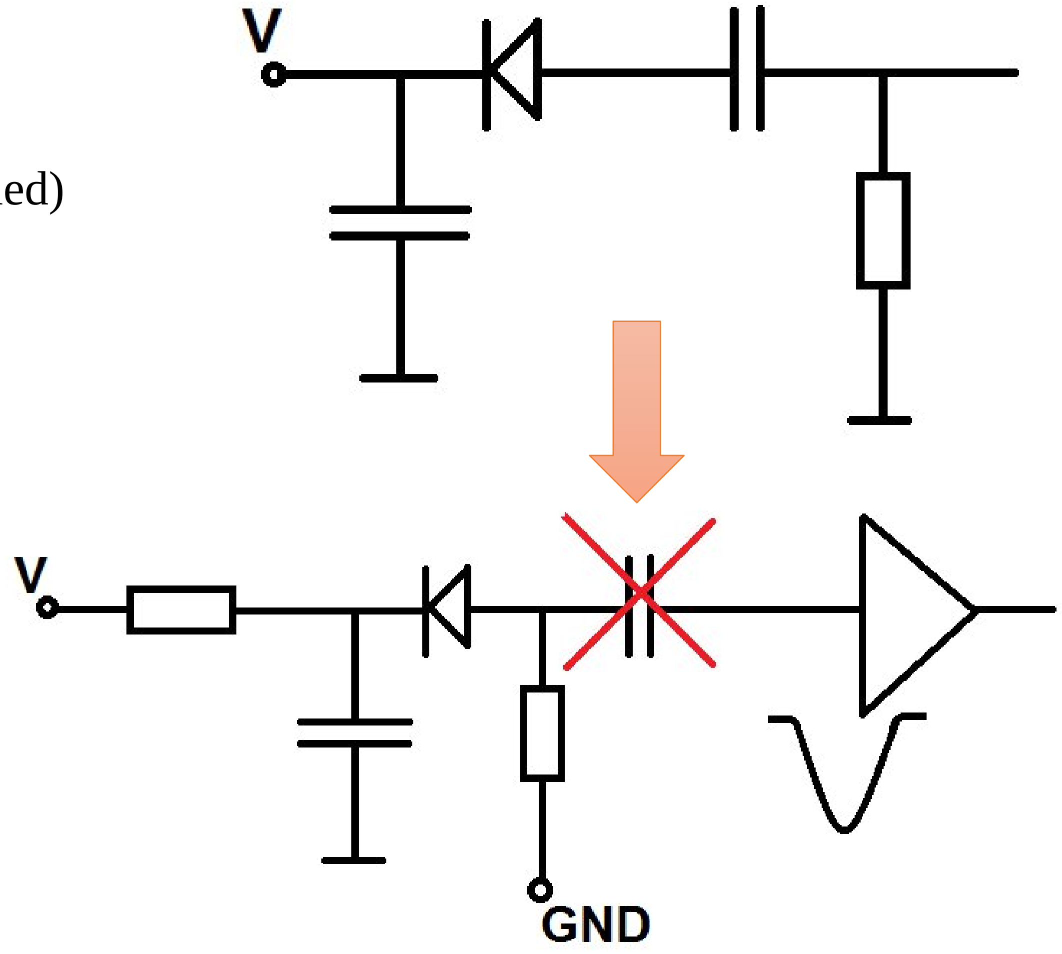
Sectional view of the central sphere with matrices



SiPMs matrix 8x8

Power unit requirements

1. Multichannel power supply
2. Unipolar power supply (off a channel in case of s.c; DC coupled)
3. VME 6U form factor
4. High channel density (>64 channels)
5. Setting the voltage with an accuracy of 10mV
6. Voltage stability better than 10mV
7. Reliable connection protocol : CAN
8. Configurable voltage range: 50V, 100V, 120V
9. Scaling up to thousands channels
10. Currents ~100 μA for power supply of a SiPM’s arrays



Power unit prototyping

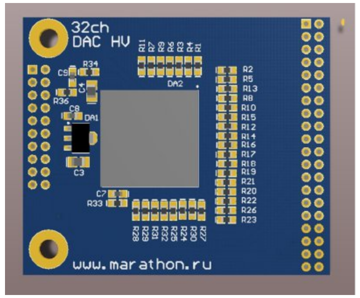
ADC AD5535B chip

FEATURES:

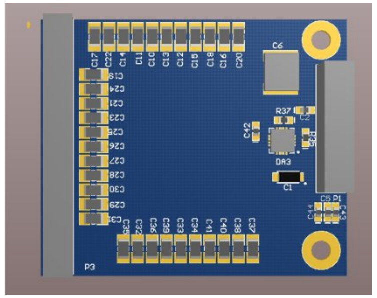
- High integration 32-channel, 14-bit denseDAC® with integrated high voltage output amplifier
- Guaranteed monotonic Housed in 15 mm × 15 mm CSP_BGA package
- Full-scale output voltage programmable from 50 V to 200 V via reference input
- 550 μA drive capability
- Integrated silicon diode for temperature monitoring
- DSP-/microcontroller-compatible serial interface
- 1.2 MHz channel update rate
- Asynchronous RESET facility
- –10°C to +85°C temperature range

Board design

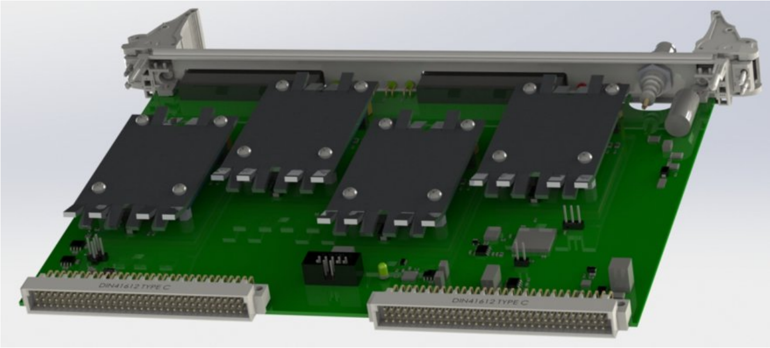
top



bottom

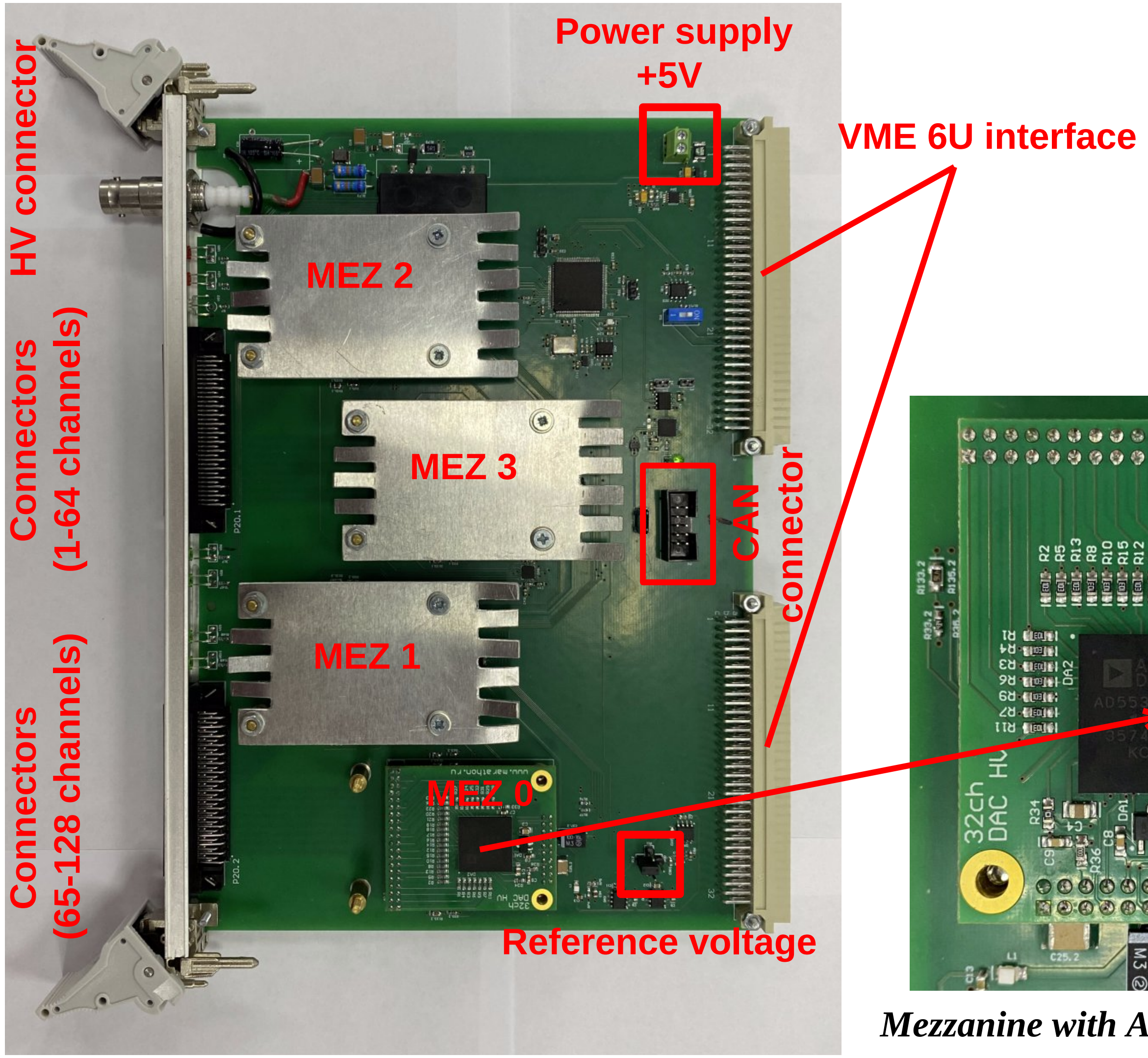


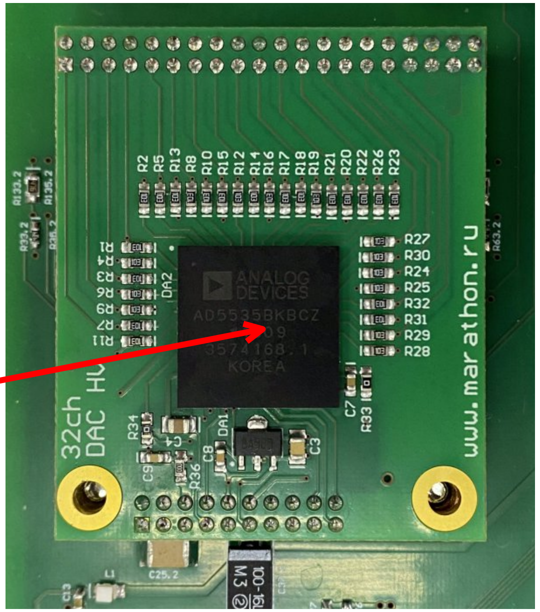
DAC 32 channels



Design by Marathon Company (MSU)

Pilot power unit



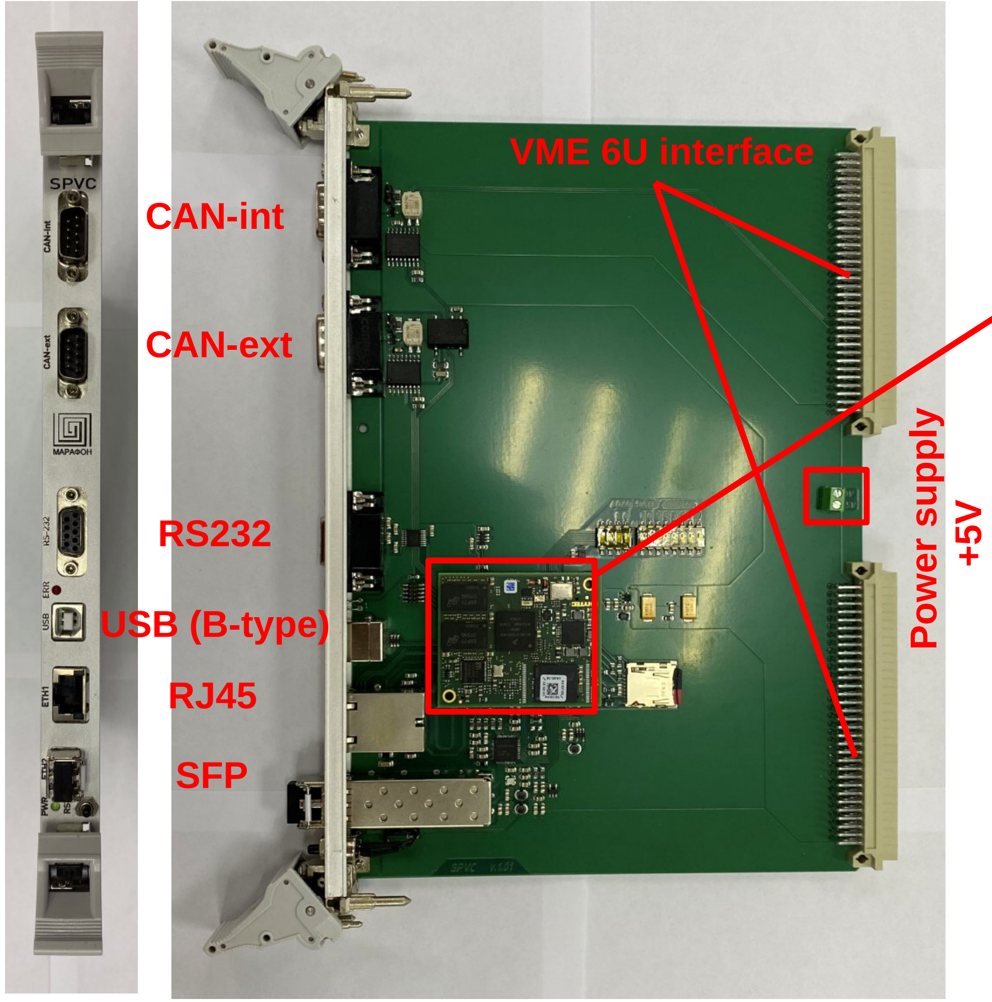


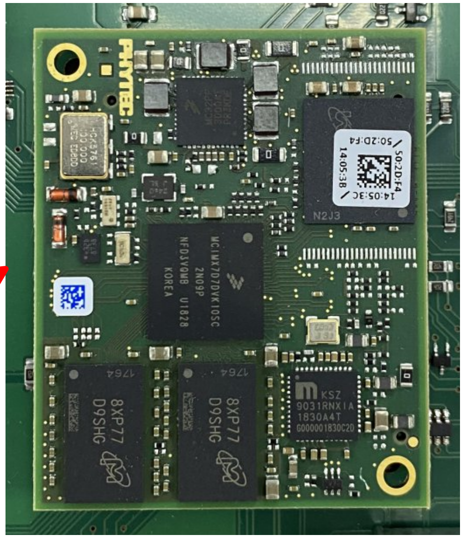
Mezzanine with AD5535B DAC chip

Main Features:

- VME mechanics
- 128 channels
- Based on AD5535B chip
- Voltage up to 200 V, 14-bit
- Max current 500 μA/ch
- 1xSHV connector
- 2x68pin IDC connectors
- PCB power supply ±12V, +5V by VME
- CAN-open protocol
- CAN interface on VME bus

Pilot control unit



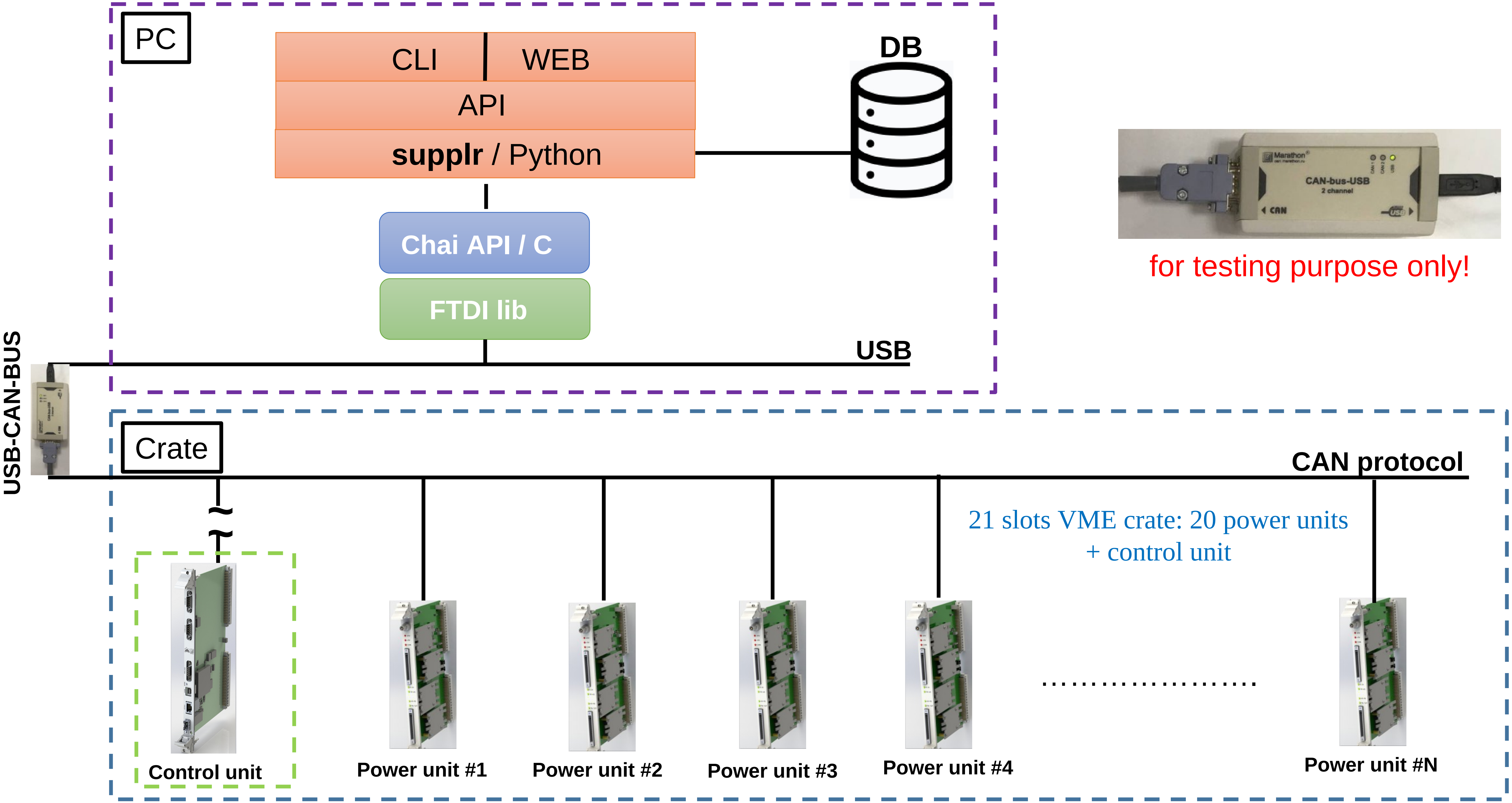


Micro PC: phyCORE-i.MX7

Main Features:

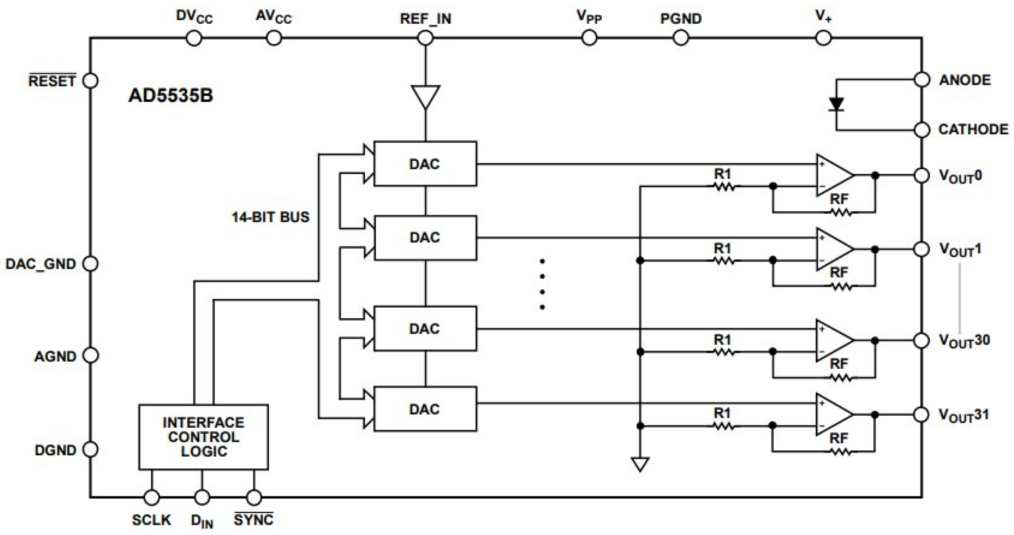
- VME mechanics
- Micro PC: phyCORE-i.MX7
- CAN-int, CAN-ext
- 2x connecion interfaces; 1GBPS (SFP) and 100MBPs (RJ45)
- COM port (RS232) and USB (B-type) for direct access to the micro PC
- PCB power supply ±12V, +5V by VME
- CAN-open protocol
- CAN interface on VME bus

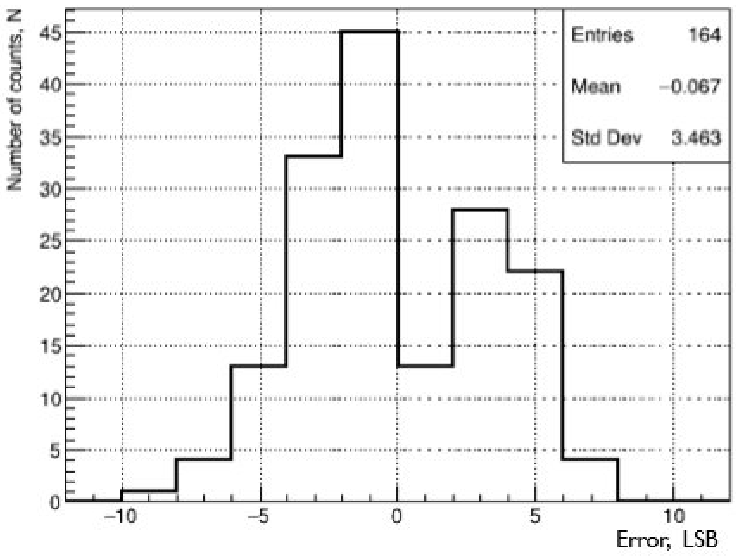
Unit management and software



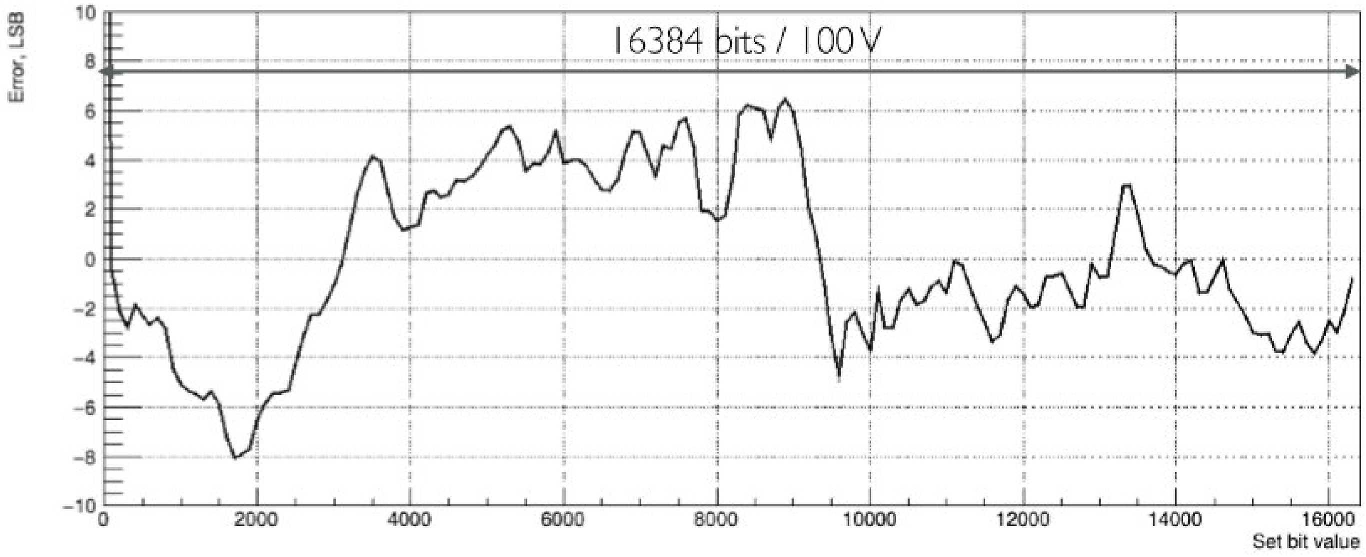
Integral nonlinearity

Functional block diagram of DAC





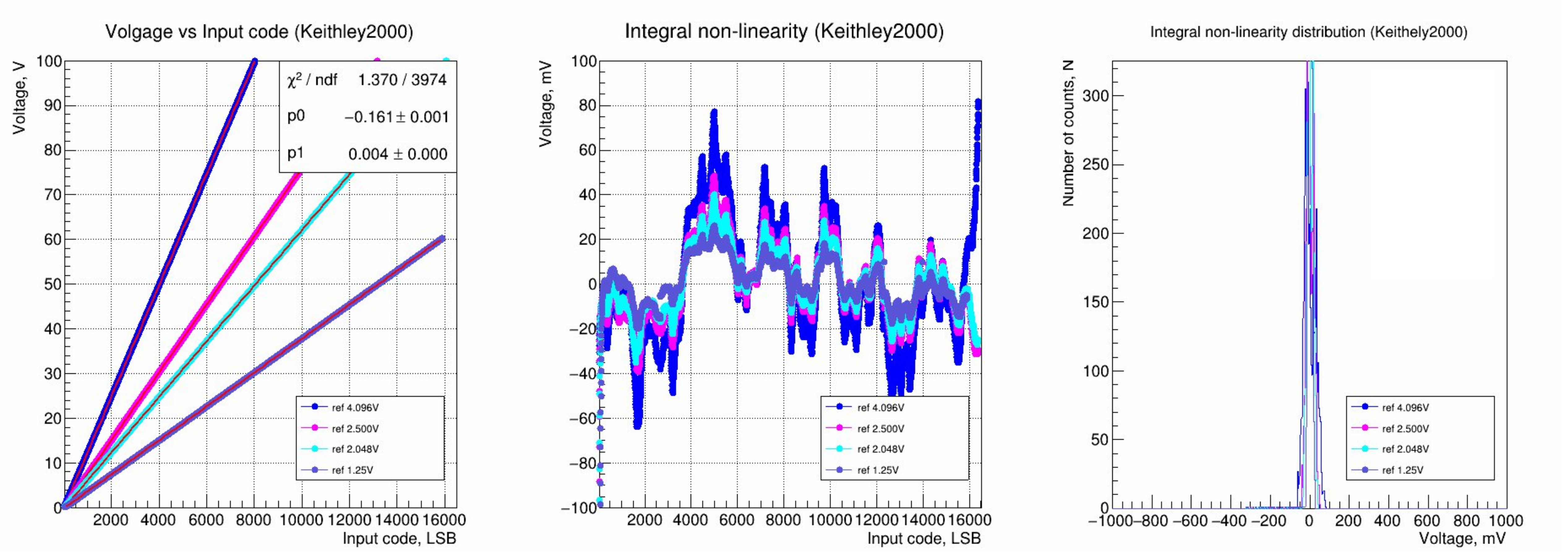
Integral nonlinearity example for single DAC channel



All points are within ±10 LSB (±60mV in range up to 100V)

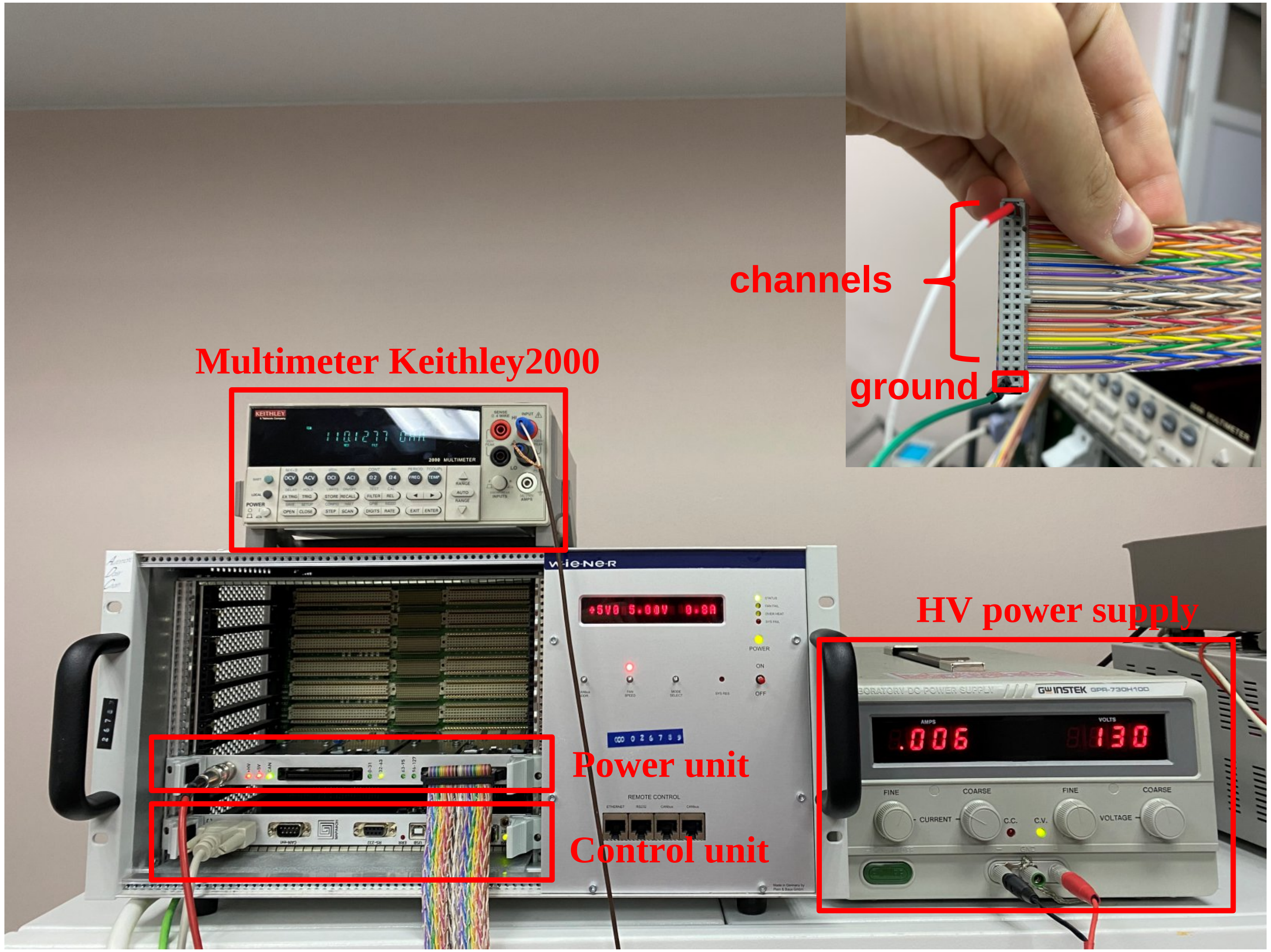
Can be corrected by calibration!

Integral nonlinearity example for single DAC channel at different reference voltages



V_{ref}, V	Output range, V
1.25	0-50
2.048	0-100
2.5	0-150
4.096	0-200

Calibration procedure



The calibration procedure of a single HV channel:

1. Voltage scan over all range (0 - 2^{14} bit) with an optimal step by precised multimeter.
2. Reconstruction of intermediate points.
3. Storing of all the date to a file (or database)

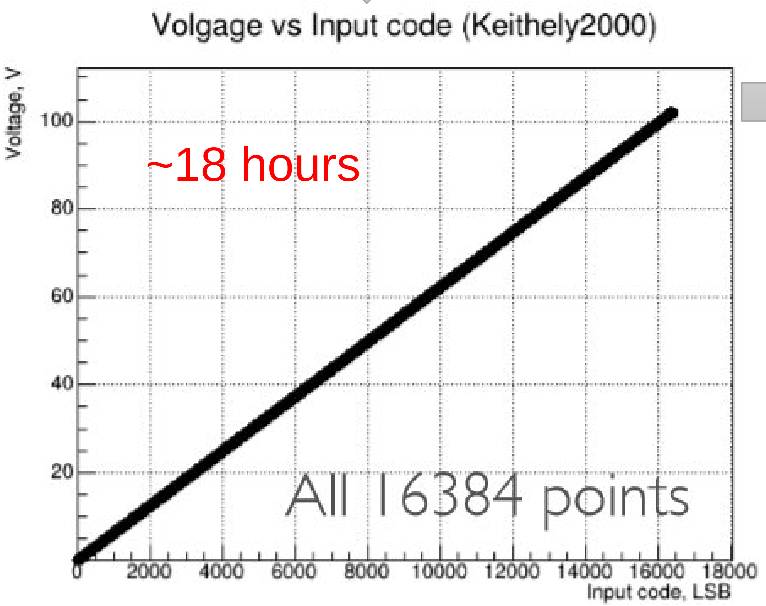
Studying of optimal settings for the calibration:

1. Determination of optimal scan step (32/64/128/…)
2. Testing of algorithm for reconstruction of intermediate points

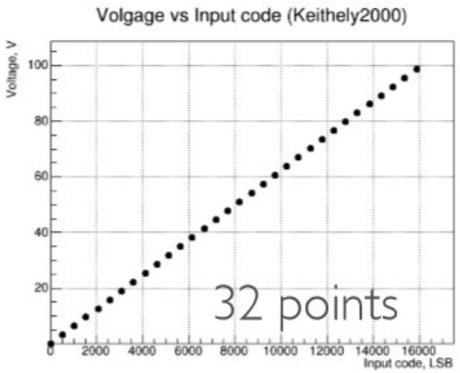
Studying of optimal settings for the calibration

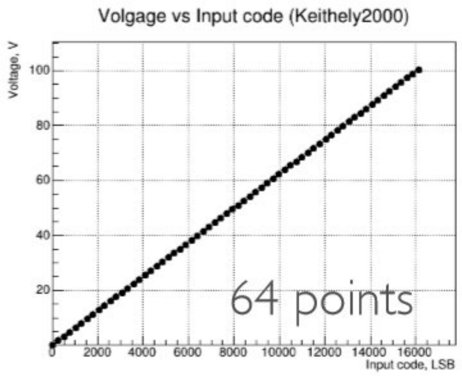
Calibration file

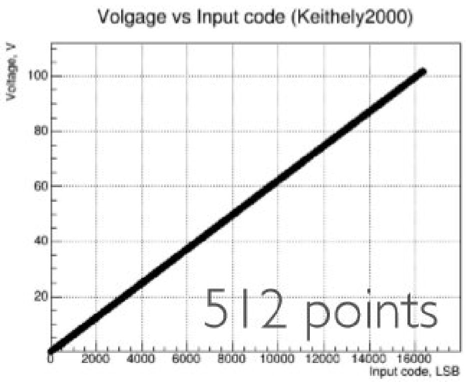
#DAC,bit	ADC,V	K2000,V	Tchip,C
0	0.122	0.198	24.669
1	0.123	0.2	24.618
2	0.125	0.201	24.636
...			
[illegible]	[illegible]	[illegible]	[illegible]
16381	99.544	101.987	25.754
16382	99.55	101.993	25.751
16383	99.555	101.999	25.739

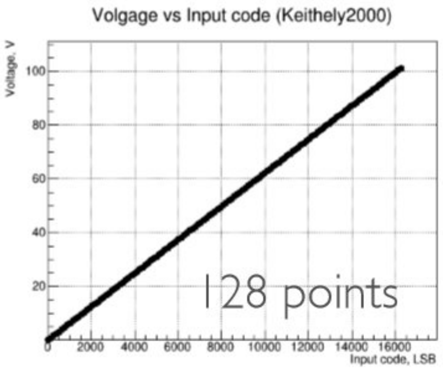


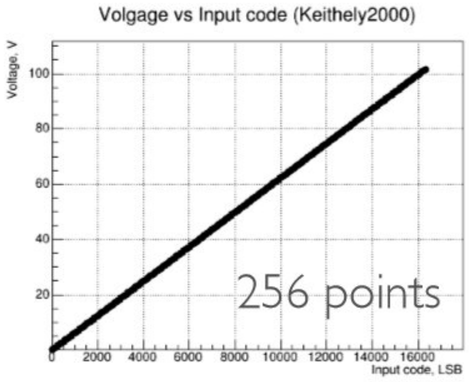
Sampled number of points



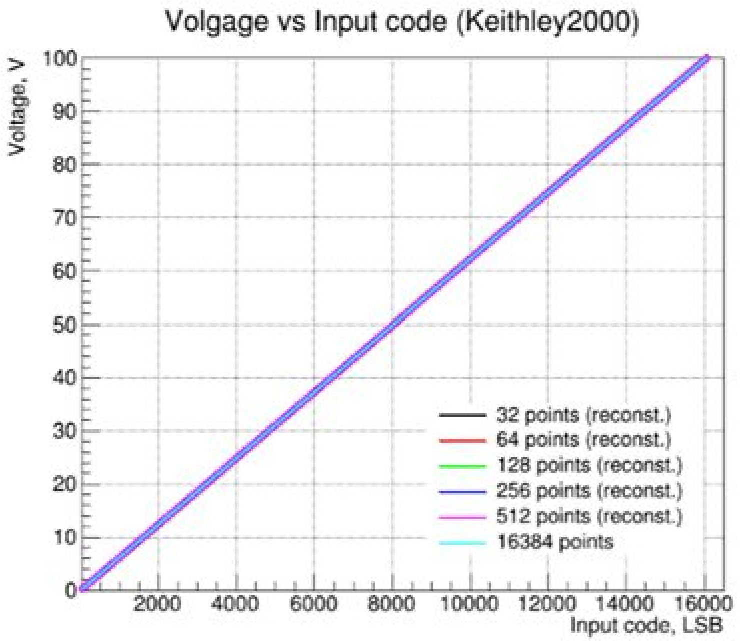


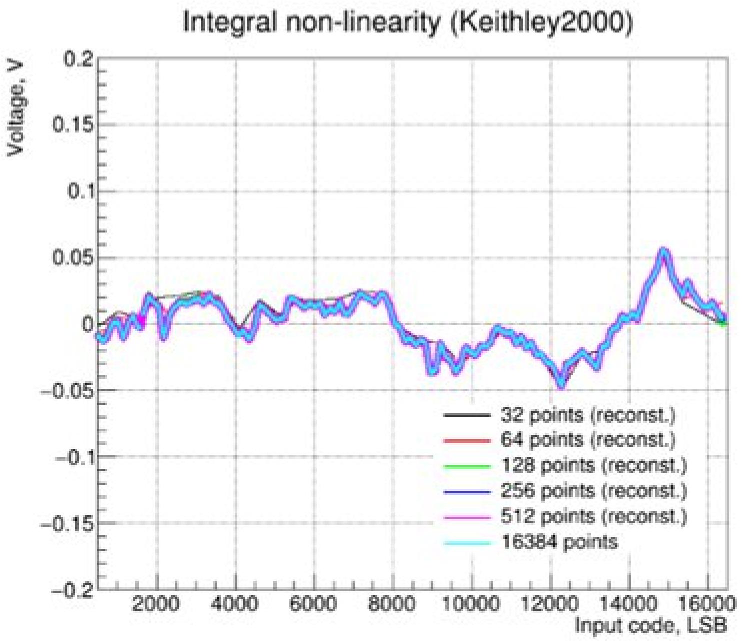


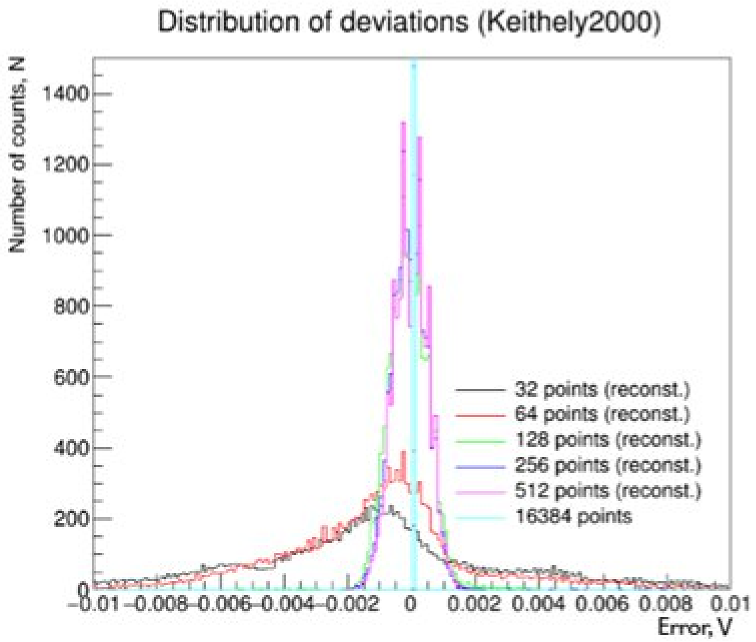




Reconstruction (model test)
(spline algorithm)





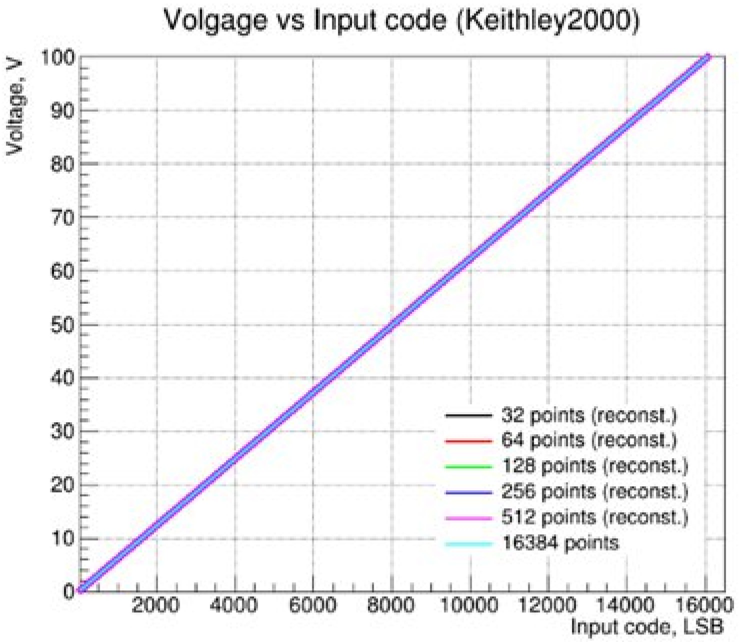


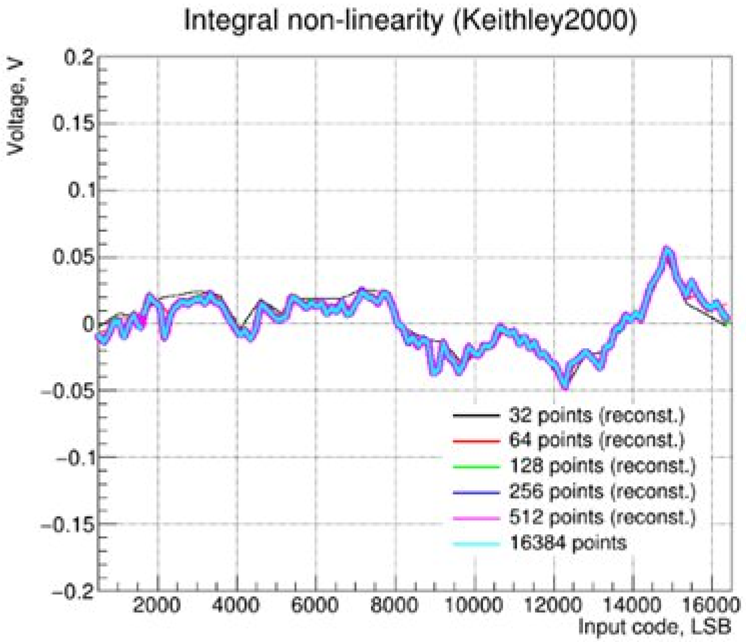
- *16384 points - original data set - measured by Keithley multimeter*
- *32 points (reconst.)… - curves with the reconstructed intermediate points (also 16384 points inside)*

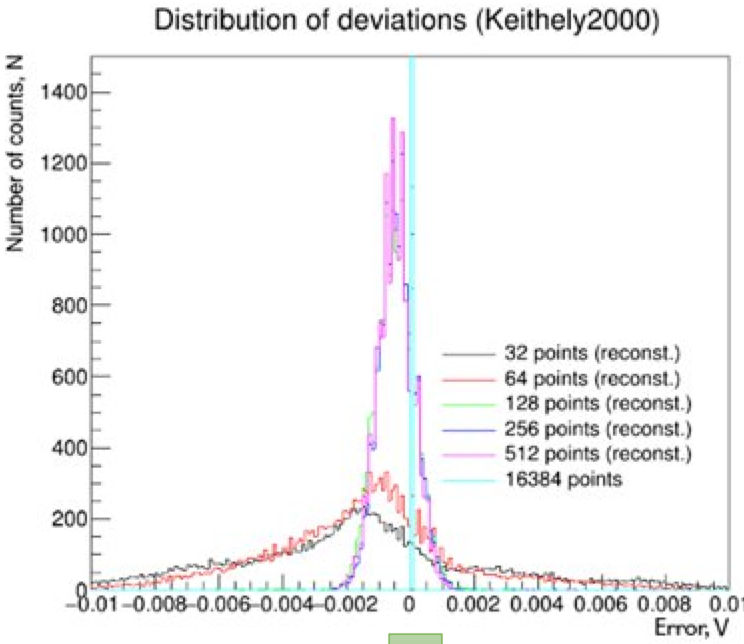
Reconstruction (real data)
(spline algorithm)

The algorithm was applied on the real data:

- *Voltage was scanned (32, 64, 128, 256, 512 points) by means of Keithley 2000*
- *Intermediate points were reconstructed the same way for each set of points*

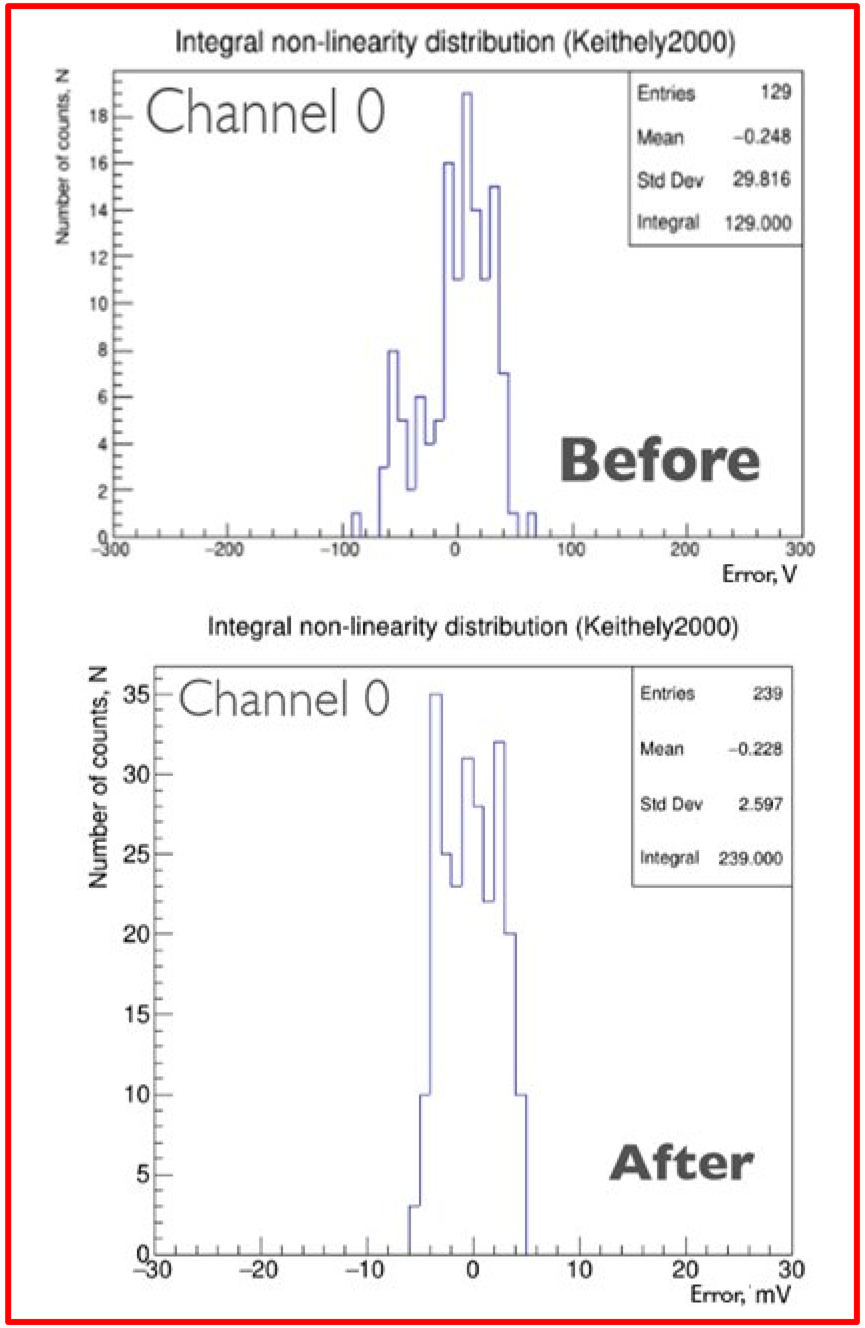


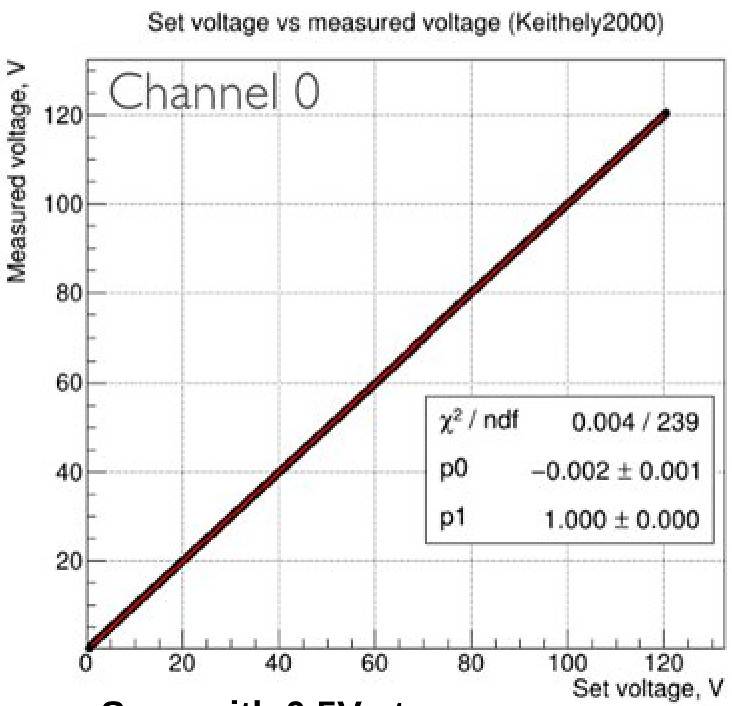




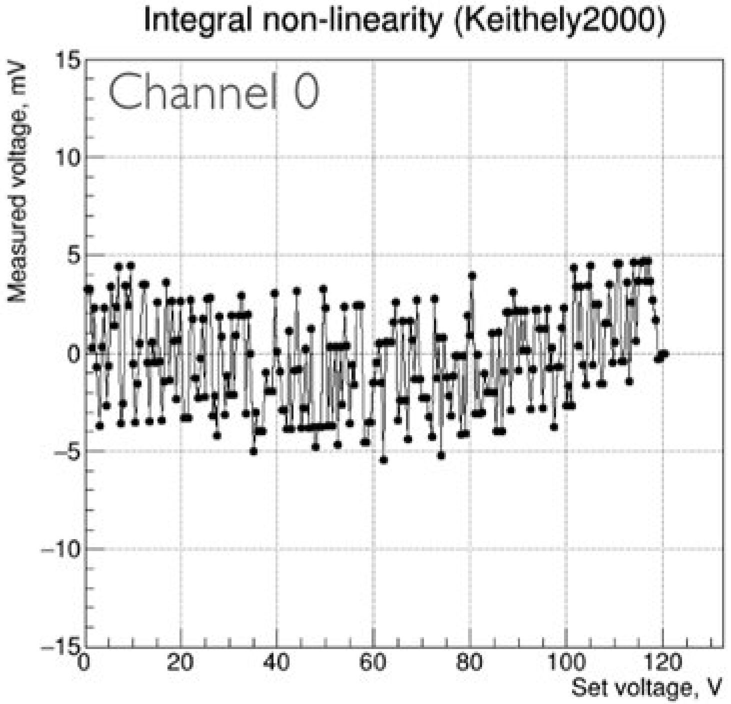
- Over 128 points must be acquired for calibration of a single channel
- time: ~10 min/128 points is required
- 128ch*10min ~ 20h/Power Unit
- Switching channels in automatic mode is needed (multiplexer)

Applying of correction on a single channel





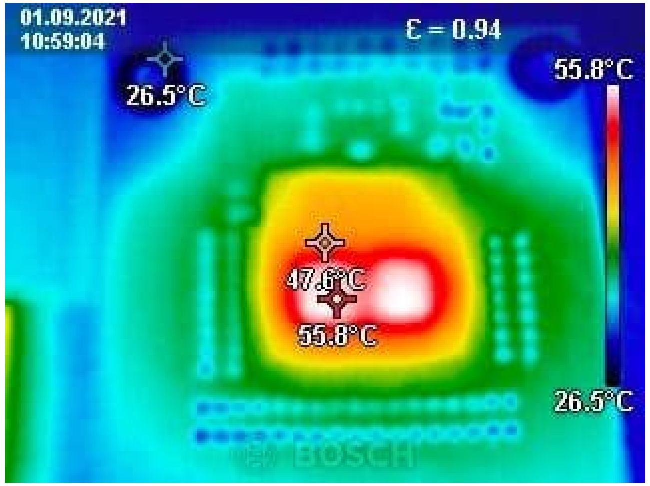
Scan with 0.5V step



Temperature stability

AD5535B chip operating range from –10°C to +85°C

Initial temperature: 35°C



ΔT ~20°C ΔV~2mV

ΔT ~30°C ΔV~3mV

ΔT ~40°C ΔV~5mV

The crate and heat sinks keep the chip temperature from +25°C to +30°C in range from 0 to 200V

Outstanding issues and plans

- Precise calibration photodetector use?
- QA/QC protocol
- Longitivity and screening tests
- Slow control system (concept and development)
- Update from CAN to CAN-Open protocol
- Optimizing firmware and software for performance. WEB application.
- Using a control unit to monitor power units
- Simultaneous calibration of multiple power units
- Tests of power units with real detector prototypes (TAO - October, DUNE - November)

Summary

- The design of a control unit and a power unit with a DAC AD5535B chip has been developed
- Power supply unit management software developed
- A method for calibrating the power unit has been obtained. For a successful calibration of one channel, it is enough 128 points.
- It is necessary to use heat sinks and a ventilated crate for DAC chips. The voltage change will be less than 1 millivolt.
- The cost of one channel is 10$, which is significant cheaper than foreign analogs.

Thank you for your attention