Status of the concentrator chip development for TPC

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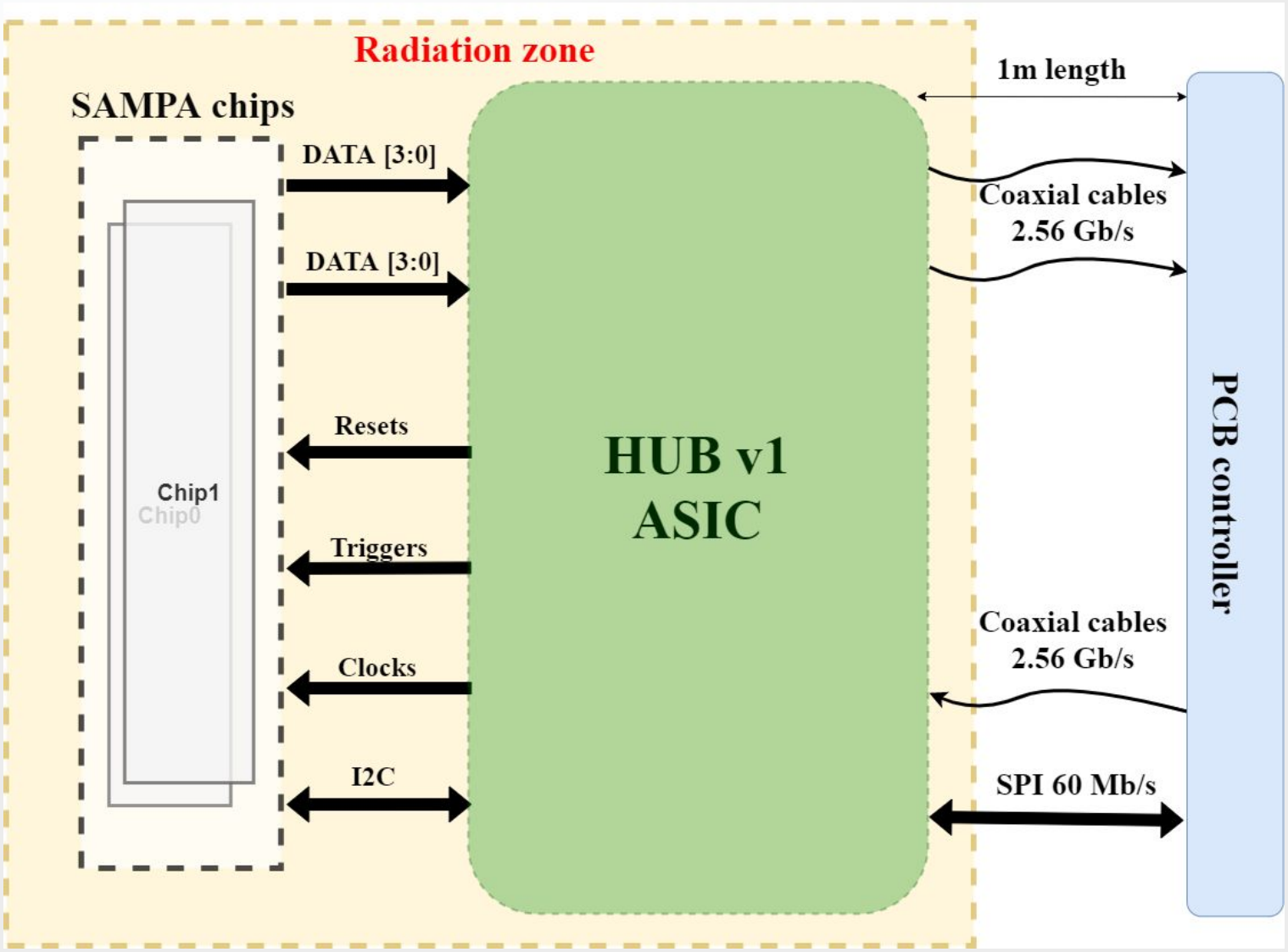
Outline

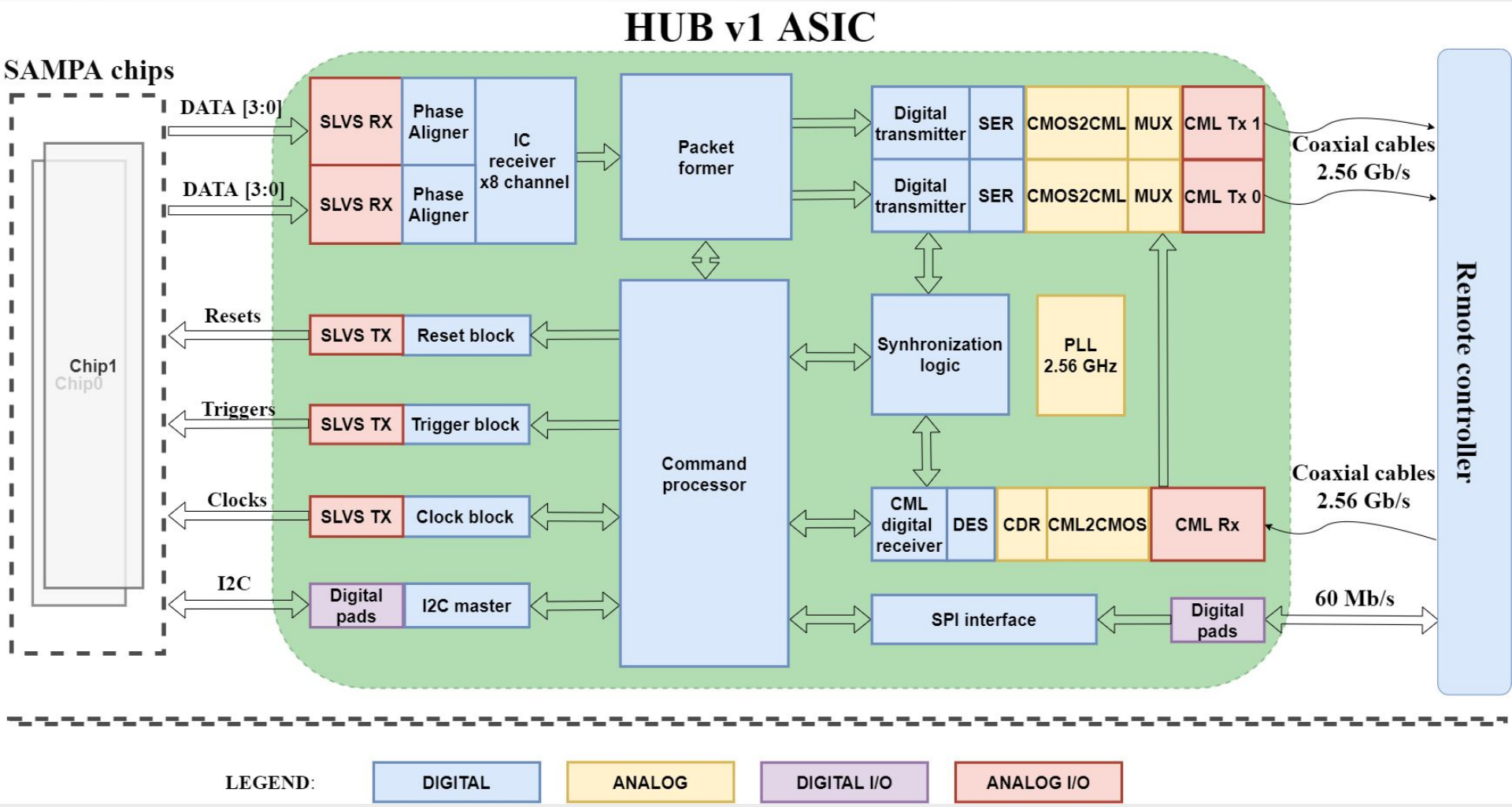
- Hub v1 ASIC
- Activity status
- Test stand
- Demonstrator for TPC
- Hub v2 ASIC

ASIC function

is data concentration and transfer from two SAMPA chips to counting room via fast 2.56 Gb/s bi-directional interface



Block diagram



Layout

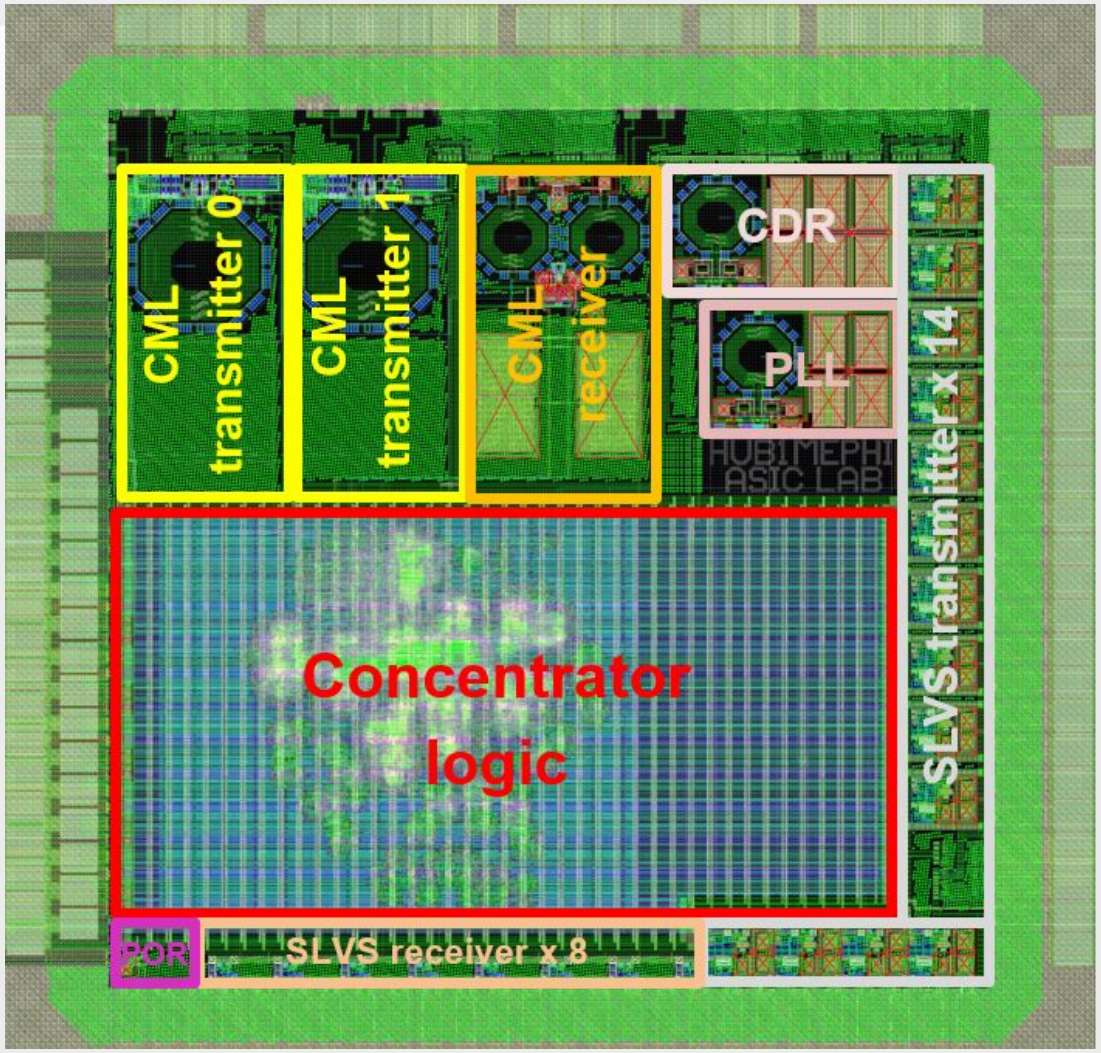
1) Process – TSMC65 LP MS RF
   1P9M_6X1Z1U_RDL;

2) Chip area – 1980 x 1980 um;

3) Bond pads – 111
   37 type CUP staggered
   74 type IN-LINE
   Pad size – 57 x 69 um
   Pad Pitch – 60 um

4) Europractice technological run of Nov. 2020

5) 2 types of packaging:
   CPGA 120 (10 pcs) & caseless (80 dies)



Specifications

Specifications	Value
Technology	TSMC CMOS 65 nm
I/O voltage	2.5 V
Core voltage	1.2 V
Power consumption	< 500 mW
Radiation tolerance	> 100 Krad
Input control interface	1 channel, speed - 2.56 Gbit/s, type - CML
Data output interface	2 channels, speed - 2.56 Gbit/s, type - CML
Data input interface	8 channels, speed - 320 MHz, type - SLVS
Output control interface	IIC , 10 bit address , frequency 100 kHz ÷ 5 MHz, LVCMOS
Synchronization interface	6 channels, 5/10/20/40/80/160/320 Mbit/s, type - SLVS
Trigger output channels	6 channels, type - SLVS
Reset output channel	2 channels, type - SLVS

Radiation tolerance

1) Well characterized 65 nm TSMC (Taiwan) design process was used

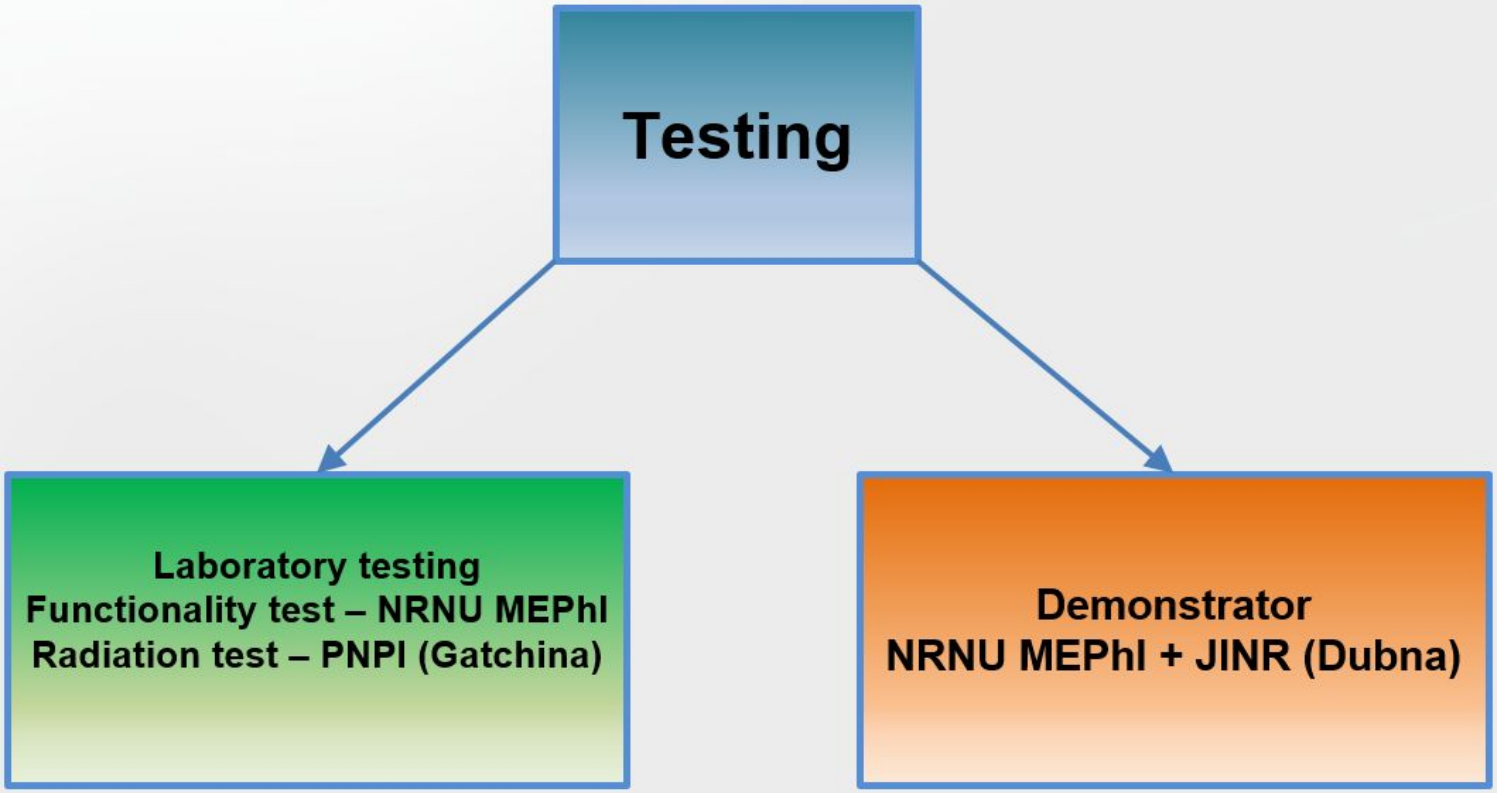
2) The number of high-impedance nodes was reduced. To the remaining nodes low-pass filtering was applied

3) Channel length optimization (bandwidth vs tolerance) to reduce small channel radiation effects was done

4) Majority-logic schemes were employed in critical digital blocks

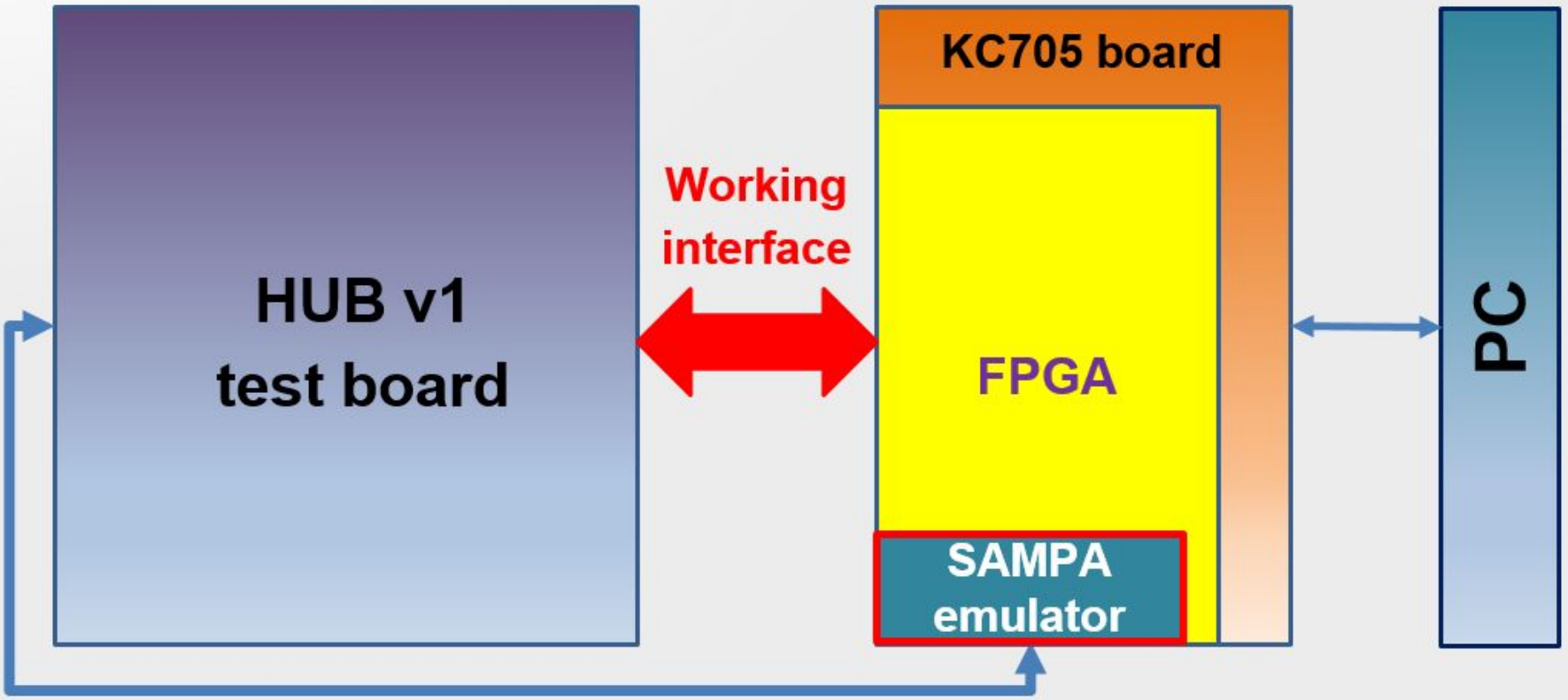
Current status

1) Fabricated Hub v1: 10 chips in CPGA-120 package and 80 chips - caseless
2) Hub v1 is in laboratory testing phase
3) Prototype demonstrator is being built

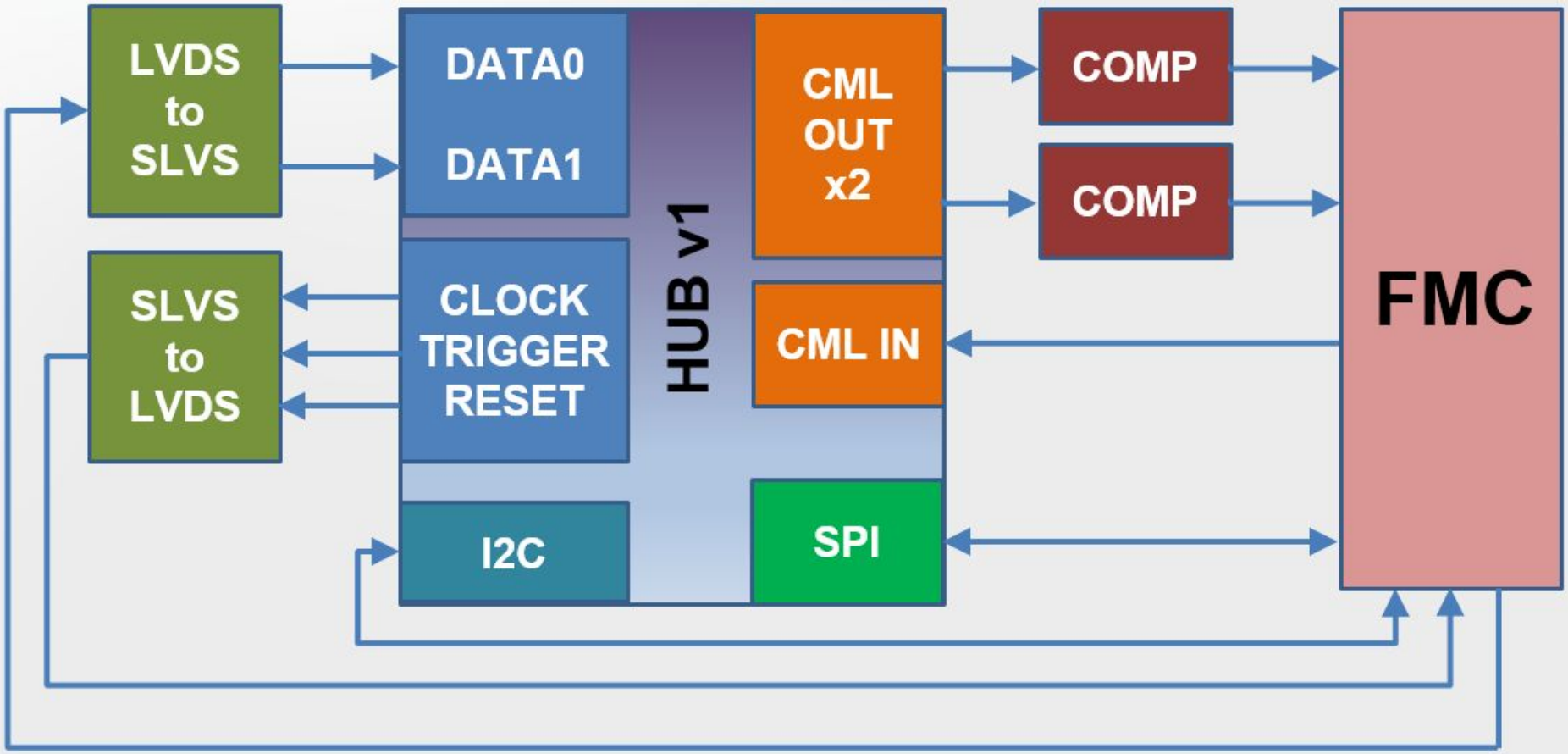


Structure of test stand

Purpose - check functionality of the chip at lab conditions

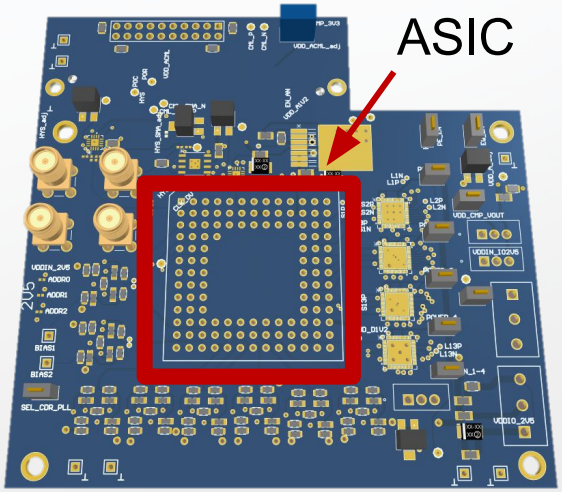


Test board block diagram

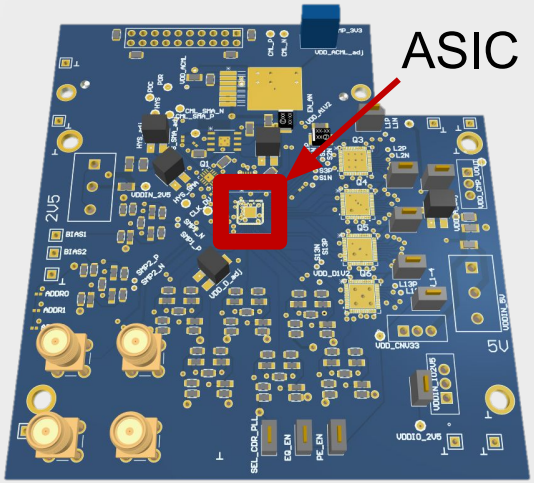


PCBs for lab tests

PCB with CPGA-120 socket



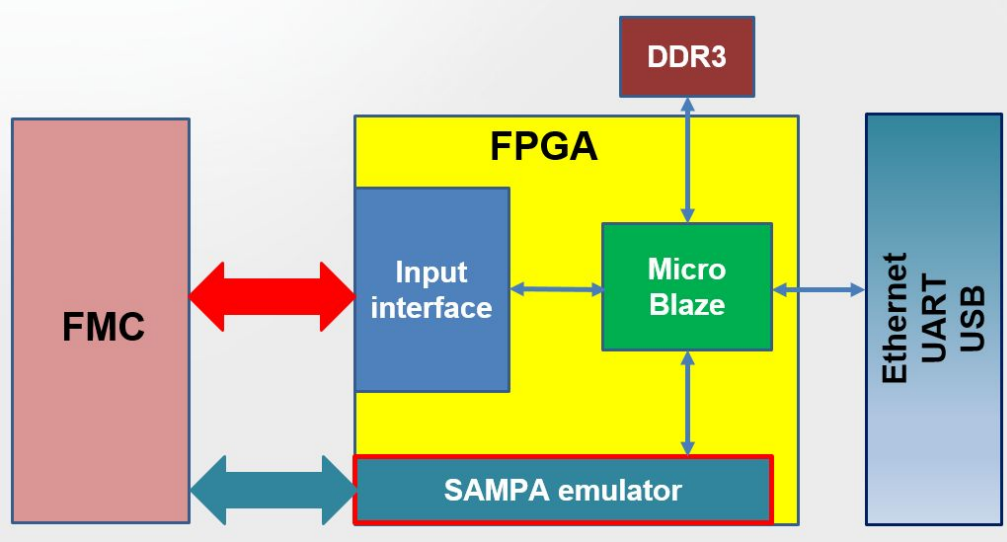
PCB with caseless chip



- Two versions: in CPGA-120 socket (initial testing) and caseless (final testing)
- SLVS – LVDS translators ICs and passive discrete components
- Comparators with adjustable hysteresis to evaluate CML eye-opening at different loads
- FMC HPC (on back side)

PCBs are under manufacturing

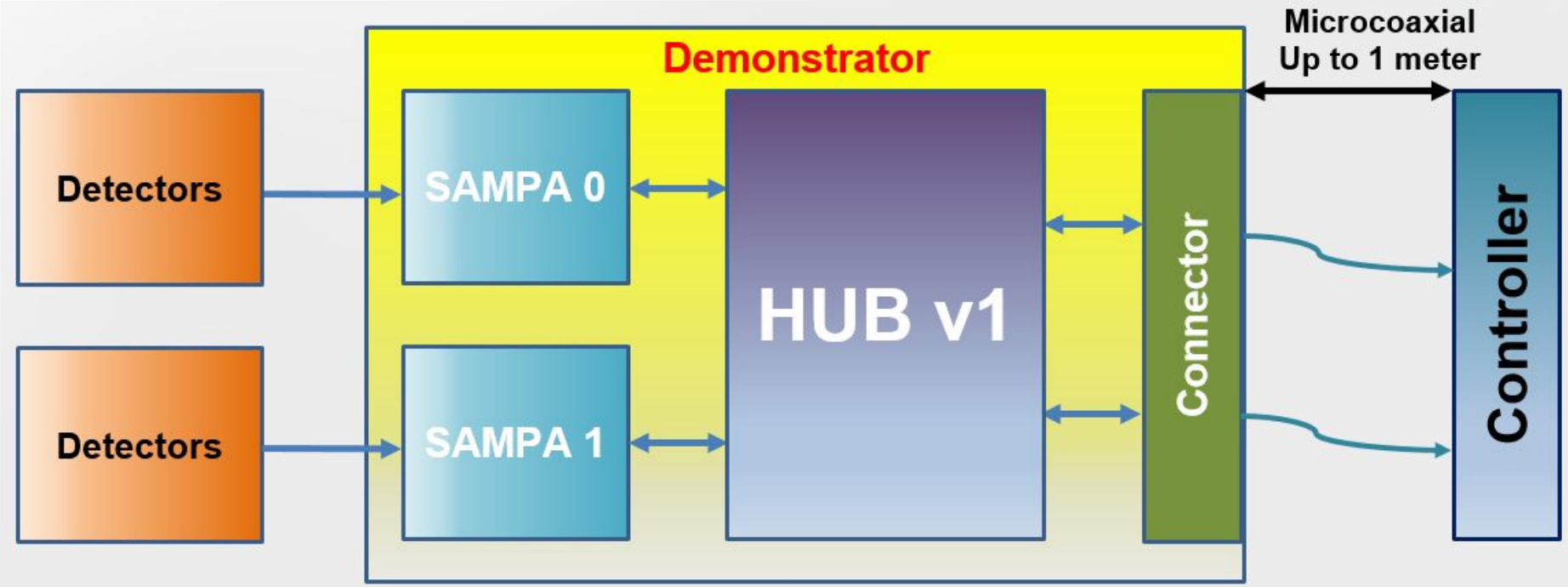
KC705 FPGA control board



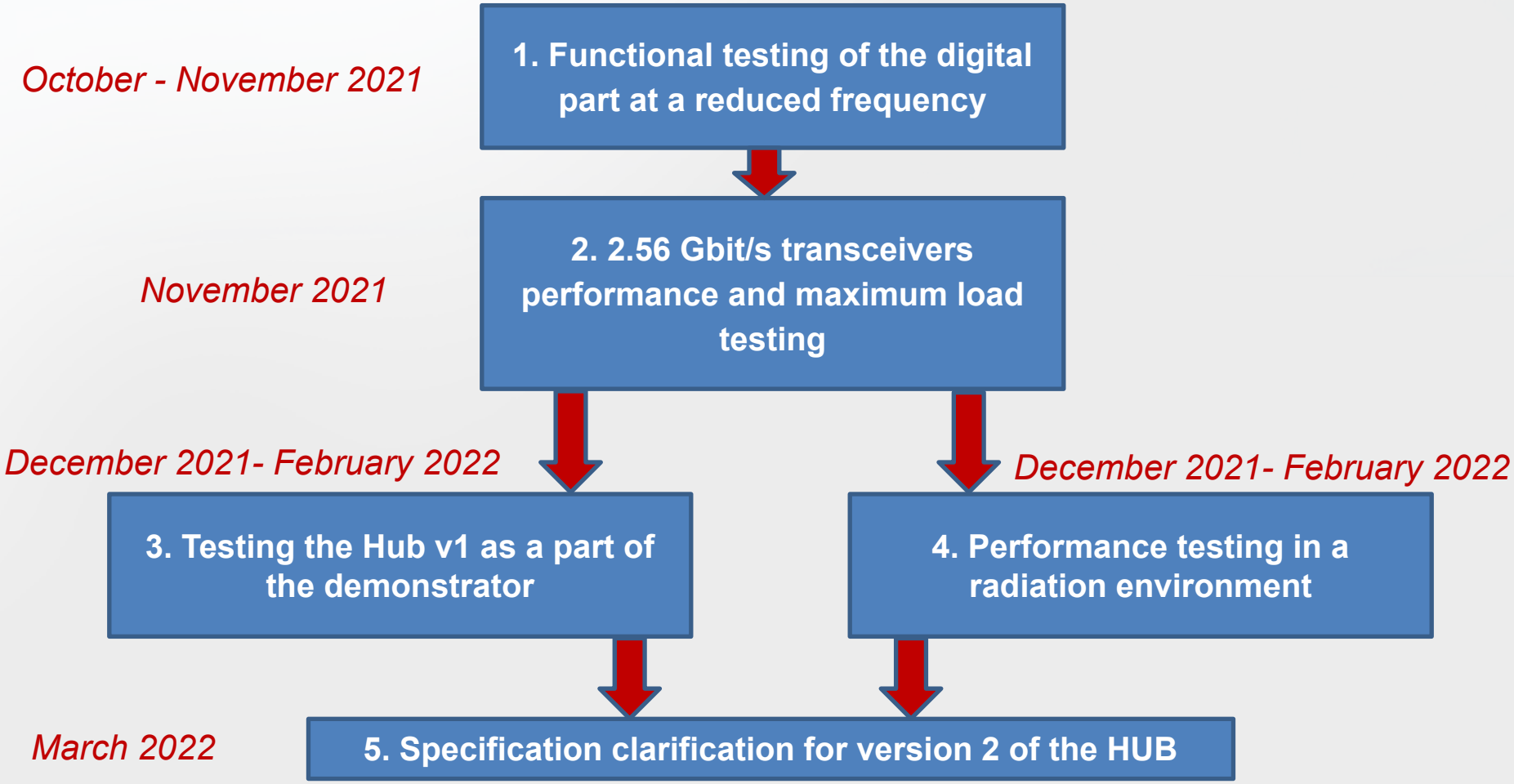
Key features:

- Kintex-7 XC7K325T FPGA with MicroBlaze capability
- 1 GB DDR3 memory
- USB port with USB-to-UART bridge
- 1000 Mb/s Ethernet interface
- FMC HPC:
  - 4 high-speed GTX transceivers
  - about 70 differential LVDS lines

Block diagram of the demonstrator



Hub v1 testing plans



Next version of the chip – Hub v2

Planned are:

1) Study additional measures to improve the radiation resistance of the IP blocks against heavy charged particles

2) Shift to a flip-chip bonding

3) Optimize the size and functionality of the digital blocks

4) Based on the Hub v1 test results, adjust the IP blocks to improve their characteristics

Summary

- Two versions of boards for testing of Hub v1 ASIC are developed. They are in production
- Development of test technique for Hub v1 is in progress
- Demonstrator board is under development
- The design of the 2nd version HUB with improved radiation resistance and block parameters is planned