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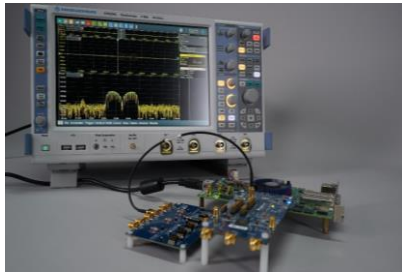
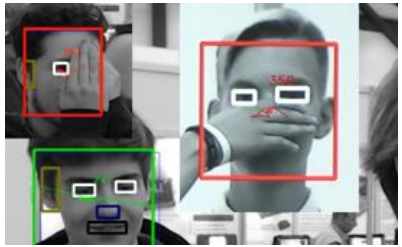
POLYTECH
Laboratory Industrial Systems for Streaming Data Processing






SPD Meeting

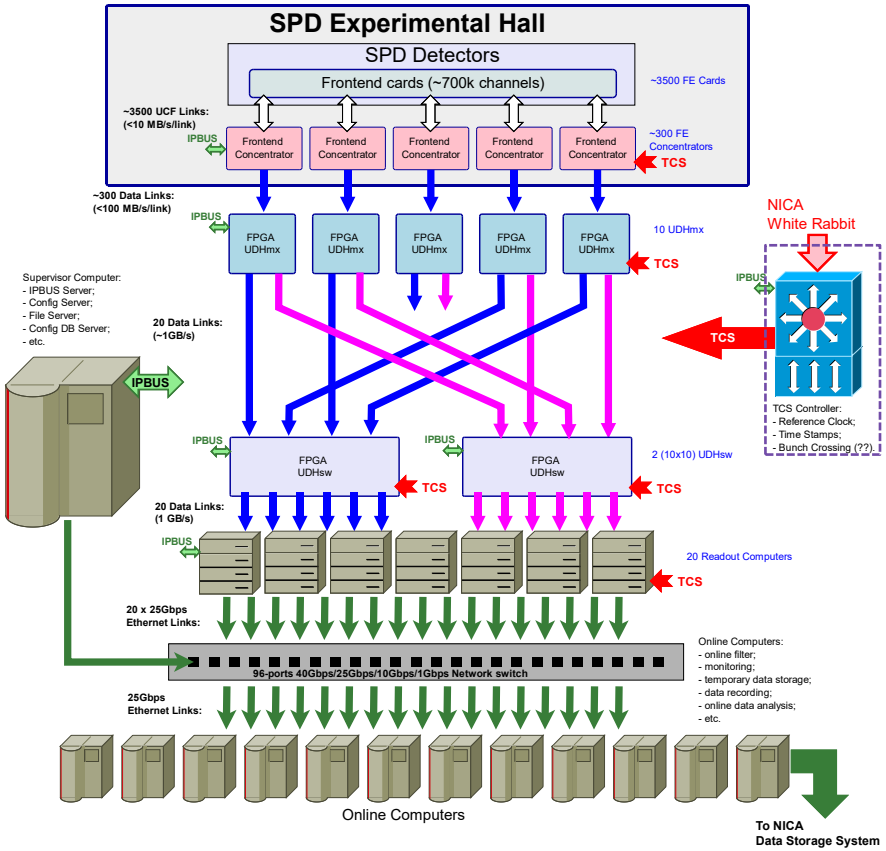
September 23rd, 2021

TCS (COMPASS) reengineering for DAQ-SPD

Andrey Antonov, Lead Engineer
Anton Doinikov, Engineer
Olga Mamoutova, Engineer
Ivan Orlov, Engineer

Laboratory “Industrial Systems for Streaming Data Processing”, SPbPU NTI Center

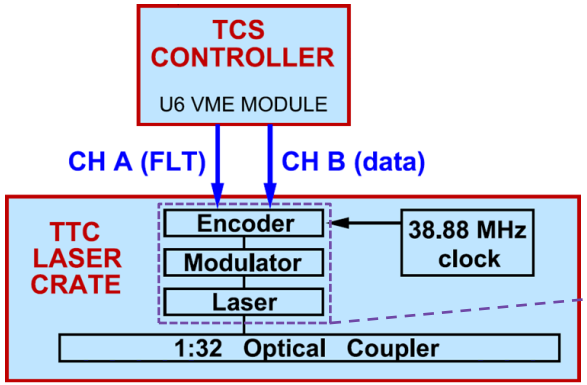
TCS (COMPASS) reengineering for DAQ-SPD

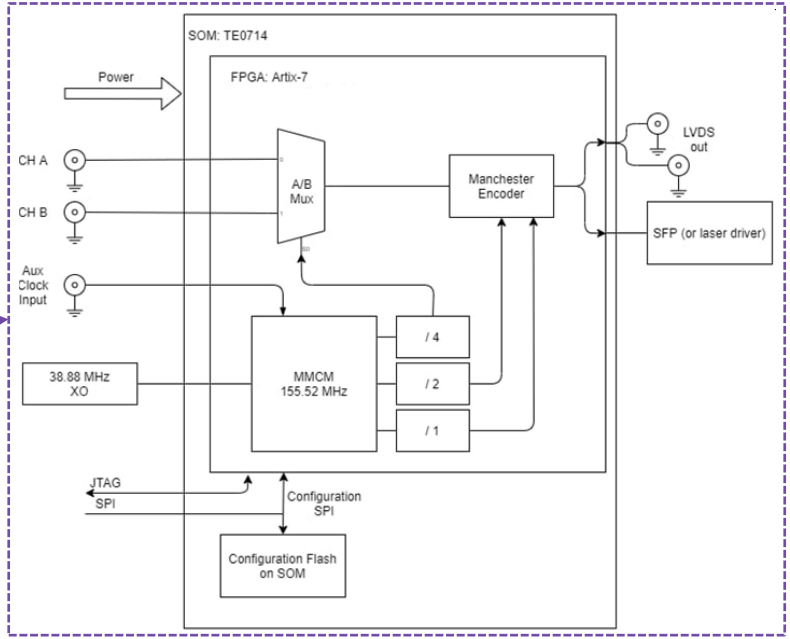


TRIGGER (TIMING) AND CONTROL SYSTEM – PILOT PROJECT

- Heart of the DAQ – orchestrates work of the whole system
- Pretty simple but crucial system component
- COMPASS TCS is not suitable for the triggerless DAQ-SPD system
- High demand for performance improvement in DAQ-SPD
- COMPASS TCS hardware is based on obsolete components
- Little to no technical support from the developers

TCS (COMPASS) reengineering for DAQ-SPD



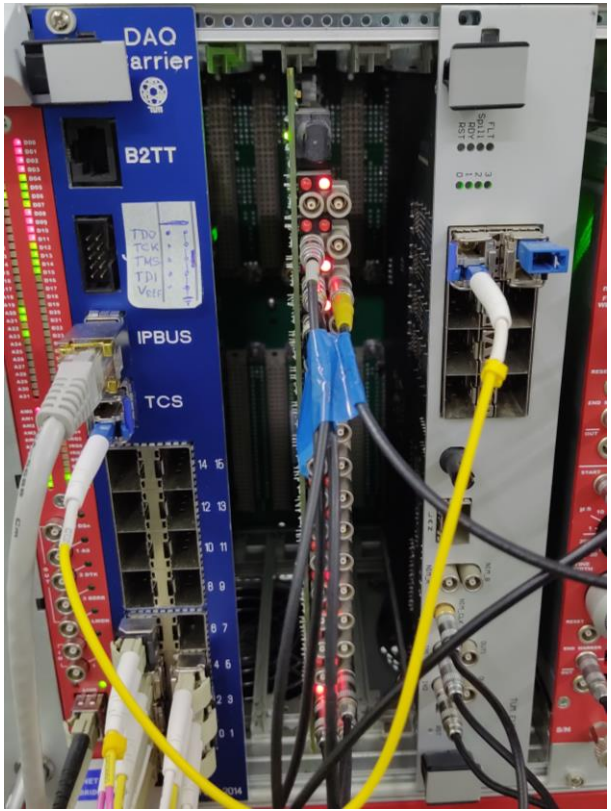


- Fully function-compatible with the original COMPASS TCS
- Xilinx Artix-7 FPGA-based hardware platform
- Rapid device development using Trenz TE0714 SoM
- Different form factor – no need of using VME for standalone device
- Planned implementation in a 19-inch rack unit with standard AC power supply – TCS does not require high-precision or exotic supply voltages
- Low-cost solution

TCS (COMPASS) reengineering for DAQ-SPD

ROADMAP: TCS FOR STRAW TRACKER

- **Schematic and PCB design – TCS Controller + Encoder**
- **TCS Encoder FPGA design**
- **TCS Encoder debugging and testing in the real straw tracker experiment environment**
- Full TCS FPGA design
- Full TCS debugging and testing in the real straw tracker experiment environment



ROADMAP: FURTHER STEPS

- TCS architecture redesign for DAQ-SPD
- New TCS development, debugging and testing
- Optimization of online processing tasks and DAQ

TCS (COMPASS) reengineering for DAQ-SPD

PROSPECTIVE APPLICATION OF RESEARCH INTERESTS IN CURRENT AND FUTURE PROJECTS

- Reengineering: the problem of a conceptual model recovery during modernization of inherited equipment according to new requirements. Application to TCS Encoder and TCS subsystem
- Reliability: the problem of evaluation of an architectural vulnerability to SEU. Application to TCS subsystem and other DAQ nodes located at the middle level
- Application of our expertise in White Rabbit sub-nanosecond synchronization: we have successfully ported WR on various FPGA-based platforms

Contacts

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