ARCADIA

Technology and Status Report

Spin Physics Detector Meeting
July 12th, 2021

Istituto Nazionale di Fisica Nucleare

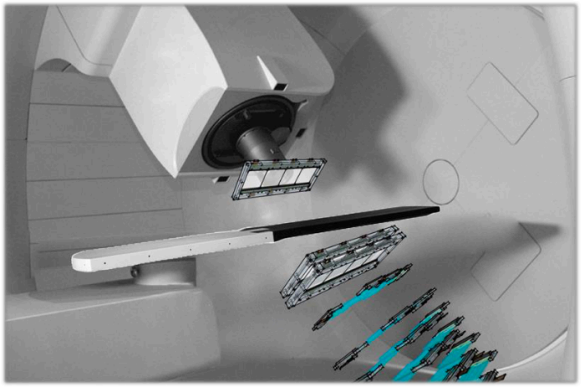
Manuel Da Rocha Rolo (INFN)
on behalf of the ARCADIA Collaboration

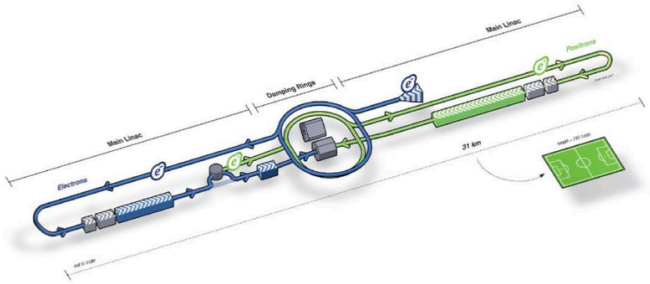
ARCADIA: CMOS DMAPS platform at INFN

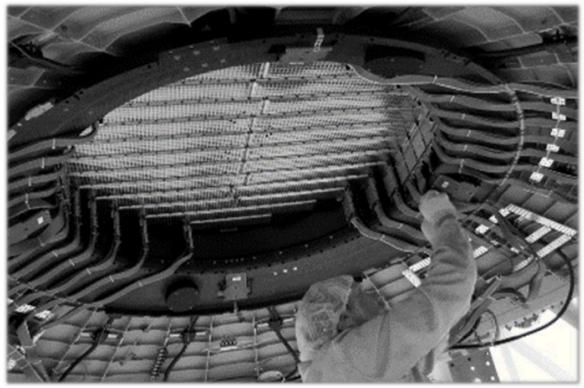
What do we want: to develop a design and fabrication platform for large-area fully-depleted CMOS sensors, at the moment targeting space, medical and future HEP infrastructures (thin sensors) and X-ray detectors (thicker sensors)

What do we need from the silicon foundry:

- access to an engineered CMOS process (developed in collaboration with LFoundry) and custom starting substrates
- access to future SPW runs for dedicated reticle size (next 3 years) and larger-than-reticle (from 2023) designs







Medical
- Low power (≤ 40 mW/cm²)
- Medium rate ≈ 10 MHz – 100 MHz/cm²
- Ultra low material budget (low energy)
- Very large area (≥ 16 cm²)
- 3-side buttable design
- Low to medium rad-tolerance ≈ 10 kGy

e⁺e⁻
- Low power (≤ 40 mW/cm²)
- Medium rate ≈ 10 MHz – 100 MHz / cm²
- Very low material budget
- Large area (≥ 6 cm²)
- 3-side buttable design
- Low to medium rad-tolerance ≈ 10 kGy

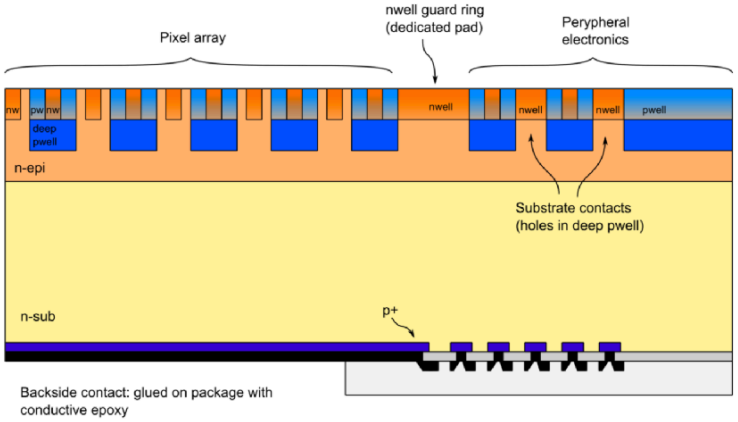
Space
- Ultra low power (≤ 10 mW/cm²)
- Very low rate ≈ kHz/cm²
- Low material budget
- Large area (≥ 6 cm²)
- 3-side buttable
- Low rad-tolerance ≈ 1 kGy

ARCADIA (INFN CSNV Call Project)

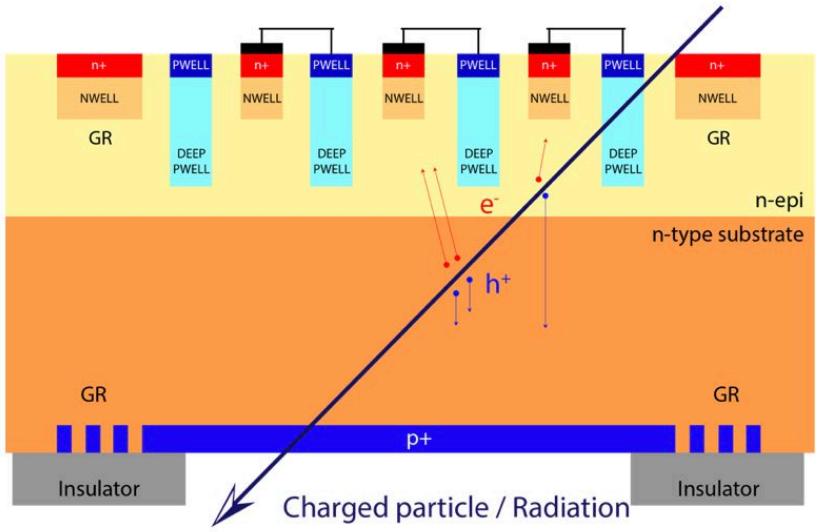
Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

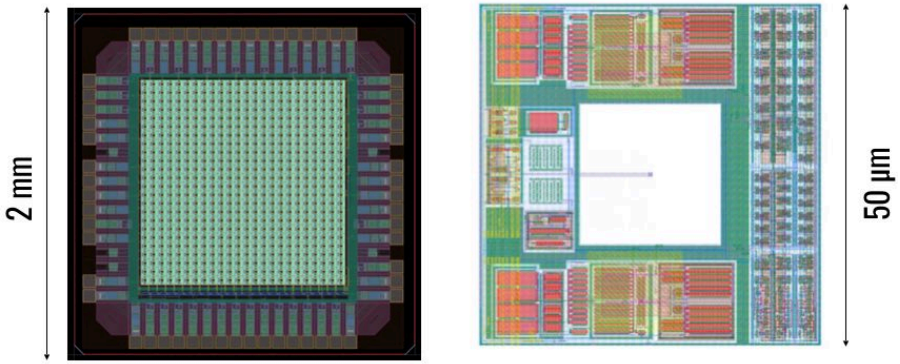
Ongoing activity towards a CMOS sensor design and fabrication platform allowing for:

- Active sensor thickness in the range 50 µm to 500 µm or more;
- Operation in full depletion with fast charge collection only by drift, small charge collecting electrode for optimal signal-to-noise ratio;
- Scalable readout architecture with ultra-low power capability (O(10 mW/cm2));
- Compatibility with standard CMOS fabrication processes: concept study with small-scale test structure (SEED), technology demonstration with large area sensors (ARCADIA)
- Technology: 110nm CMOS node (quad-well, both PMOS and NMOS), high-resistivity bulk
- Custom patterned backside, patented process developed in collaboration with LFoundry



Small-scale demo: MATISSE





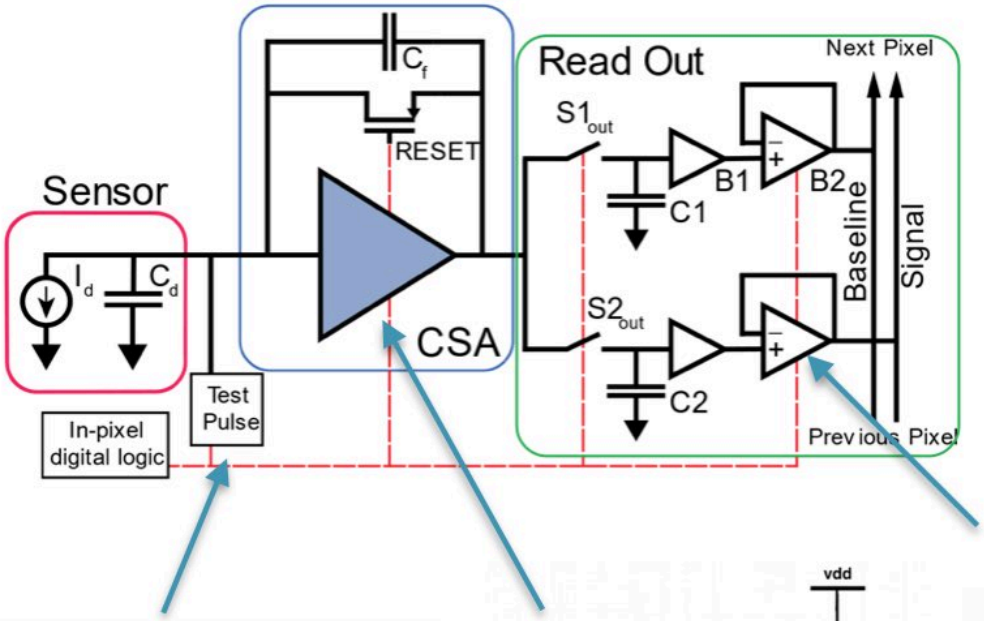
MATISSE

Pixel CAD Layout

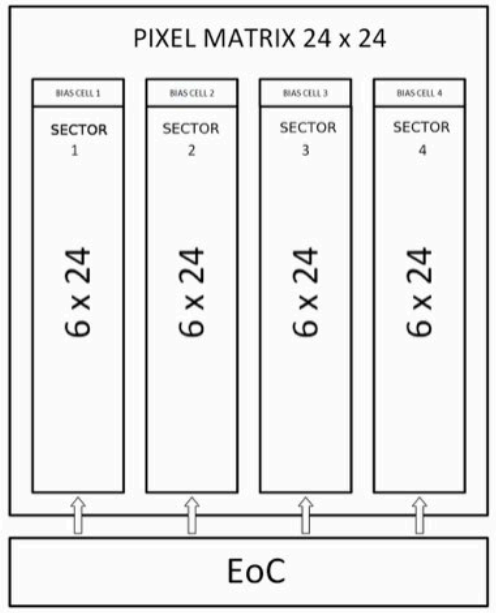
PIXEL ELECTRONICS		
	DESIGN SPECs	RESULTS
Technology	CMOS 110 nm	
Voltage Supply	1.2 V	
Measurements	Hit Position Energy Loss	
Number of Channels	24 × 24	
Input Dynamic Range	Up to 24 ke⁻	
Sensor Capacitance	~20 fF	
Analog Gain	131 mV/fC	116 mV/fC
CSA Input Common Mode Voltage	> 600 mV	
Local Memories	2 (~70 fF each)	
Noise	< 100 e⁻	~40 e⁻
Shutter Type	Snapshot	
Readout Type	Correlated Double Sampling Double Sampling	
Readout Speed	Up to 5 MHz	
Other Features	Internat test pulse Mask Mode Baseline Regulation	

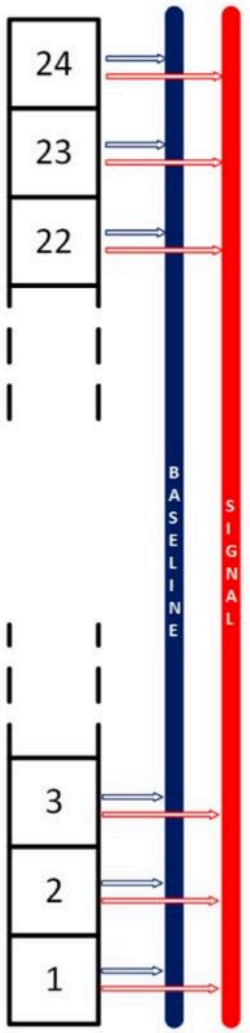
Small-scale demo: MATISSE

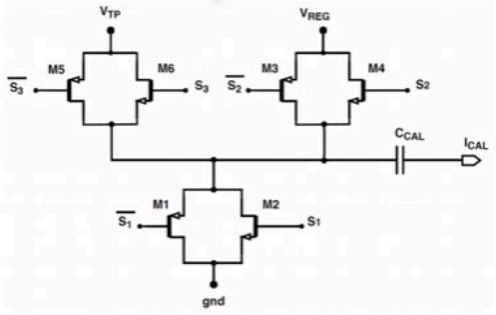
Charge Sensitive Amplifier
With a RESET transistor

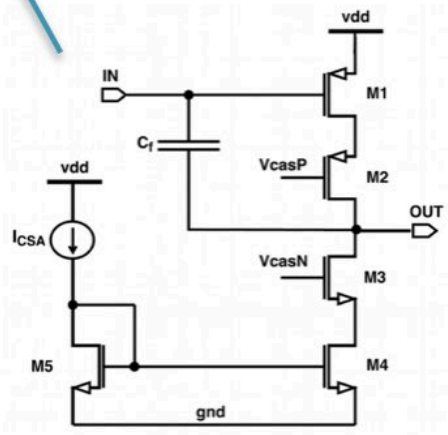


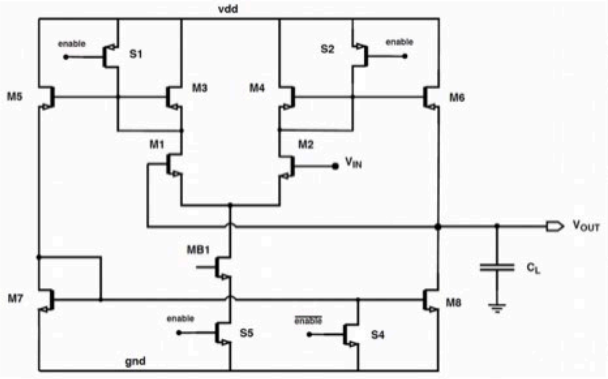
Correlated Double Sampling



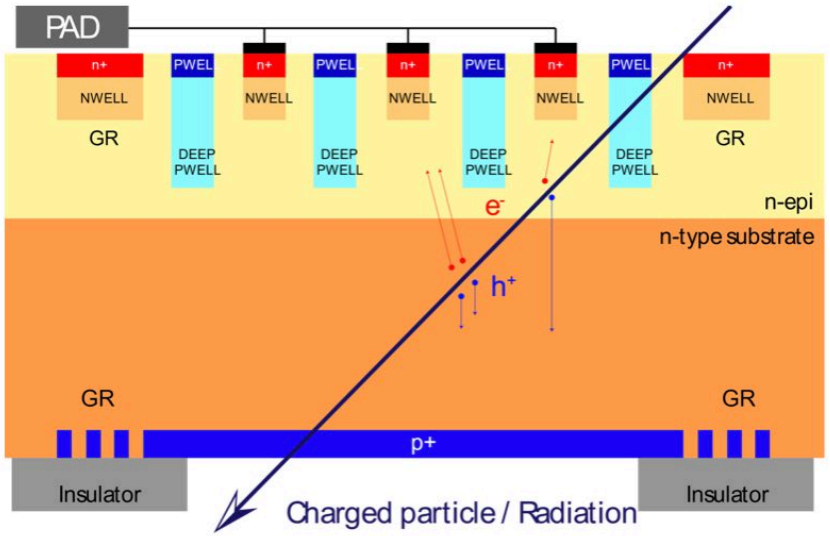




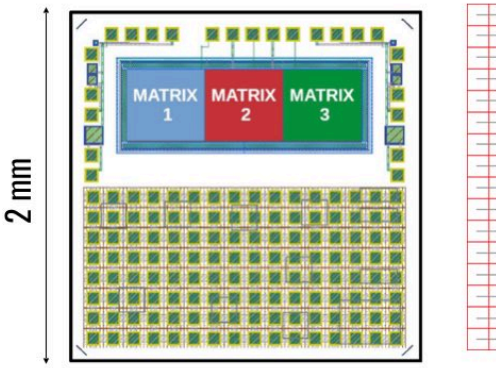




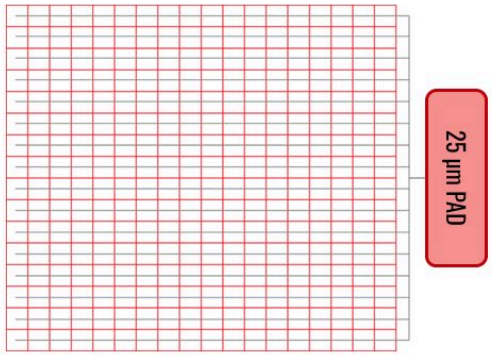
Small-scale demo: pseudo-matrices



- Sensor thicknesses: 100 µm, 300 µm, 400 µm
- Three matrices with different pixel sizes: 10 µm (40 x 45), 25 µm (16 x 18) and 50 µm (8 x 9)
- Front-side deep-pwell, would host the CMOS electronics (no electronics on PMs)



Pseudo-matrix Layout

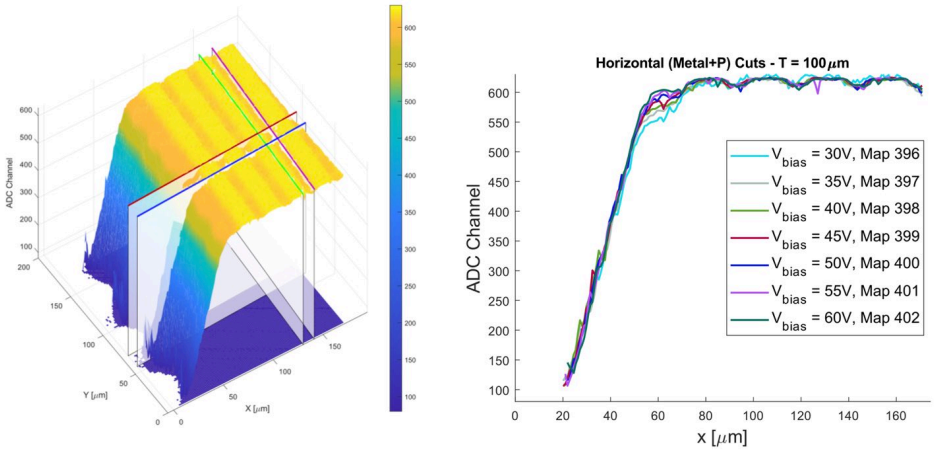


Pixel Scheme

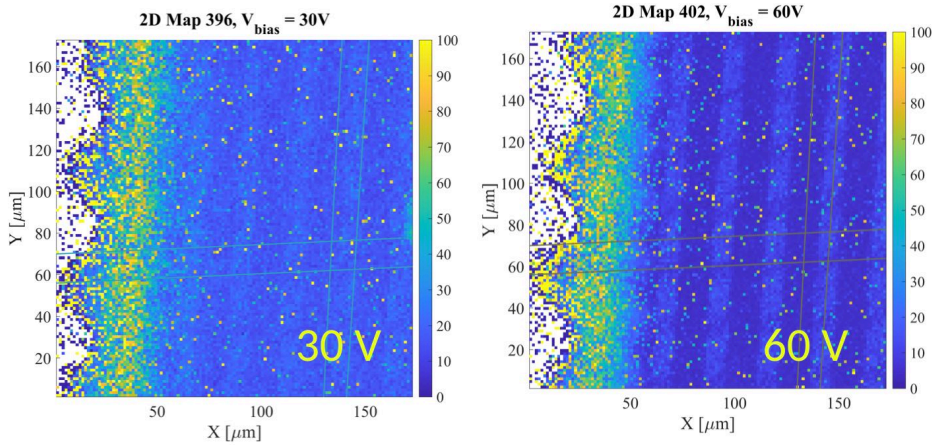
- All the collector nodes of a matrix are shorted and connected to a PAD
- Each pixel is shorted using Al metal lines of increasing width per PM: 6, 8 and 15 µm

Characterisation with pseudo-matrices

Cuts along the Metal + P and Metal + N lines on the energy map with varying bias voltages show uniform CCE above FD with ~1.7 % loss over metals (100 µm thick)



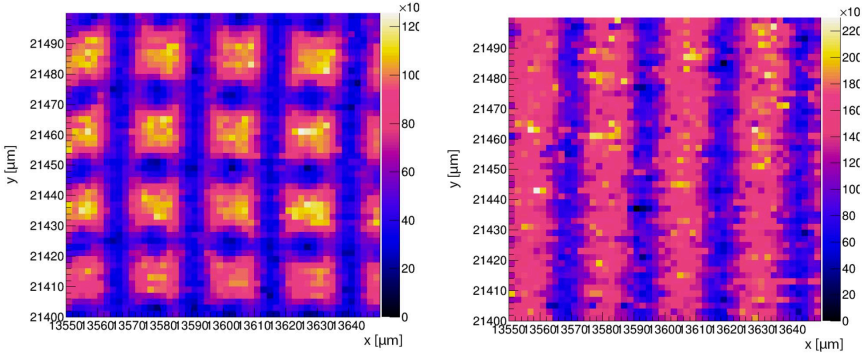
Standard deviation maps show the expected higher electronic noise when the sensor is not depleted (below 30 V), due to the higher top capacitance.



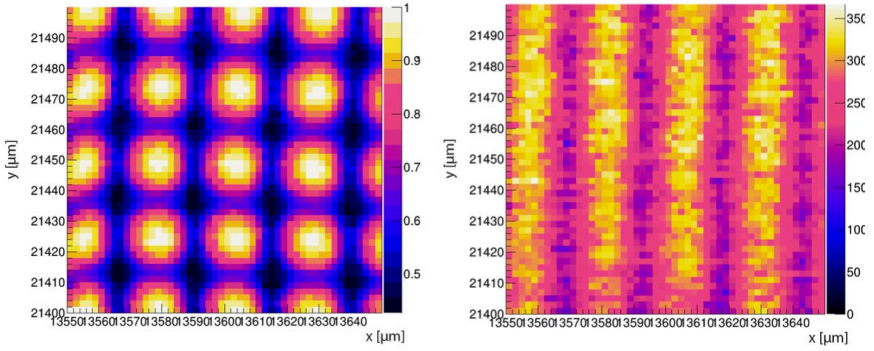
(RUĐER BOŠKOVIĆ INSTITUTE)* Zagreb, Croatia

- 600 keV to 2 MeV Tandetron
- TANDEM 1-6 MeV proton source
- LASER TCT laboratory

TCT Scan: CCE

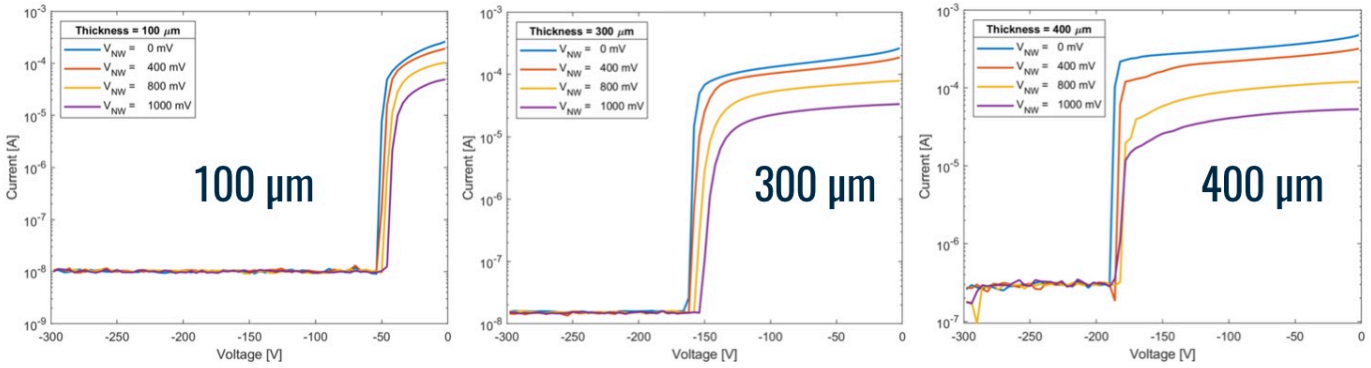


TCT Scan: Amplitude

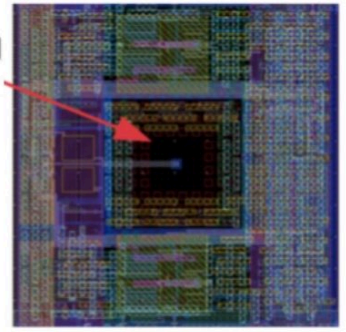


Characterisation with SEED MATISSE

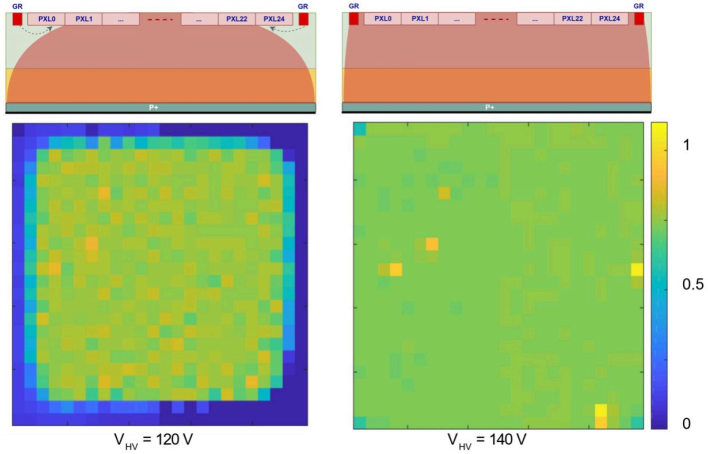
Full depletion studies in 100-300-400 µm prototypes



Low metal density

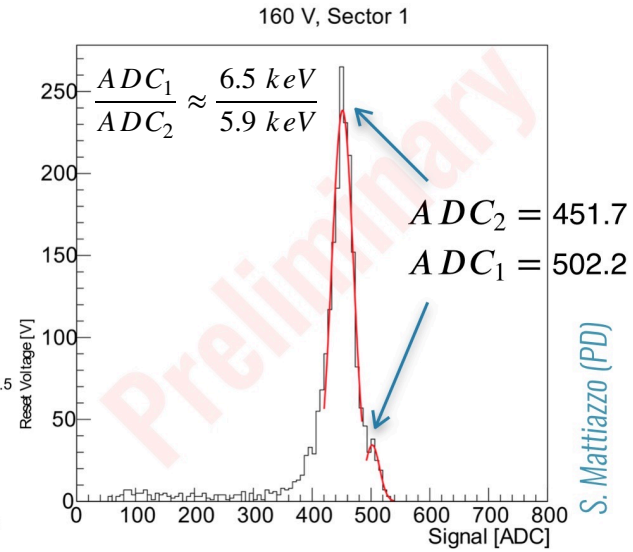


Map of pixel reset voltage (MATISSE 24x24 pixel matrix) as a function of the back-side voltage applied to the sensor. Depletion starts from the back-side.



L. Pancheri (TN)

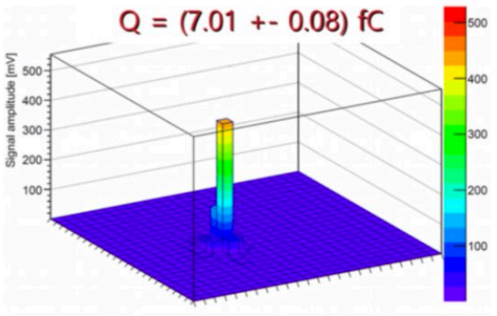
Preliminary results with ^{55}Fe



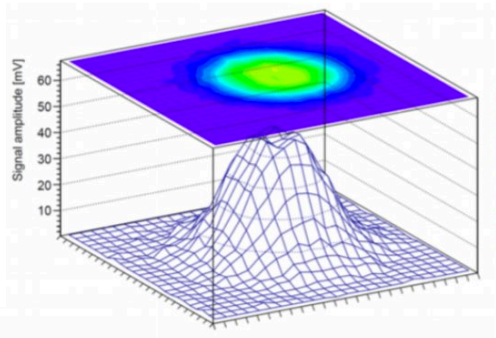
S. Mattiazzo (PD)

The ^{55}Fe emits monochromatic X-rays at 5.9 keV (K_α). A K_β line at 6.5 keV is also emitted with a relative probability below 5%.

Focused pulse



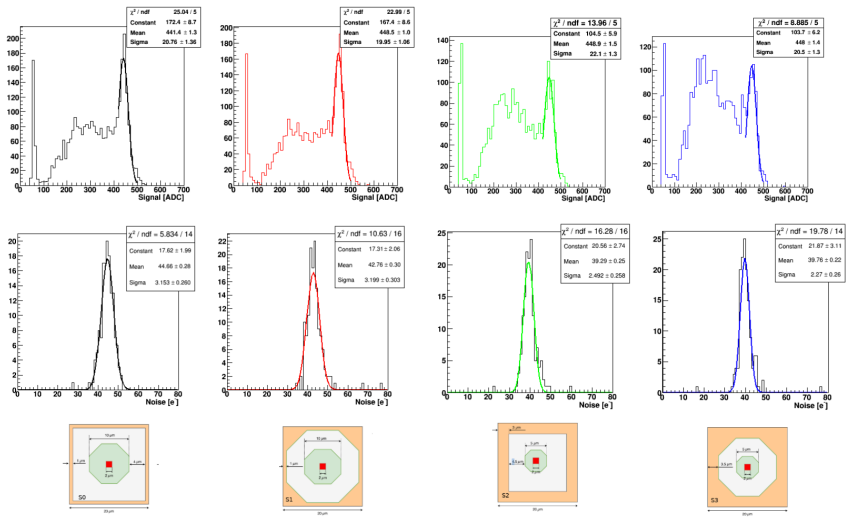
Non focused pulse

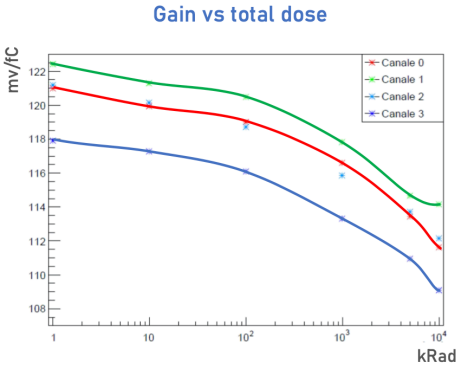


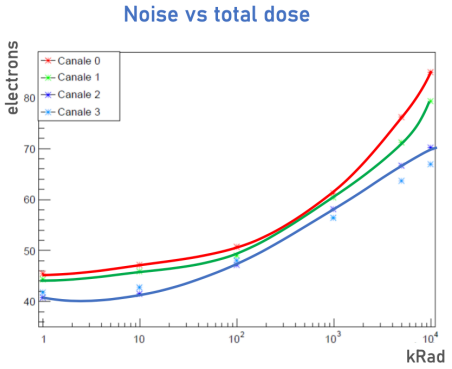
J. Olave FEE2018

Characterisation with SEED MATISSE

S. Mattiazzo (BG)







Gain was calibrated with ^{55}Fe source [Left, signal and noise for the SEED 4 quadrants, featuring different CE geometries]. The gain is only slightly affected up to about 1 kGray (100 kRad). TID is done using x-rays (Seifert machine) .

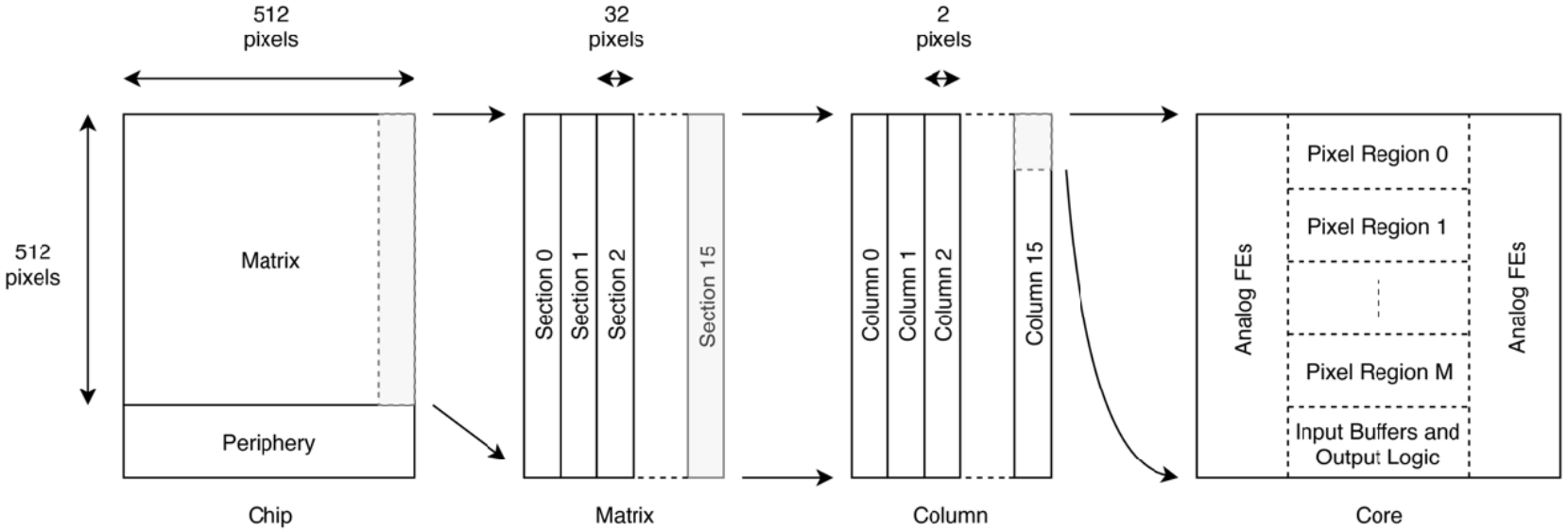
Neutron Irradiation at the Triga Mark II Lubiana (January 2020)

- ☐ 2 boxes 10^{12} 1 MeV neutron equivalent fluence Neutron/cm^2
- ☐ 2 boxes 10^{13} 1 MeV neutron equivalent fluence Neutron/cm^2
- ☐ 2 boxes 10^{14} 1 MeV neutron equivalent fluence Neutron/cm^2

Initial measured activity (1.3E+05) for ^{182}Ta higher than the exemption level.

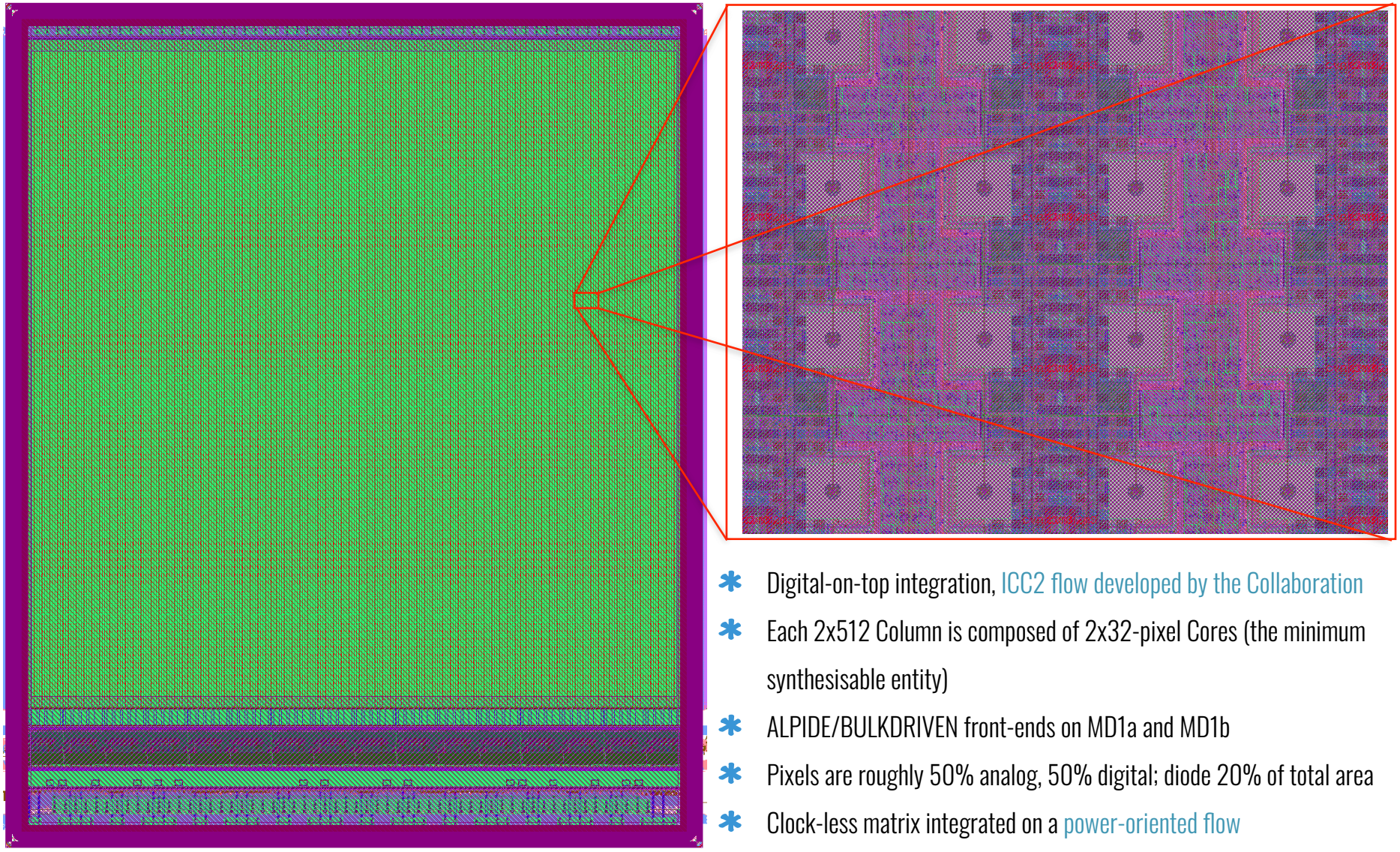
Received 4 (out of 6) boxes, test are ongoing in Padova.

ARCADIA-MD1: Main Demonstrator Chip



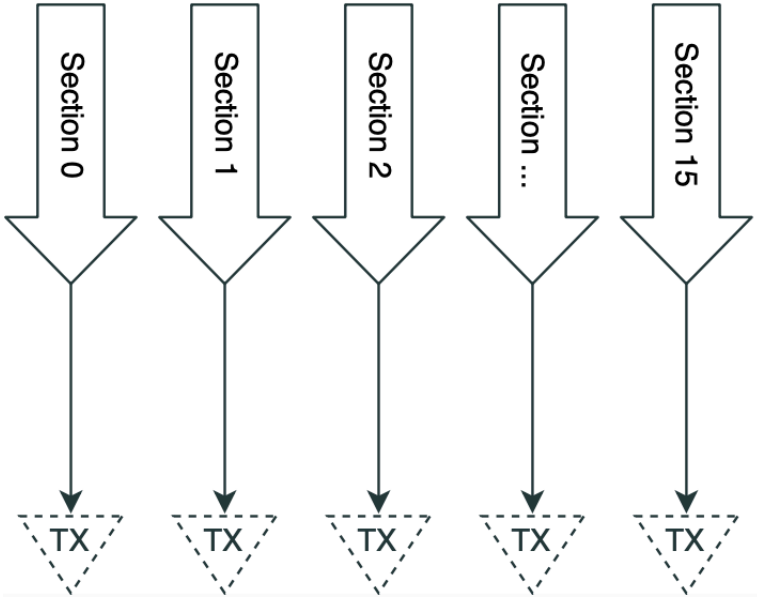
- Pixel size 25 µm x 25 µm: process, back-side pattern and geometry validated in silicon (both MATISSE and pseudo-matrices, electrical, laser, radioactive source and microbeam).
- Matrix core 512 x 512, "side-abuttable" to accomodate a 1024 x 512 silicon active area (2.56 x 1.28 cm^2). Matrix and EoC architecture, data links and payload ID: scalable to 2048 x 2048*
- Triggerless binary data readout, event rate up to 100 MHz/cm^2
- First Engineering Run (SPW) with ARCADIA-MD1 by 11/2020, 2nd full CMOS maskset mid-2021 (higher data throughput, SEU protection, on-chip data compression), 3rd SPW mid-2022 with design fixes, explorative sensor and CMOS designs

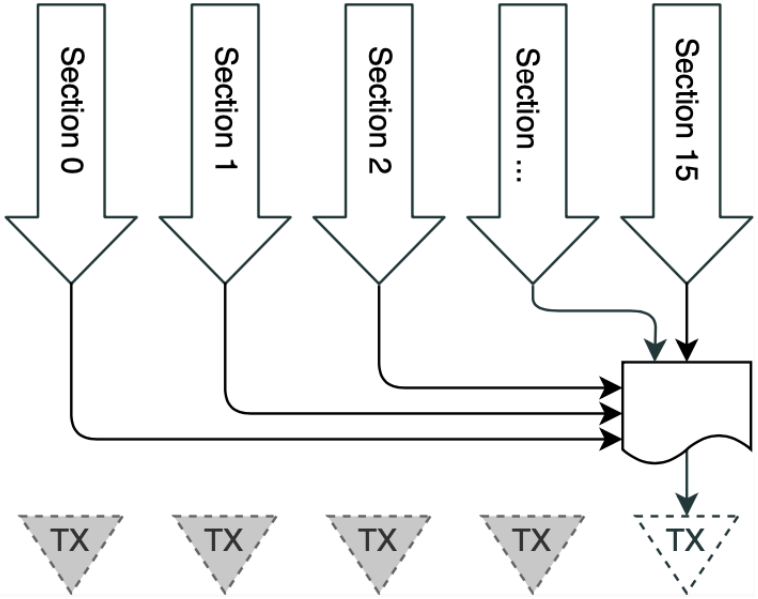
ARCADIA - Main Demonstrator Chip



- Digital-on-top integration, ICC2 flow developed by the Collaboration
- Each 2x512 Column is composed of 2x32-pixel Cores (the minimum synthesisable entity)
- ALPIDE/BULKDRIVEN front-ends on MD1a and MD1b
- Pixels are roughly 50% analog, 50% digital; diode 20% of total area
- Clock-less matrix integrated on a power-oriented flow

ARCADIA-MD1 High-rate & Low-Power Modes





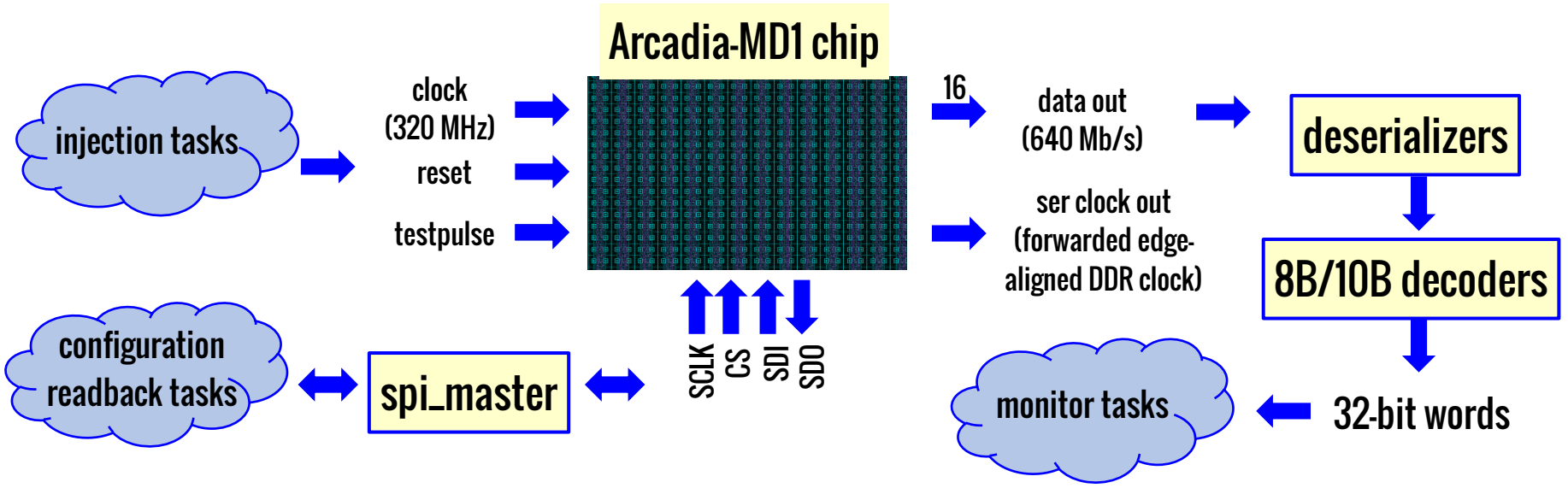
Section Output Unit (SOU)

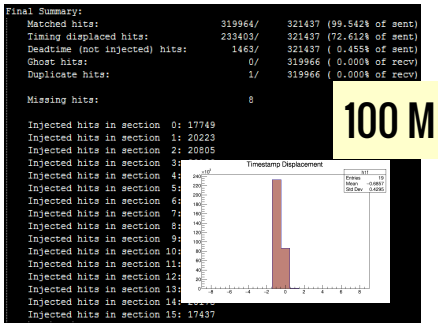
- *320MHz DDR Serializer*
- *8b10b encoder*
- *c-LVDS transceiver*
- *Finite-State Machine*

When configured to operate in ”Low-Power” mode:

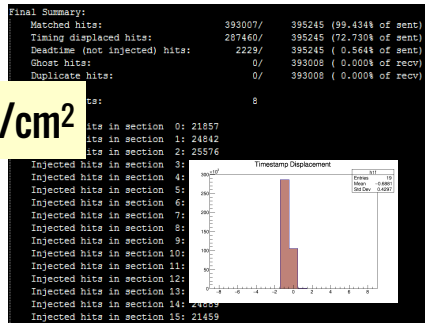
- *Buffers data from all the SRUs in a central FIFO*
- *Gates the clock to all SOU but the SOU_0*
- *Disables all c-LVDS TXs but that of SOU_0*
- *Uses SOU_0 to send the data from the central FIFO*

ARCADIA-MD1 Verification Framework



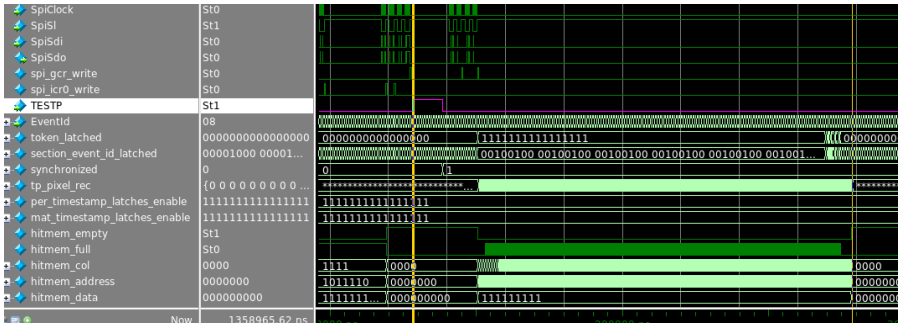


100 MHz/cm^2



dEdx9.2_thetamax0_thickness100_posMED_100MHz_50mmColl_uniform

dEdx23_thetamax4_thickness100_posMED_100MHz_50mmColl_uniform

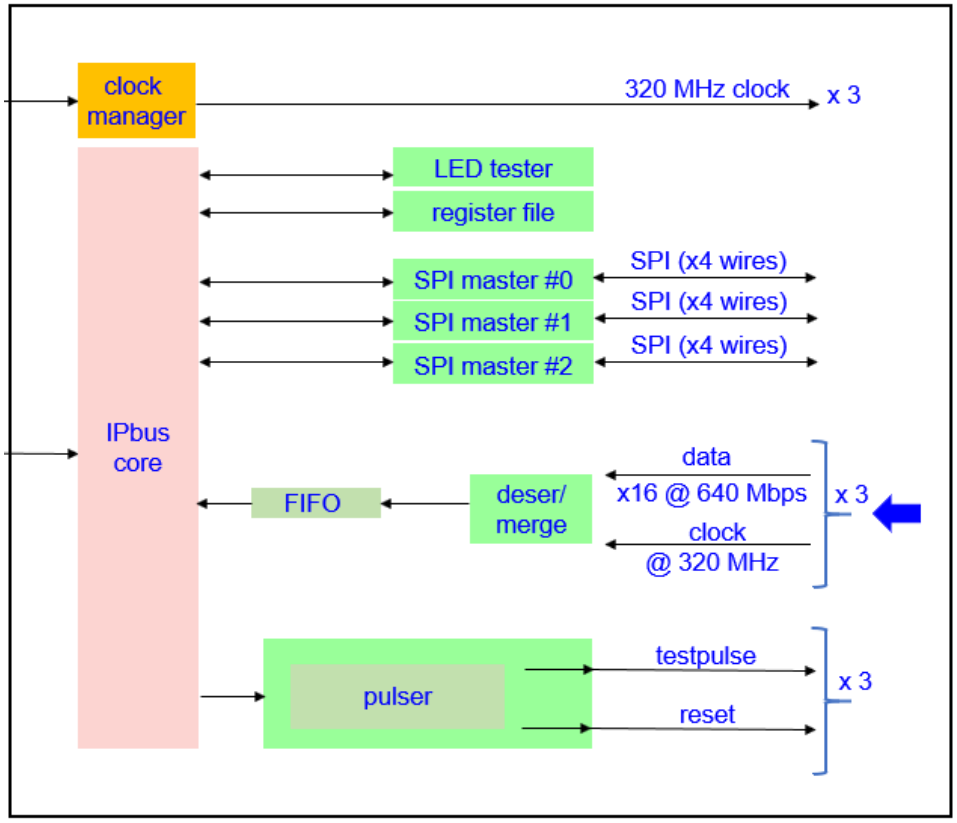


ARCADIA DAQ Firmware

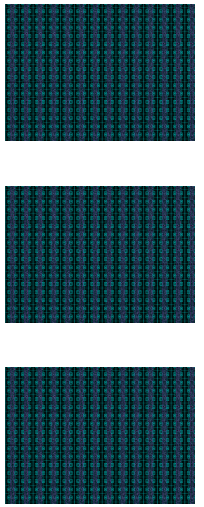
- The DAQ firmware blocks have also been inserted into the same simulation framework used for the ARCADIA-MD1 chip verification;
- We currently have a **universal simulation framework** in which the **ARCADIA-MD1 chip is configured and readout** via IPbus atomic operations **through the DAQ blocks**. This list of atomic operations is also being translated into the software running on the PC, which is being designed.

IPbus tasks:

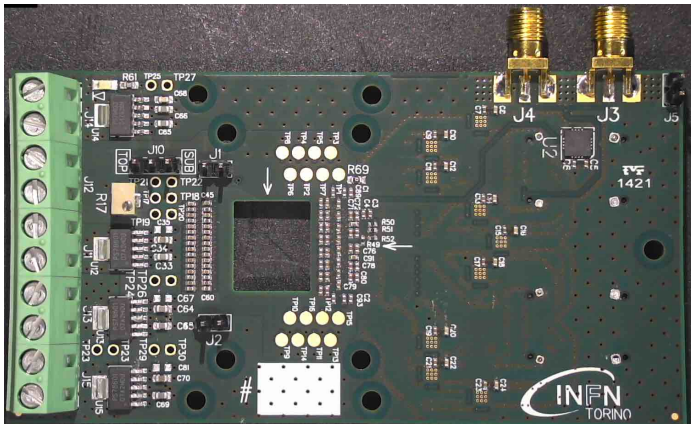
IPbus write
IPbus read
IPbus read_block

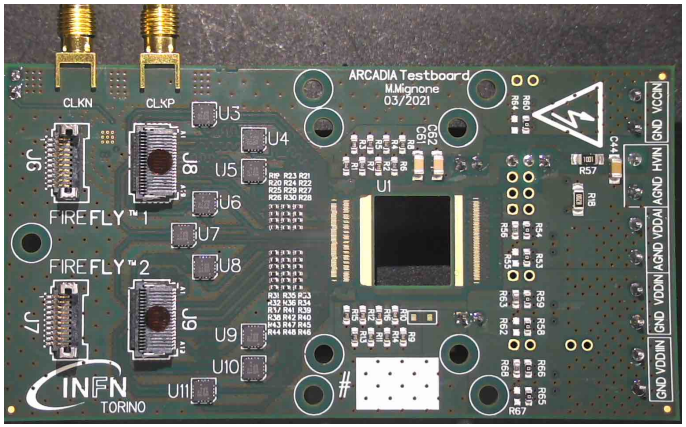


ARCADIA- MD1
(3 chips)

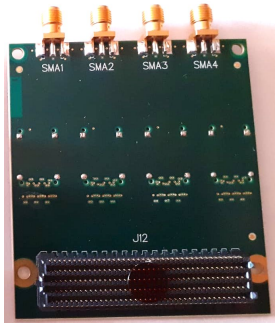


Front-End and Breakout Boards

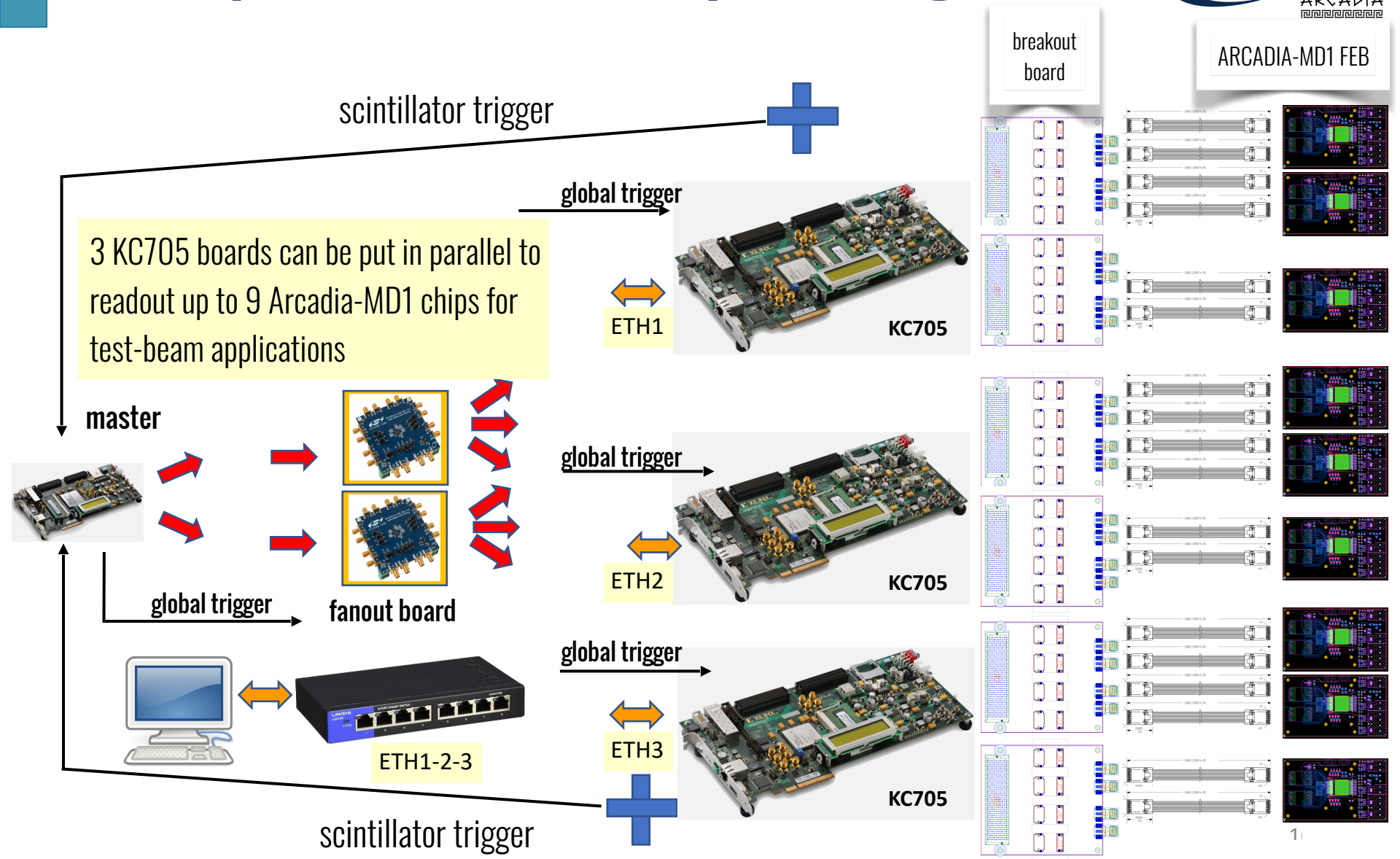




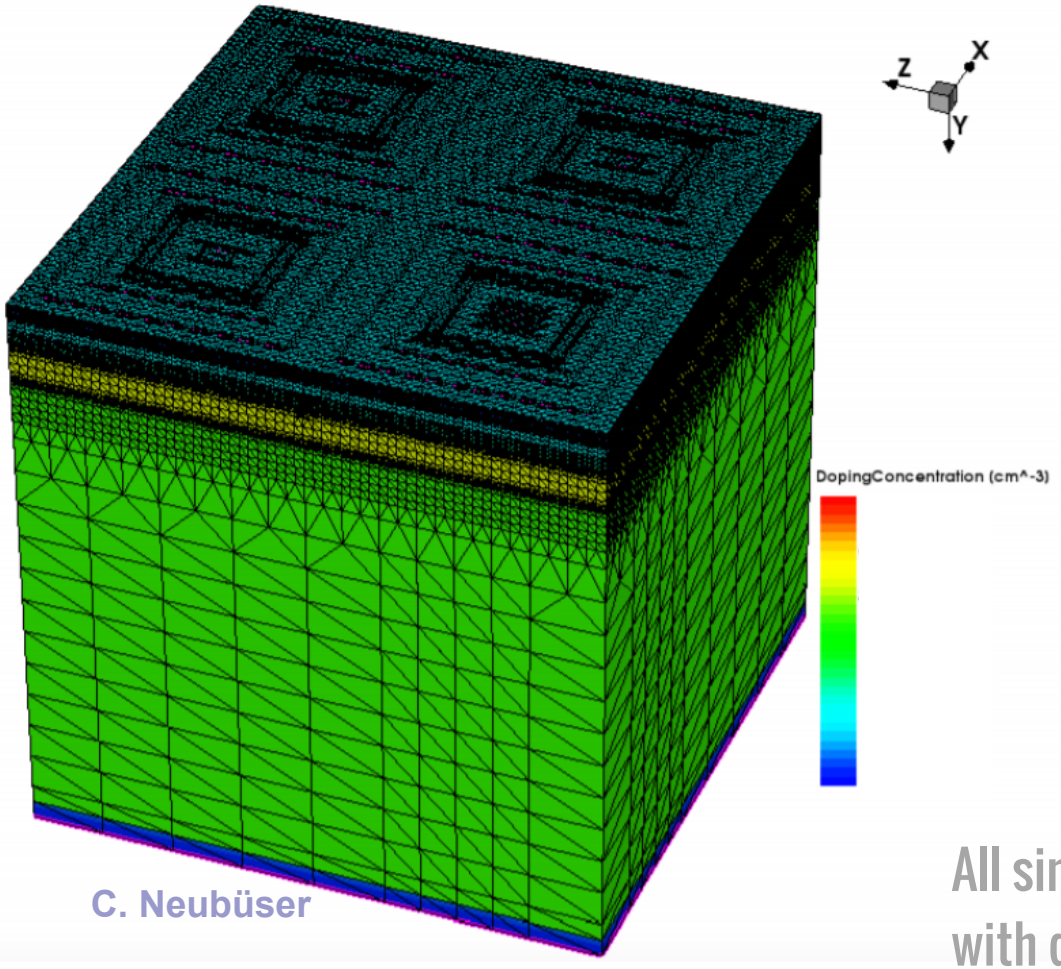
- 2 Samtec FireFly connectors for ASIC signals (Clock, SPI, Data)
- Possibility to use both an external low jitter Clock (via SMA connectors) or the clock provided by the FPGA
- Possibility to connect the high voltage on the DMAPS substrate or via the (wire bonded) pads on top
- Independent voltage regulators for the regional domains on-chip (IO Buffers, Analog Core, Digital Core)
- PCB through-hole for matrix BSI
- custom FMC-to-Firefly breakout board



Multi-plane MD1 Telescope Configuration



Sensor Optimisation: Design

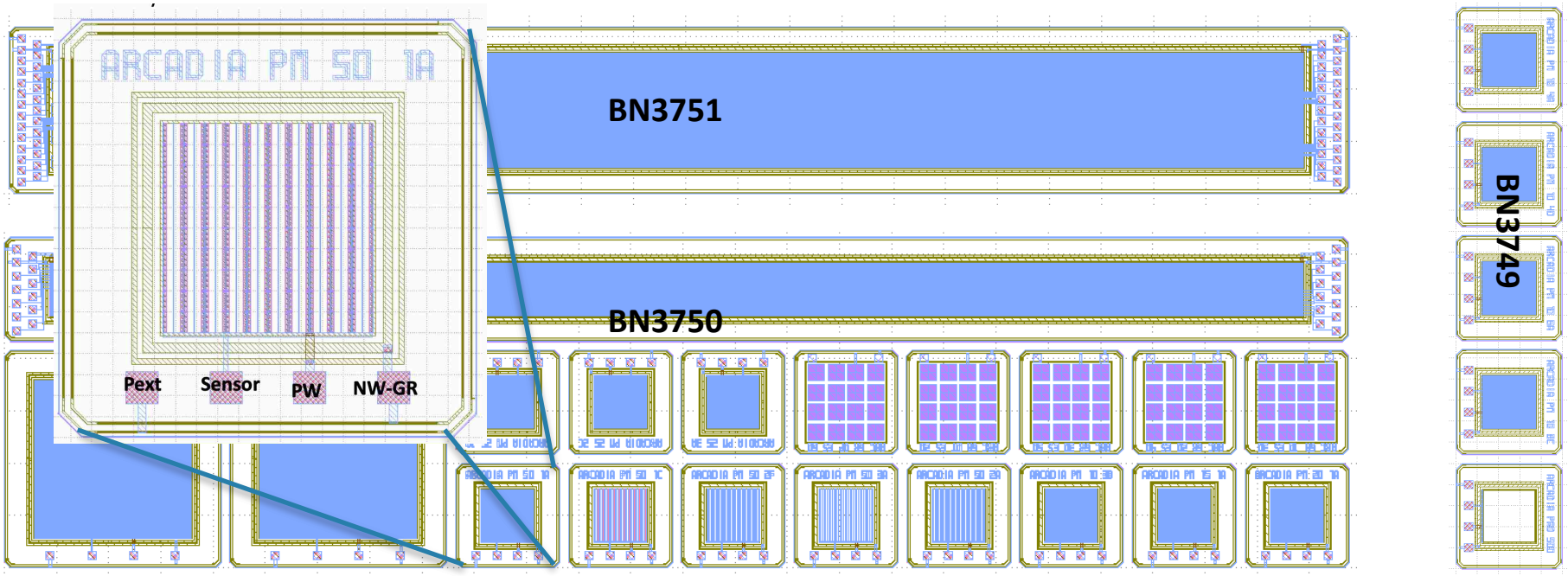


TCAD simulations:

- Operation voltage range
- Sensor capacitance
- Charge collection dynamics
- Charge sharing
- Radiation damage (surface and bulk)

All simulations are repeated for pixels with different pitch, substrate thickness and sensor geometries

Pixel/Strip Test Structures



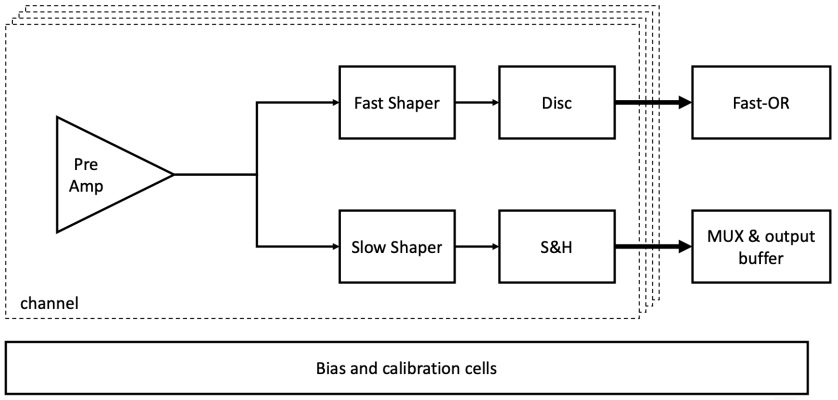
- **strips come in different flavours:**
  - 25 μm pitch pixelated + 25 μm continuous (10+10) [2 variants]
  - 10 μm pixelated (4 groups of 12 strips connected to pads) [4 variants]

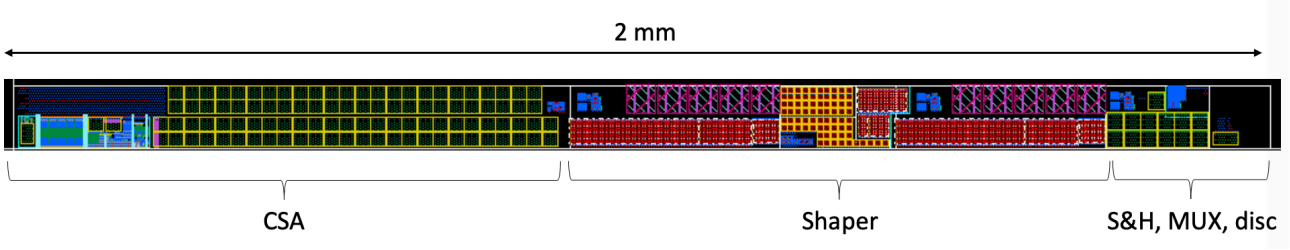
- **and pixels as well:**
  - Pseudo-Matrices of 1x1 and 2x2 mm^2
  - 50 μm (5 variants)
  - 25 μm (3 variants)
  - **10 μm (6 variants)**

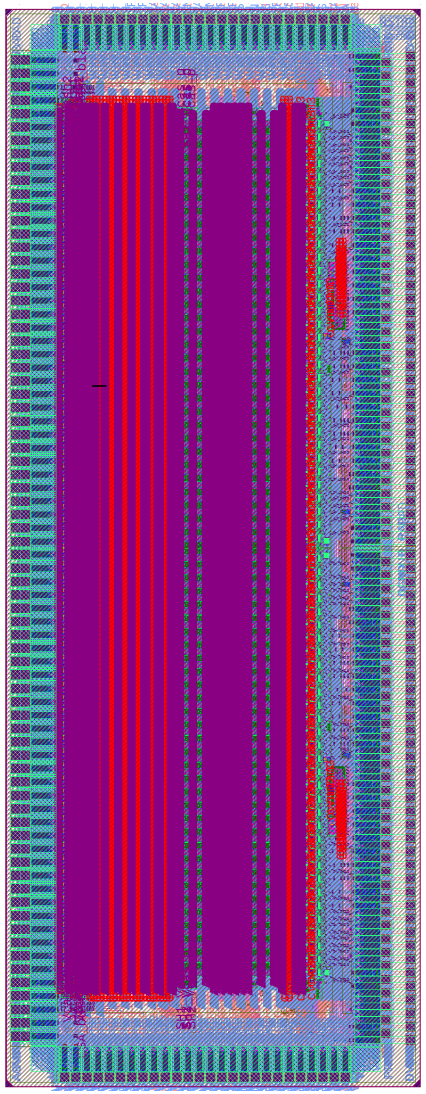
ASIC for Si-Strip readout…

- Chip area=3x3.5mm^2
- 32 channels (100 µm pitch), layout with scalability to 64 channels (and 50 µm pitch)
- Front-End compatible for both polarities
- Programmable peaking time (1.5-8.5 µs)
- Configurable gain to make it suitable for different sensors topologies (i.e. 150-300 µm thickness sensors)
- ENC = 800 e- @ C_{in} = 100 pF and T_p = 6.5µs
- Power consumption < 0.6 mW/ch

Figures:
(mid) architecture and
(bot) layout of the channel;
(right) CAD layout of the 64-channel embodiment







…and embedded Si-strip and readout

- Design and Production of continuous and “pixelised” strips, range 10 - 100µm pitch
- Proof-of-concept: **CMOS monolithic strip block and readout electronics**

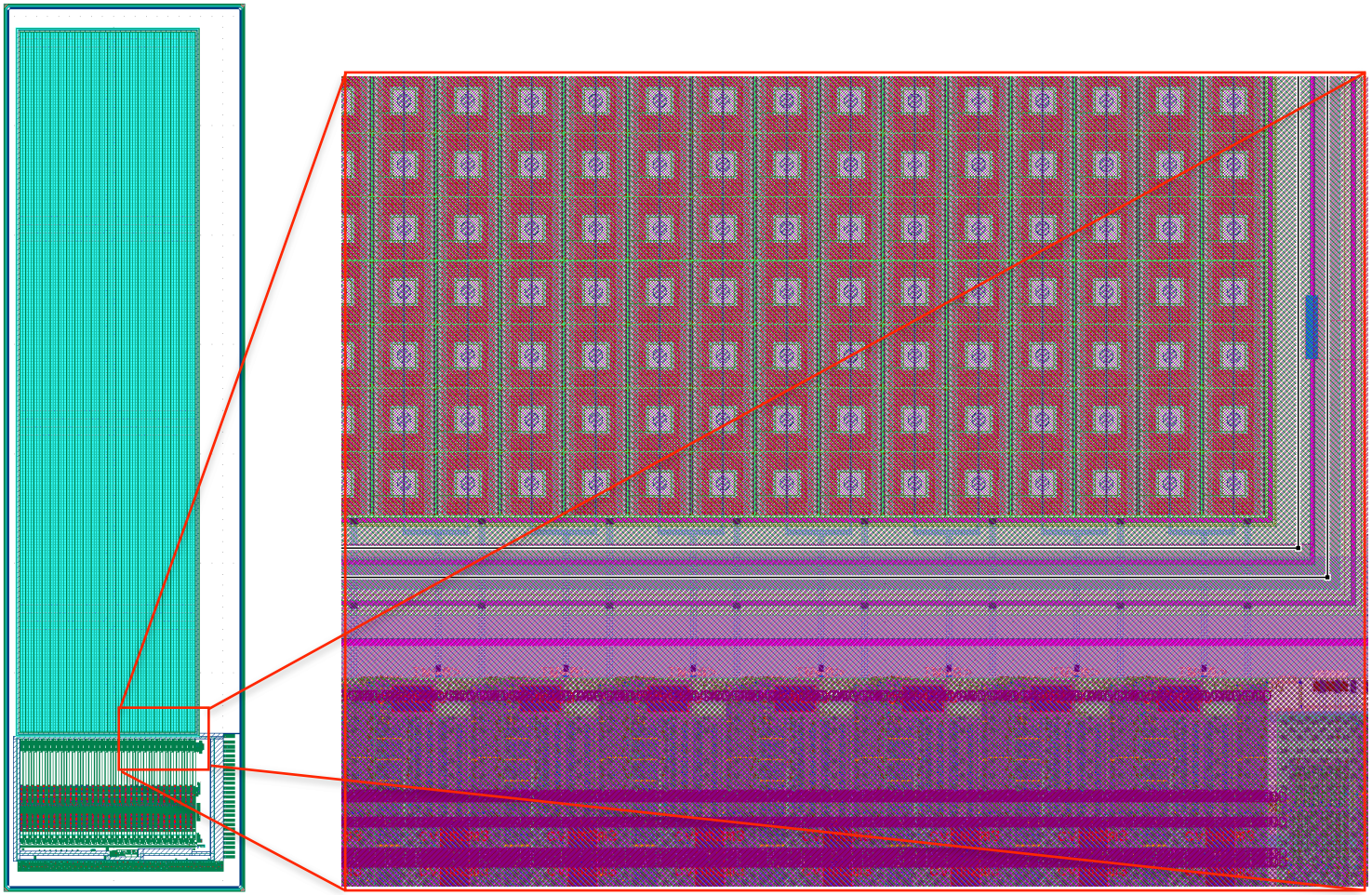


Figure: CAD Layout of 2x32x50µm pixelised strips

Figure: (top) detail of 2x32x50µm pixelised strips and (bottom) 32-channel custom readout

Getting ready for silicon

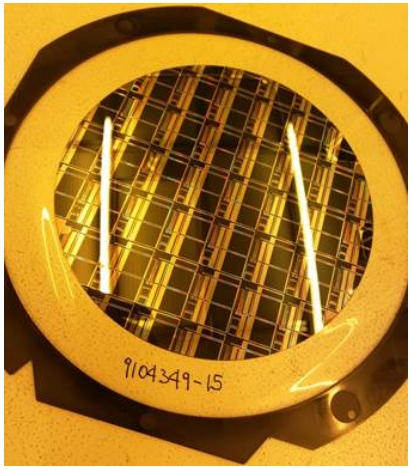
- **Measurements on bonded test structures (first non-irradiated and then irradiated with x-rays and neutrons), front-side and back side**
  - IV curves with temperature, extraction of depletion, punch-through voltages, dark current and capacitance
  - Charge collection with focused pulsed laser (back-side). On pixels: only signal evolution with time and position of the laser spot. On strips: charge sharing is also possible.
  - Lab. sources. (top-side and back-side)

- **Characterisation of the ARCADIA-MD1**
  - functional and electrical characterisation (basic functionalities with on-chip test pulse and hit injection, s-curves, threshold calibration, rate assessment)
  - laser scans with red and IR light (CCE vs bias voltage, uniformity, clustering and resolution)
  - tests with x-ray and radioactive sources (55Fe, 241Am, 90Sr)
  - cosmic ray stand (sync and event building, efficiency, resolution) and beam tests with MD1 telescopes

ARCADIA: status and plans in a nutshell

- **ARCADIA** has now secured a total budget of 1.4 M€ with several groups working on:
  - Sensor R&D and Technology
  - CMOS IP Design and Chip Integration
  - Data Acquisition for electrical characterisation and beam tests with multi-chip telescopes
  - Radiation Hardness qualification
  - System-level characterisation for Medical (pCT), Future Leptonic Colliders and Space Instruments

- **Schedule for 2021-2022**
  - all hardware and firmware ready for testing, first silicon just delivered
  - 1st SPW run included 800 mm2 of innovative DMAPS, sensor and CMOS technology (first tests on sensors are ok, wafers currently being diced)
  - 2nd run mid-2021: sent to foundry, 3rd run planned for mid-2022;



Thank you for listening!