Система сбора данных на основе SoC-FPGA для координатных кремниевых детекторов

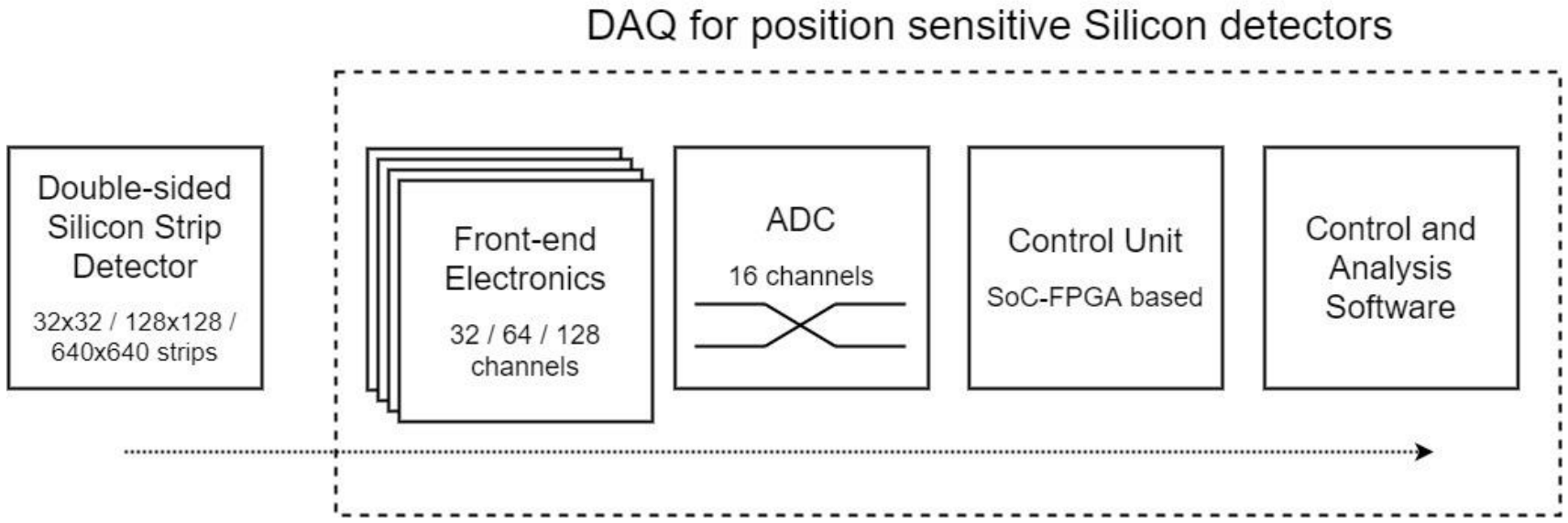
The SoC-FPGA based Data Acquisition System for position sensitive Silicon detectors

Yu. Topko, B. Topko, S. Khabarov, N. Zamyatin

The SoC-FPGA based DAQ system for position sensitive Silicon detectors

Front-end Electronics for Double-sided Silicon Strip Detector systems

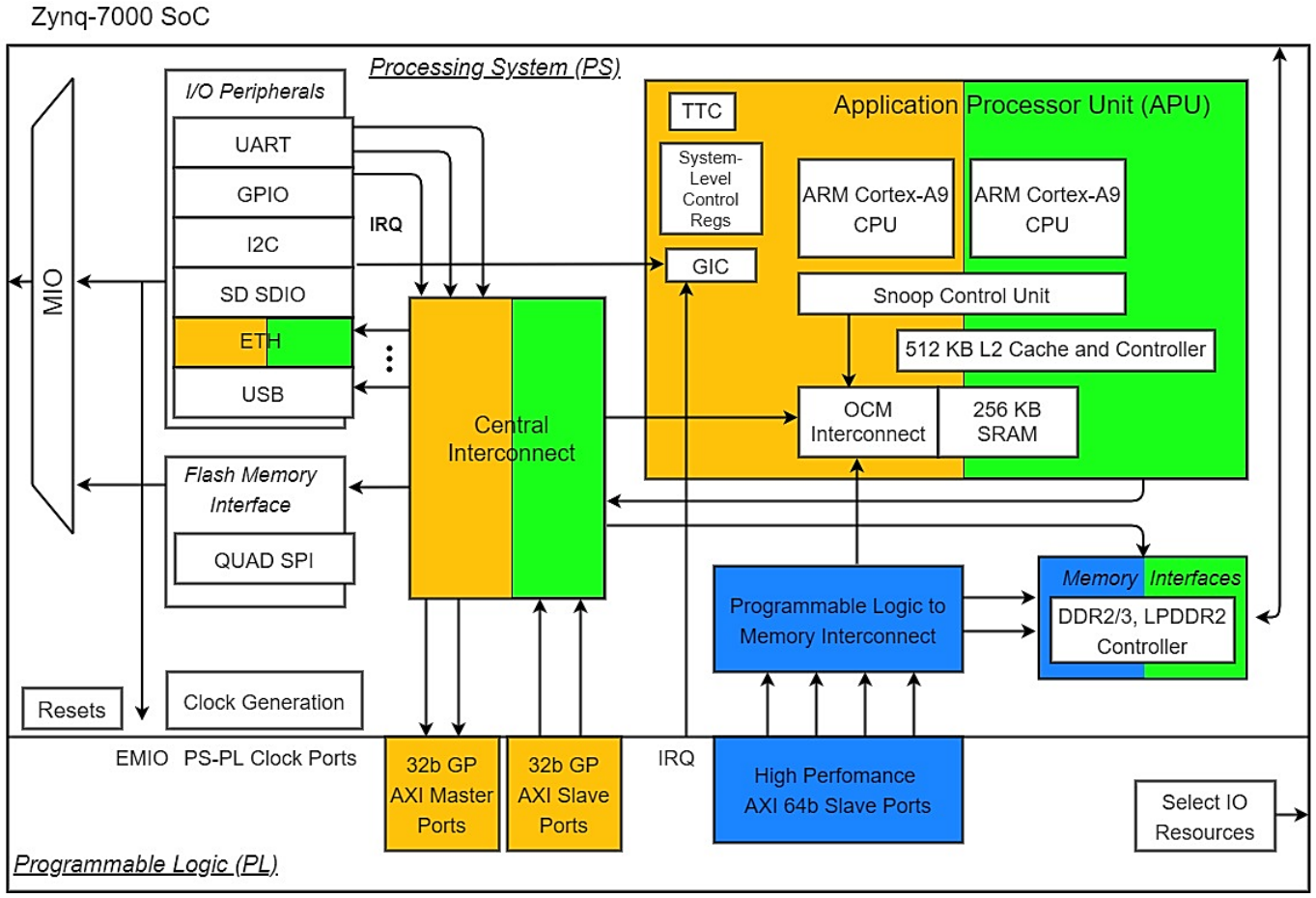
DSSD system	Number of detector strips	IDEAS ASIC	Dynamic range	Number of ASIC channels	Self-triggered
Silicon beam profilometer	32x32	VA163, TA32cg2	-750 ÷ +750 fC	32	yes
Silicon beam tracker	128x128	VATA64HDR16	-20 ÷ +55 pC	64	yes
Silicon module	640x640	VATAGP7.1	-30 ÷ +30 fC	128	no



Control Unit. Processing System

The Control Unit is an autonomous, portable module based on the MicroZed development board equipped with the Xilinx Zynq-7000 SoC: integrated dual-core ARM Cortex-A9 based Processing System (PS) and Xilinx Programmable Logic (PL) in a single device.

The Processing System provides a connection to the Control and Analysis Software via Ethernet interface for data flow transmission and control words receiving.

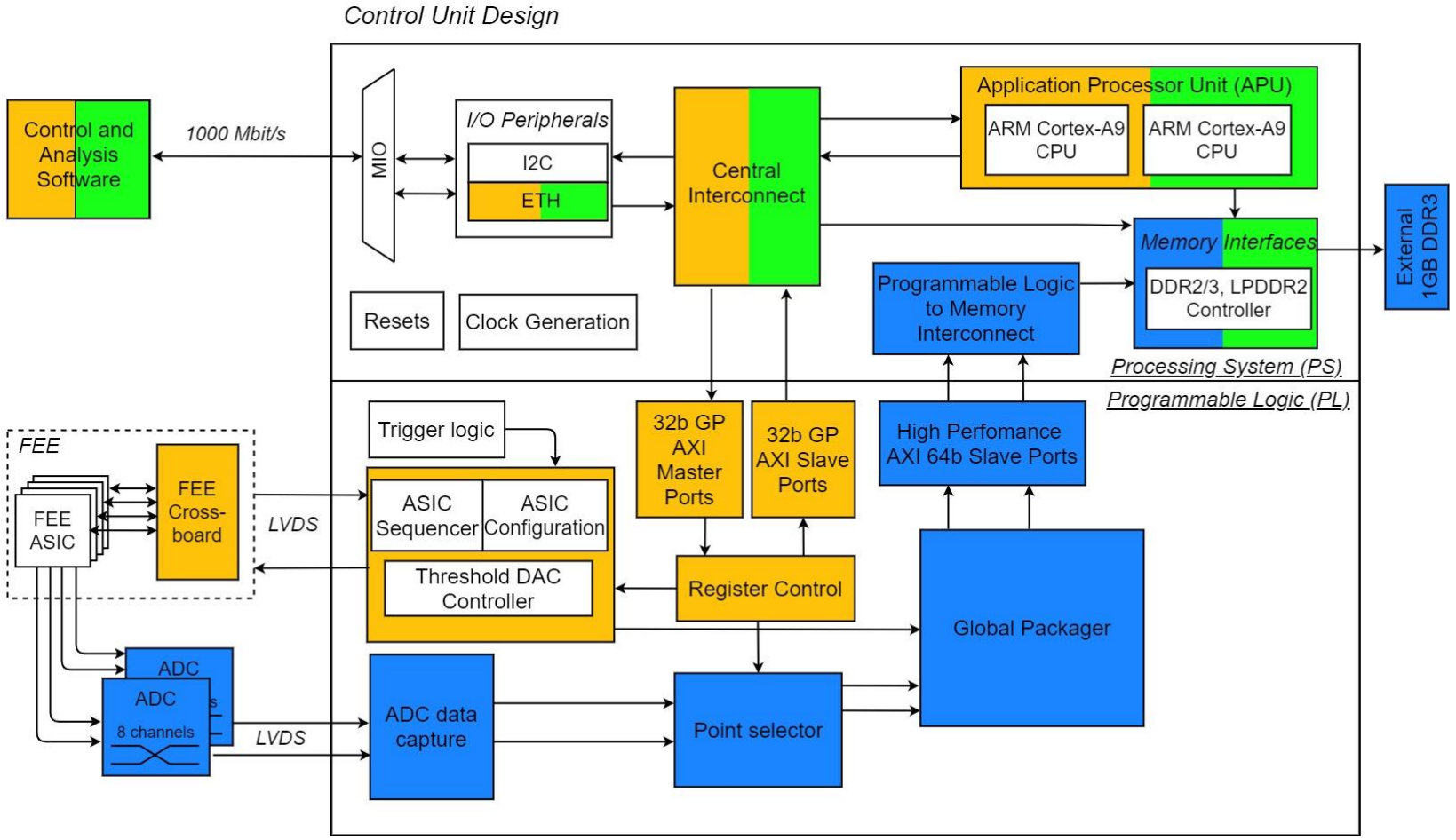


The yellow blocks represent the datapath of control words receiving, the green blocks – data flow transmission, the blue blocks – FEE data storing.

Control Unit. Programmable Logic

The Control Unit PL part functions

- set internal ASIC configuration bits;
- send the readout diagram by trigger in four trigger modes;
- simultaneously pack ADC data from all 16 channels;
- transmit packed data to the external DDR.



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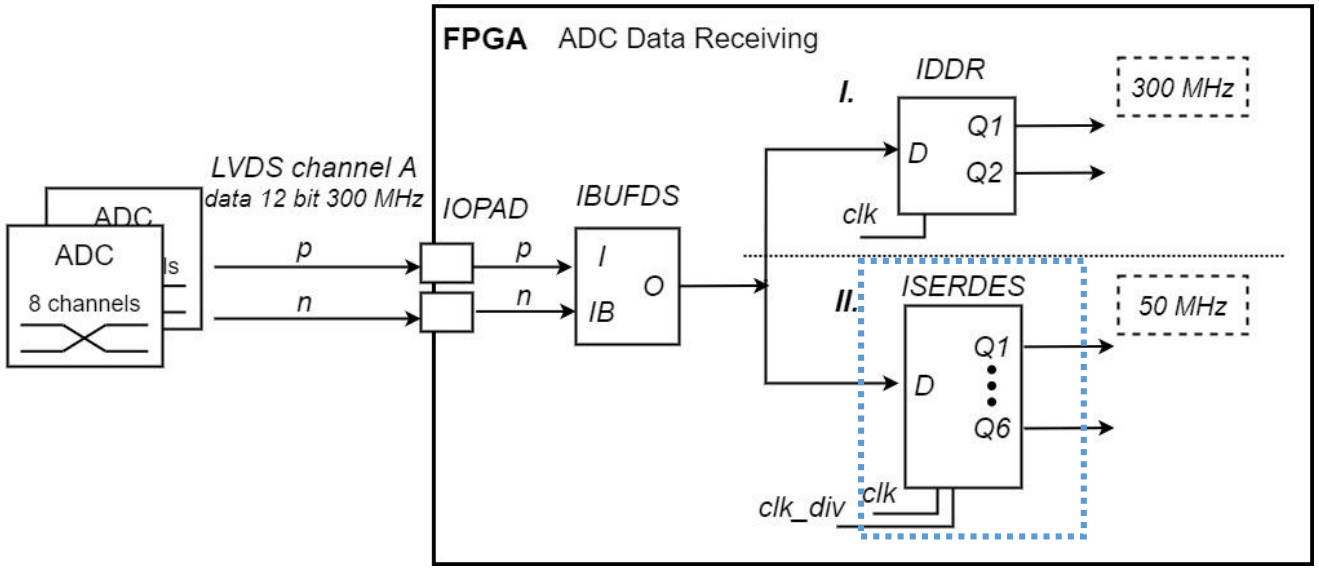
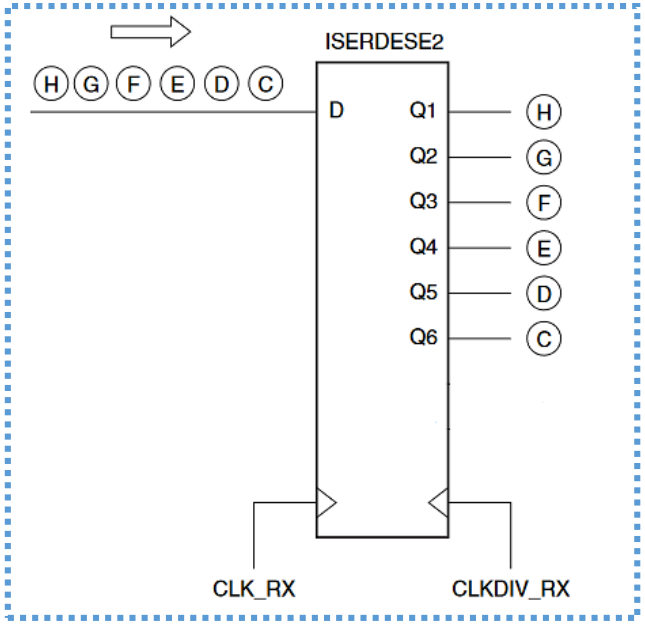
ADC data receiving





I.

The bandwidth with packed IDDR output:

$$B = \frac{IDDR\ output \cdot 8\ ADC\ channels + FCO\ bit}{8\ bit} \cdot clock\ rate =$$

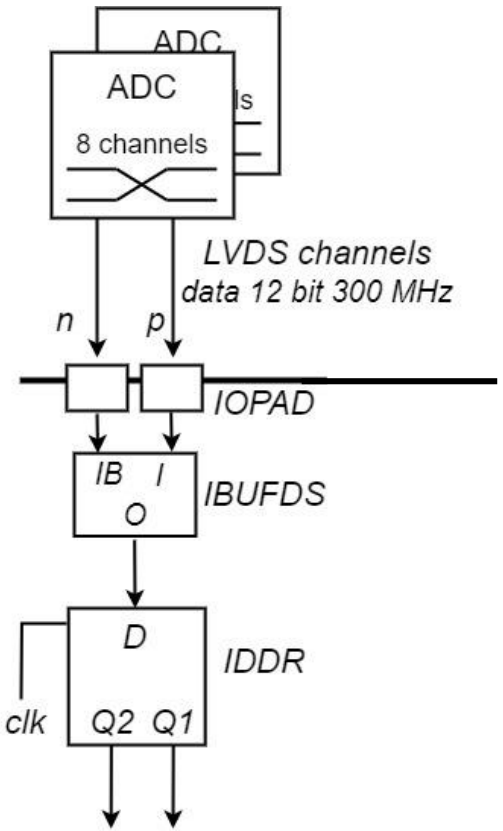
$$= \frac{(2 \cdot 8 + 1) bit}{8\ bit} \cdot 300\ MHz = \underline{\underline{637.5\ MB/s}}$$

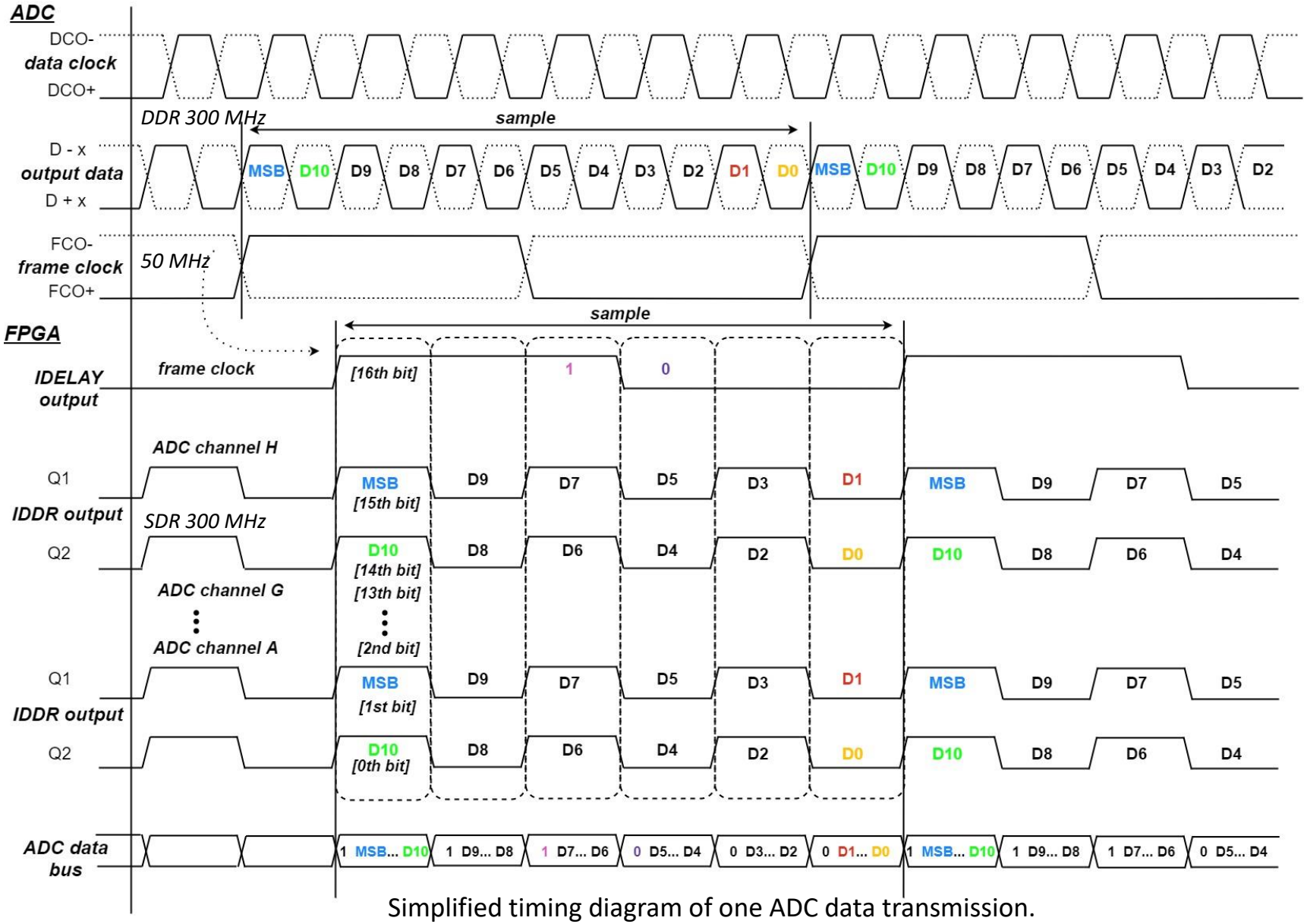
II.

The bandwidth with ISERDES primitive implementation:

$$B = \frac{ADC\ word\ width}{8\ bit} \cdot clock\ rate = \frac{12\ bit}{8\ bit} \cdot 50\ MHz = \underline{75\ MB/s}$$

ADC data transmission and improved bandwidth





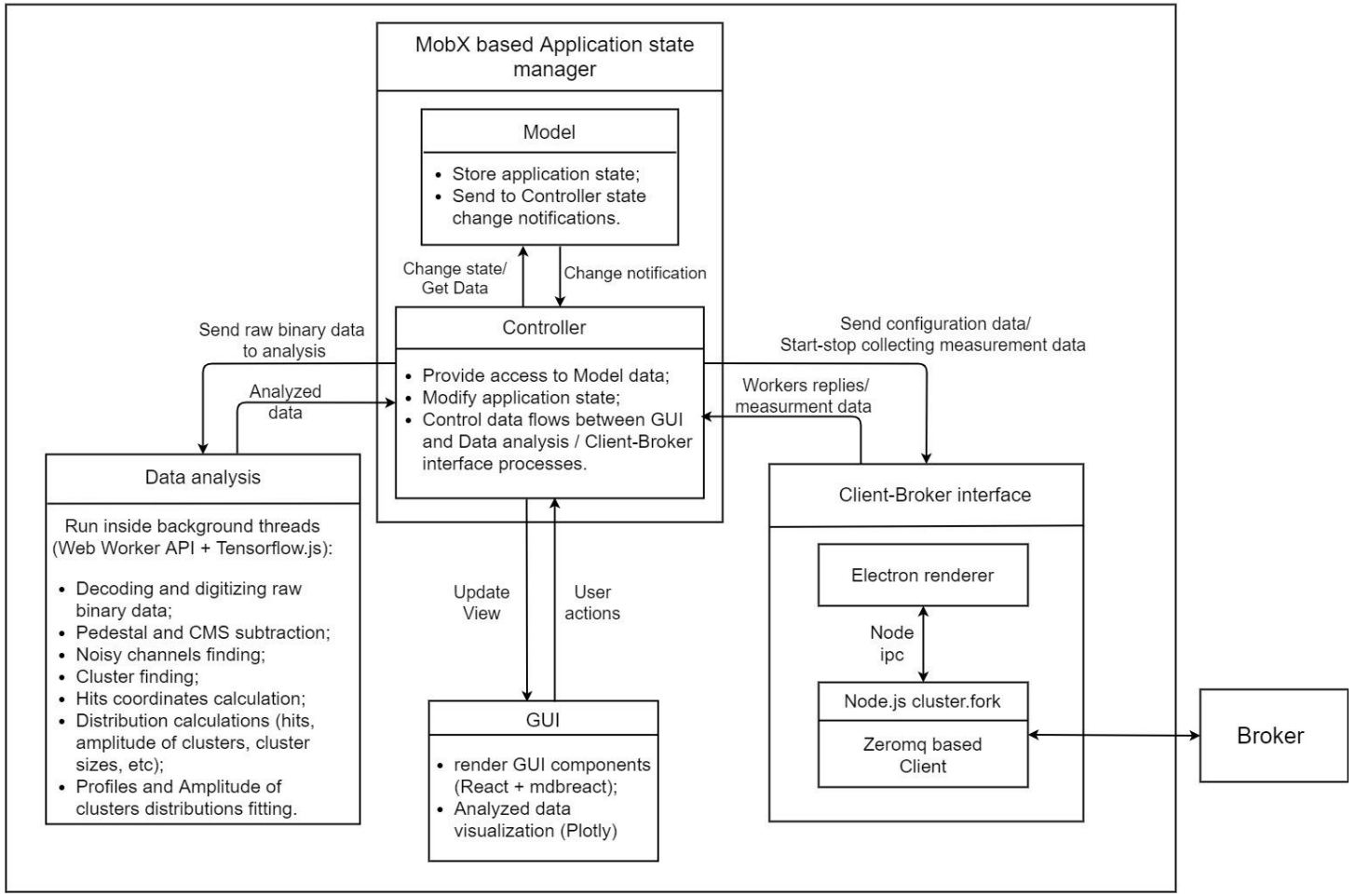
Simplified timing diagram of one ADC data transmission.

Control and Analysis Software

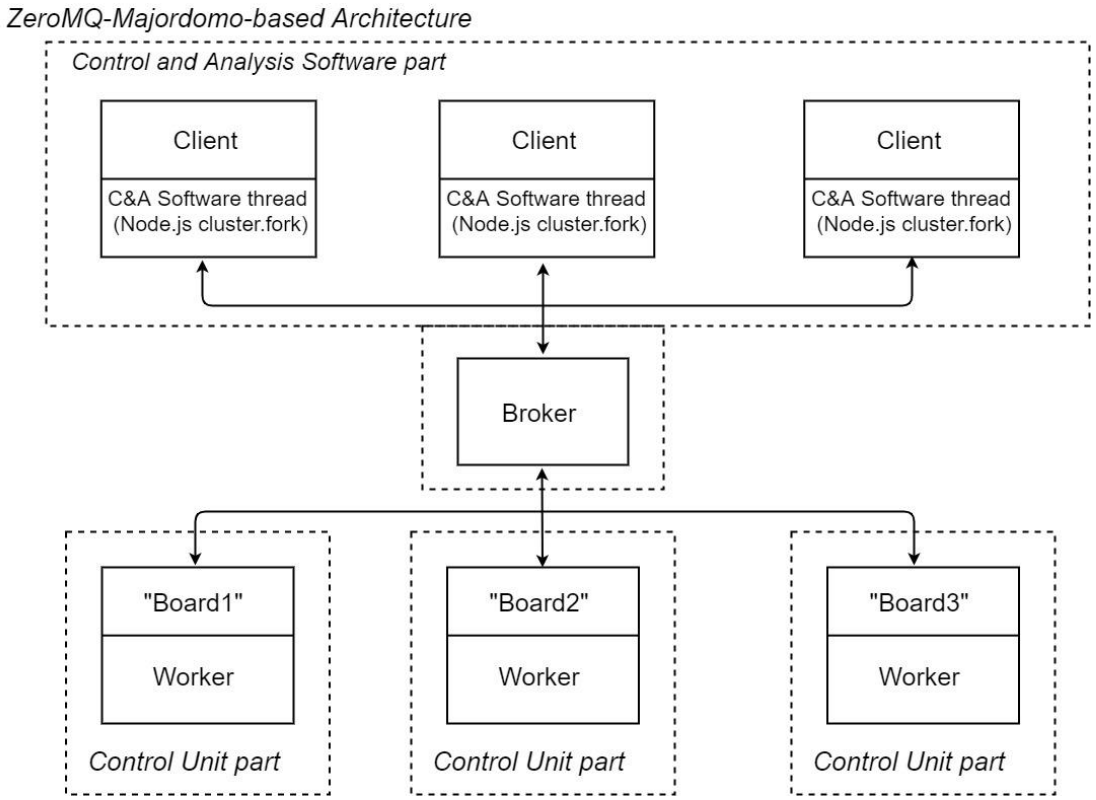
Control and Analysis Software functions:

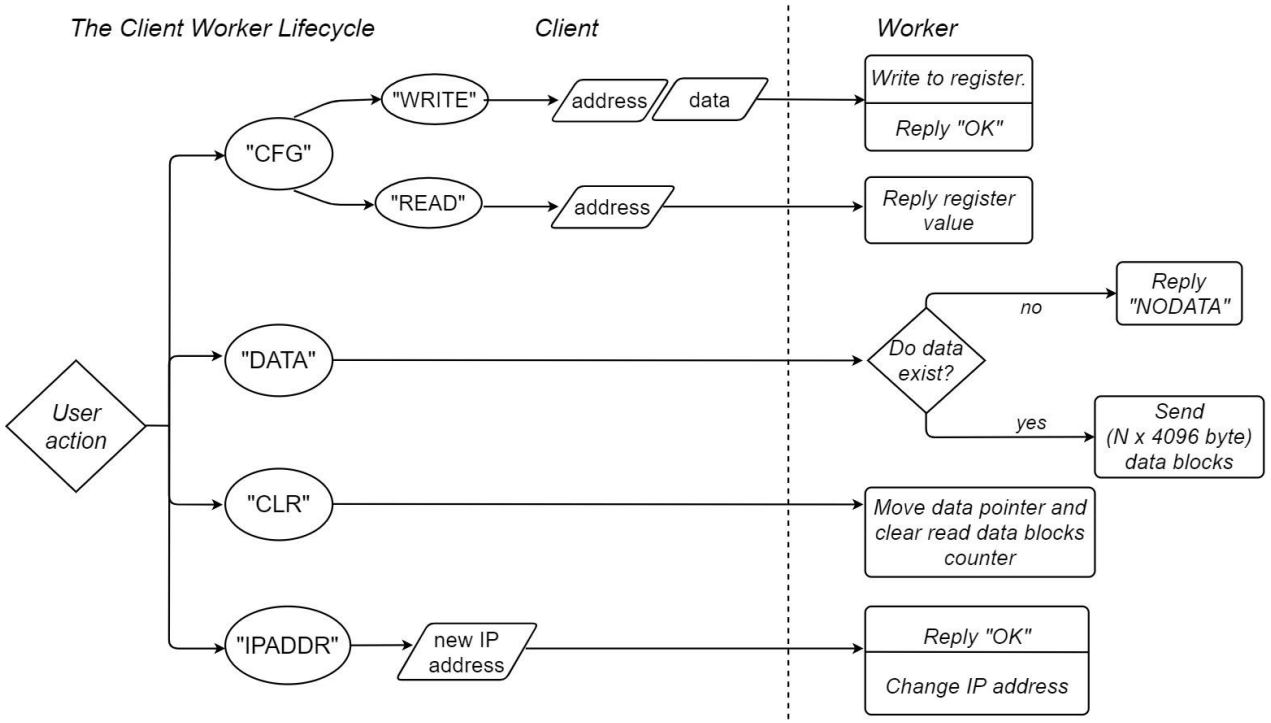
- a network connection to the Control Unit;
- FEE ASICs configuration;
- decoding and digitizing raw binary data;
- pedestal and common-mode shift (CMS) subtractions;
- noisy channels finding;
- cluster finding;
- hits coordinates calculation;
- distribution calculations (hits, amplitude of clusters, cluster sizes etc.);
- Profiles and Amplitude of cluster distributions fitting.

Electron-based Control and Analysis software



Scalable architecture



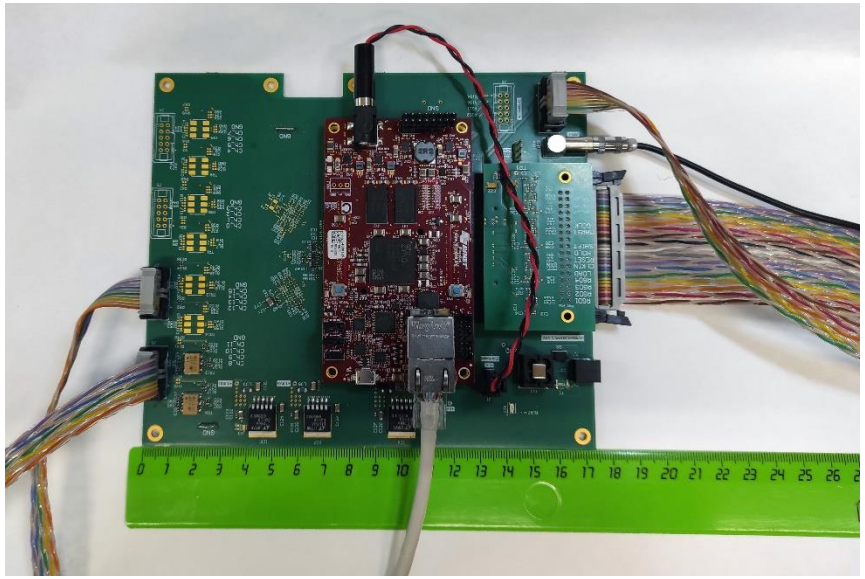


- "CFG" means configuration and divides into two branches to write ("WRITE") and read ("READ") registers on the Control Unit PL side;
- "DATA" is used to obtain measurement data. The Worker asynchronously sends a number of 4 Kb data blocks or replies a "NODATA" control word.
- "CLR" clears previously written to DDR3 data blocks by moving data pointer;
- "IPADDR" is a control word to change the Control Unit board IP address.

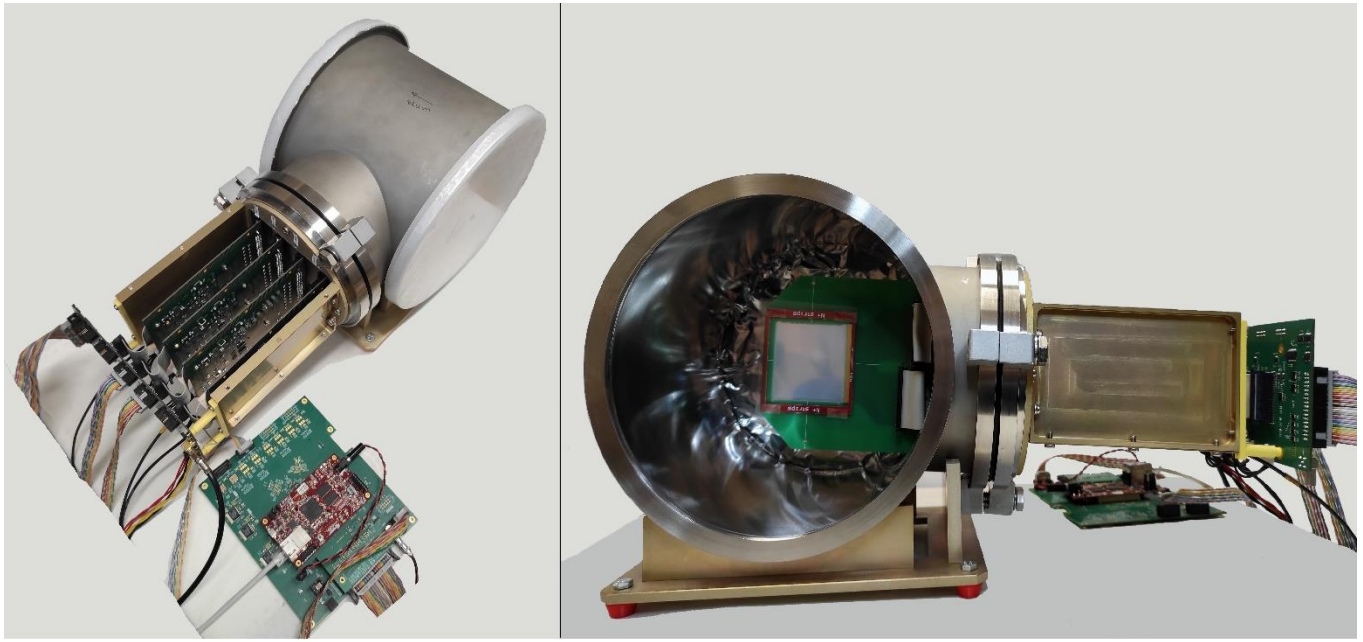
The SoC-FPGA based DAQ system for Silicon beam tracker

DSSD is located inside the vacuum station flange and has the following parameters:

- 61 mm x 61 mm active area;
- 470 µm p+/n+ sides strips pitch;
- 175 µm thickness;
- 90^{o} stereo angle between strips.



The autonomous, portable Control Unit Carried Board based on the MicroZed development board and ADCs with essential connections to FEE cross-board.



(a) (b)

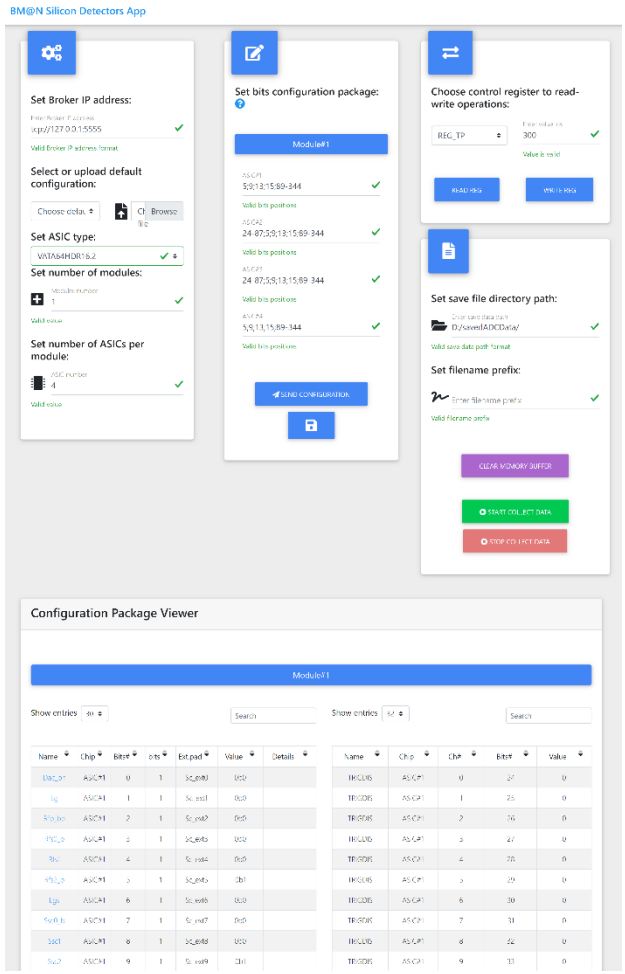
The SoC-FPGA based DAQ system for Silicon beam tracker (left) and the opened flange with DSSD inside (right).

Test results for Silicon beam tracker

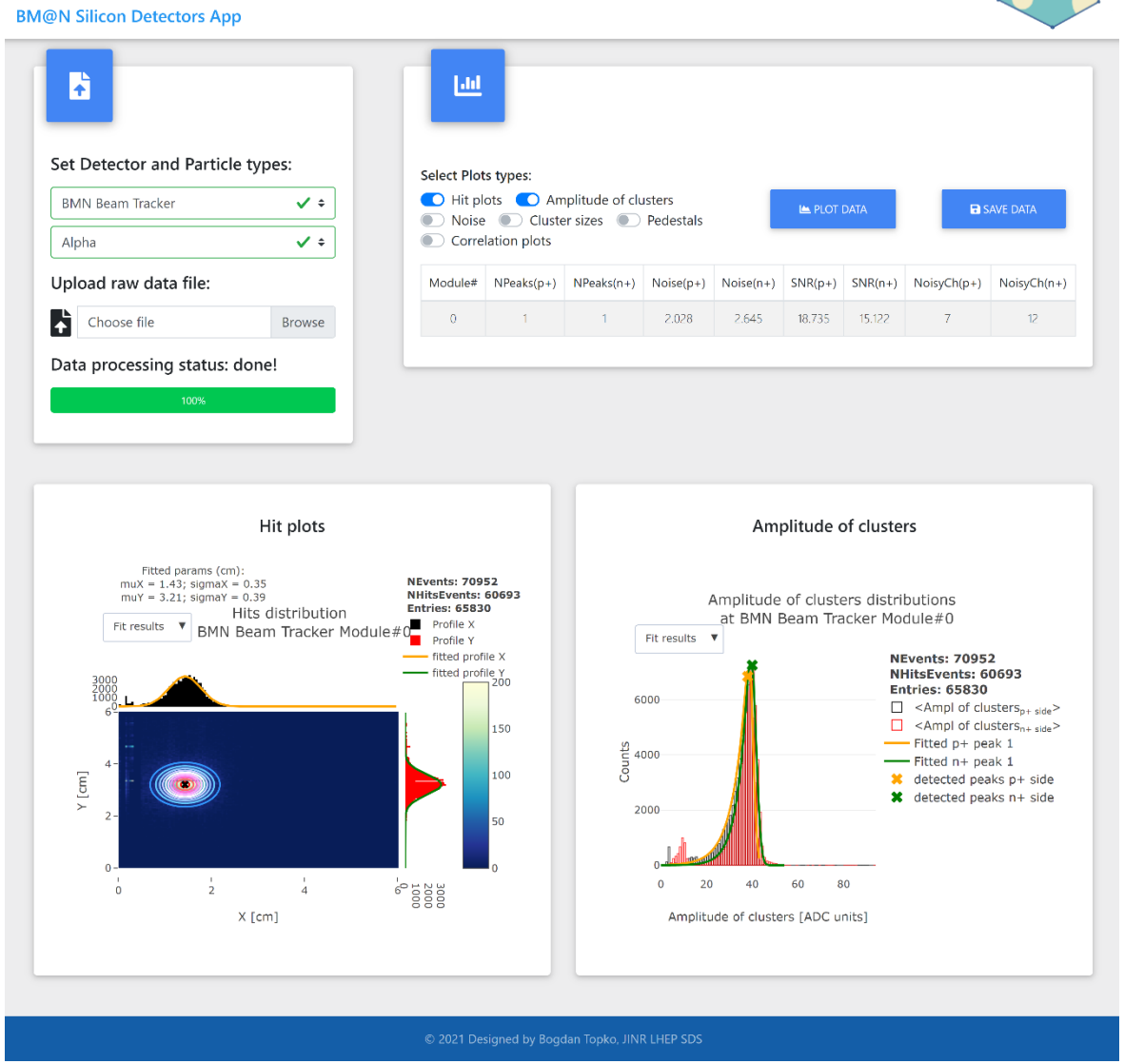
Particle	Energy	Charge	ADC units
Alpha	5.499 MeV	244 fC	40
Carbon	4 AGeV	96 fC	16
Gold	4 AGeV	18 pC	1475

Profile center coordinates are X = 1.43 cm and Y = 3.21 cm with standard deviations σ_X= 0.35 cm and σ_Y= 0.39 cm.

The alpha spectrum peak positions are automatically found with values 38 and 40 ADC units



the FEE configurations in the Control and Analysis Software



Alpha source (^{238}Pu) measurement visualization in the Control and Analysis Software

Conclusions

- the DAQ system for position sensitive Silicon detectors is composed of the FEE cross-board, FEE cards with wire bonded and encapsulated multichannel IDEAS ASICs, the SoC-FPGA based Control Unit Carried Board equipped with two 8 channels ADCs, and the multithreading user-friendly Control and Analysis Software;
- the autonomous DAQ system was designed for Silicon beam profilometer, Silicon beam tracker and Silicon modules test benches;
- and tested with alpha source for Silicon beam tracker;
- the SoC-FPGA based DAQ system could be used for position sensitive Silicon detectors to measure a wide range of ultra-relativistic ion coordinates at the BM@N experiment;
- the portable DAQ system could be adjusted for other beam position measurement goals.