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## Система сбора данных на основе SoC-FPGA для координатных кремниевых детекторов

# The SoC-FPGA based Data Acquisition System for position sensitive Silicon detectors

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#### The SoC-FPGA based DAQ system for position sensitive Silicon detectors



#### Front-end Electronics for Double-sided Silicon Strip Detector systems

DSSD system	Number of detector strips	IDEAS ASIC	Dynamic range	Number of ASIC channels	Self-triggered
Silicon beam profilometer	32x32	VA163, TA32cg2	-750 ÷ +750 fC	32	yes
Silicon beam tracker	128x128	VATA64HDR16	-20 ÷ +55 pC	64	yes
Silicon module	640x640	VATAGP7.1	-30 ÷ +30 fC	128	no

#### DAQ for position sensitive Silicon detectors







#### Control Unit. Processing System



The Control Unit is an autonomous, portable module based on the MicroZed development board equipped with the Xilinx Zynq-7000 SoC: integrated dual-core ARM Cortex-A9 based Processing System (PS) and Xilinx Programmable Logic (PL) in a single device.

The Processing System provides a connection to the Control and Analysis Software via Ethernet interface for data flow transmission and control words receiving.



The yellow blocks represent the datapath of control words receiving, the green blocks – data flow transmission, the blue blocks – FEE data storing.





## Control Unit. Programmable Logic



The Control Unit PL part functions

- set internal ASIC configuration bits;
- send the readout diagram by trigger in four trigger modes;
- simultaneously pack ADC data from all 16 channels;
- transmit packed data to the external DDR.



The yellow blocks represent the datapath of control words receiving, the green blocks – data flow transmission, the blue blocks – FEE data storing.









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The bandwidth with packed IDDR output:

$$B = \frac{IDDR \ output \cdot 8 \ ADC \ channels + FCO \ bit}{8 \ bit} \cdot clock \ rate =$$
$$= \frac{(2 \cdot 8 + 1)bit}{8 \ bit} \cdot 300 \ MHz = \underline{637.5 \ MB/s}$$

**ISERDESE2** HGFEDCD  $(\mathbf{H})$ Q1 G Q2 F Q3 E Q4 D Q5 C Q6 CLK RX CLKDIV RX

*II.* 

The bandwidth with ISERDES primitive implementation:

$$B = \frac{ADC \text{ word width}}{8 \text{ bit}} \cdot \text{clock rate} = \frac{12 \text{ bit}}{8 \text{ bit}} \cdot 50 \text{ MHz} = \frac{75 \text{ MB/s}}{25 \text{ MHz}}$$





## ADC data transmission and improved bandwidth

BM@N



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D5

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D4

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MSB

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D7 \

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**D**8

D9

**D**8

1 D9... D8

D7

D6

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D6 D5





## Control and Analysis Software



#### Electron-based Control and Analysis software

MobX based Application state manager Model Store application state; · Send to Controller state change notifications. Change state/ Change notification Get Data Send configuration data/ Controller Send raw binary data Start-stop collecting measurement data to analysis Provide access to Model data; Workers replies/ Analyzed Modify application state; measurment data data Control data flows between GUI and Data analysis / Client-Broker interface processes. Data analysis Client-Broker interface Run inside background threads (Web Worker API + Tensorflow.is): Electron renderer Decoding and digitizing raw Update User binary data; View actions · Pedestal and CMS subtraction; Node · Noisy channels finding; ipc · Cluster findina: · Hits coordinates calculation: Node.is cluster.fork GUI Distribution calculations (hits, Broker amplitude of clusters, cluster Zeromg based render GUI components sizes, etc); Client · Profiles and Amplitude of (React + mdbreact); clusters distributions fitting. Analyzed data visualization (Plotly)

Control and Analysis Software functions:

- a network connection to the Control Unit;
- FEE ASICs configuration;
- decoding and digitizing raw binary data;
- pedestal and common-mode shift (CMS) subtractions;
- noisy channels finding;
- cluster finding;
- hits coordinates calculation;
- distribution calculations (hits, amplitude of clusters, cluster sizes etc.);
- Profiles and Amplitude of cluster distributions fitting.





#### Scalable architecture





- "CFG" means configuration and divides into two branches to write ("WRITE") and read ("READ") registers on the Control Unit PL side;
- "DATA" is used to obtain measurement data. The Worker asynchronously sends a number of 4 Kb data blocks or replies a "NODATA" control word.
- "CLR" clears previously written to DDR3 data blocks by moving data pointer;
- "IPADDR" is a control word to change the Control Unit board IP address.



The SoC-FPGA based DAQ system for Silicon beam tracker

BM@N



DSSD is located inside the vacuum station flange and has the following parameters:

- 61 mm x 61 mm active area;
- 470 μm p+/n+ sides strips pitch;
- 175 µm thickness;
- 90° stereo angle between strips.



The autonomous, portable Control Unit Carried Board based on the MicroZed development board and ADCs with essential connections to FEE cross-board.



(a)

(b)

The SoC-FPGA based DAQ system for Silicon beam tracker (left) and the opened flange with DSSD inside (right).





#### Test results for Silicon beam tracker



Particle	Energy	Charge	ADC units
Alpha	5.499 MeV	244 fC	40
Carbon	4 AGeV	96 fC	16
Gold	4 AGeV	18 pC	1475

Profile center coordinates are X = 1.43 cm and Y = 3.21 cm with standard deviations  $\sigma_X$ = 0.35 cm and  $\sigma_Y$ = 0.39 cm.

The alpha spectrum peak positions are automatically found with values 38 and 40 ADC units

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and Analysis Software

**BM@N Silicon Detectors App** 

#### BM@N Silicon Detectors App

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2021 Designed by Bogdan Topko, JINR LHEP SE

Alpha source (<sup>238</sup>Pu) measurement visualization in the Control and Analysis Software







## Conclusions

- the DAQ system for position sensitive Silicon detectors is composed of the FEE cross-board, FEE cards with wire bonded and encapsulated multichannel IDEAS ASICs, the SoC-FPGA based Control Unit Carried Board equipped with two 8 channels ADCs, and the multithreading user-friendly Control and Analysis Software;
- the autonomous DAQ system was designed for Silicon beam profilometer, Silicon beam tracker and Silicon modules test benches;
- and tested with alpha source for Silicon beam tracker;
- the SoC-FPGA based DAQ system could be used for position sensitive Silicon detectors to measure a wide range of ultra-relativistic ion coordinates at the BM@N experiment;
- the portable DAQ system could be adjusted for other beam position measurement goals.