# STS/MUCH-XYTER v.2 testing and calibration activities at JINR

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## Introduction

We present the architecture, testing procedure and calibration of the STS/MUCH-XYTER2 ASIC (Fig. 1), a full-size 128-channel chip for the Silicon Tracking System based on double-sided silicon micro-strip sensors and GEM modules for Muon Detector at the CBM experiment at FAIR, Germany. This ASIC will be also used as a front-end ASIC for the Silicon Tracking system at BM&N stage 2 experiment at NICA (JINR, Dubna).

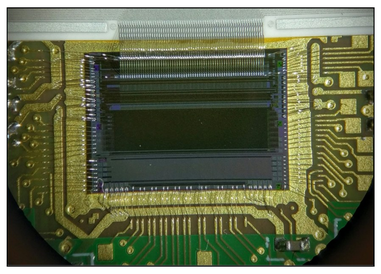

*Fig.1 STSMUCH-XYTER v.2 ASIC*

## Architecture of the ASIC

- Multichannel self-triggered architecture,
- deposited charge time and energy measurements,
- average rate of input pulses 250 kHz/channel,
- input charge range (electrons and holes):
  - ◊ 0.5 fC – 15 fC for the STS mode,
  - ◊ 1 fC – 100 fC for the MUCH mode,
- detector capacitance in the order of tens pF,
- low noise ENC < 1000 e-rms at CDET = 30 pF,
- power consumption < 10 mW/channel,
- radiation-hardness (100-200 kGy in several years of operation),
- 128 (+ 2 test) channels [1].

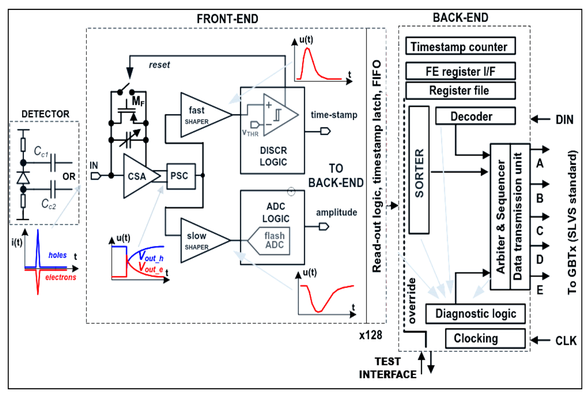


*Fig.2 The simplified architecture of the 128 channel STSMUCH-XYTER v.2 ASIC*

Each channel of the STS/MUCH-XYTER v.2 ASIC consists of a charge sensitive amplifier and two signal paths with fast and slow shapers: for timing measurement with a fast discriminator and low-noise amplitude measurement by a 5-bit continuous-time ADC with digital peak detector (Fig. 2). The circuit implements switchable shaper peaking times, gain switching and trimming, pulsed reset of the amplifier for increased input charge rate and faster recovery from overload, fail-safe measures and diagnostic modes for wafer-level and in-system testing and calibration.

The back-end part implements fast channel read-out, timestamp-wise hit sorting and data streaming via scalable interface implementing a dedicated protocol (STS-HCTSP) for chip control and hit transfer with data bandwidth up to 47 MHit/s. It also includes options for link diagnostics, fault detection and throttling features [2].

## Flash ADC

The slow signal path is designed for precise energy measurement and includes a slow shaping amplifier, a flash ADC and a digital peak detector (Fig. 3).

Flash ADC is controlled by three global reference circuits: biasing, minimum threshold and maximum threshold, which are common to all channels (Fig. 4). The measurement channel consists of 31 identical comparator cells and a decoder. Each cell consists of a comparator with a memory buffer, an 8-bit trimming DAC and 12-bit counter.

For the measurement system to be reliably calibrated, the whole signal path has to be characterized, to compensate also for the channel-to-channel gain variations and shaping amplifiers nonlinearities. Therefore, the final, calibrated ADC threshold voltages should correspond to certain input signal values, which in this case are charges, expressed in electrons or coulombs [3].

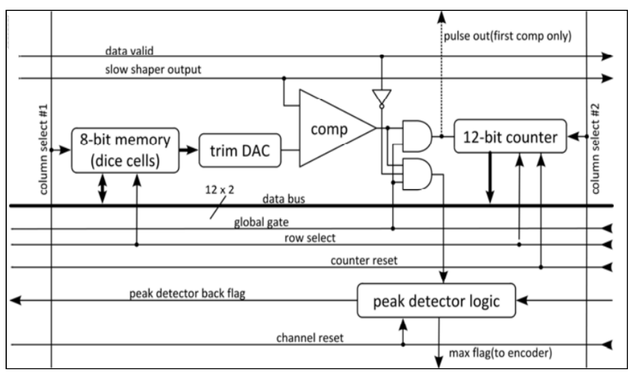


*Fig. 3 Simplified diagram of the digital peak detector cell*

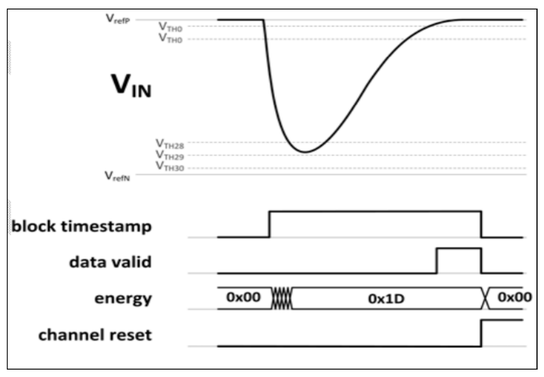


*Fig. 4 Output timing diagram*

## Test bench at JINR

The test setup consists of a PC, an AMC FMC Carrier board (AFCK), a FEB with an STS/MUCH-XYTER2 ASIC, an oscilloscope, a signal generator and a power supply (Fig. 5). AFCK is a µTCA board with a Xilinx Kintex-7 325T FPGA, 2 FMC (HPC) and RTM connectors and Multi-Gigabit Transceivers (MGT).

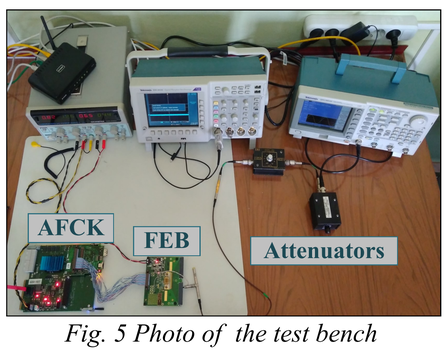


*Fig. 5 Photo of the test bench*

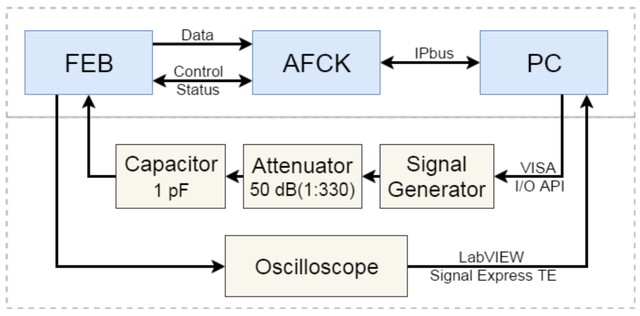


*Fig. 6 Test bench structure*

## Internal charge generator calibration

- Generated charge Qin from 0 to 15 fC,
- resolution 8 bit,
- 4 switched channel groups,
- Generator is connected to channels through 100 fF capacitors,
- can be monitored and overridden via a spy point (ampCAL).

Internal test charge generator (Fig. 7) is represented by a DAC and charge-injecting capacitors at inputs of each channel. DAC full scale and integral nonlinearity have been measured. Thereafter, charge-injecting capacitors will be characterized to evaluate accuracy of the injected charge.

After the INL correction has been made by approximating the inverse transfer curve by a 3rd degree polynomial (Fig. 8)., DAC integral nonlinearity of 1 LSB can be achieved, as opposed to initial 4-5 LSB (depending on the particular ASIC) (Fig. 9).

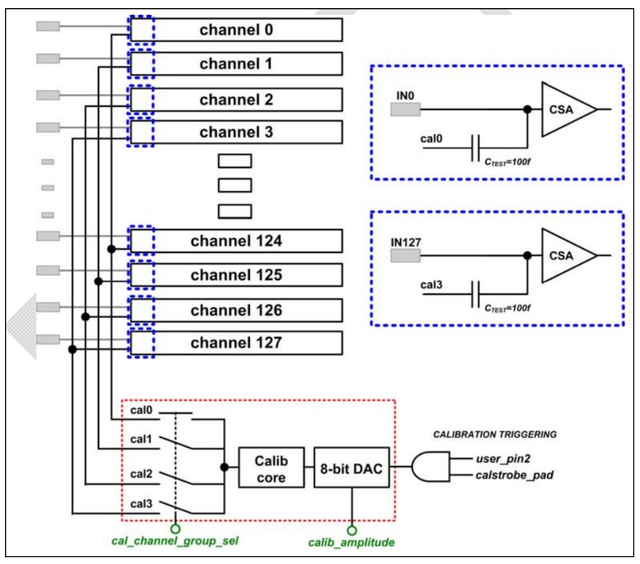


*Fig. 7 Calibration circuit block scheme*

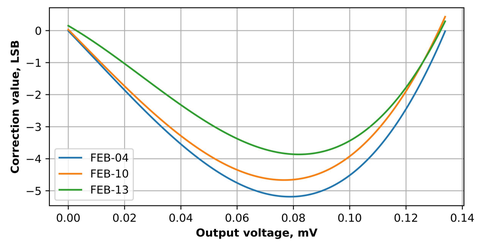


*Fig. 8 Inverse transfer functions for different ASICs*

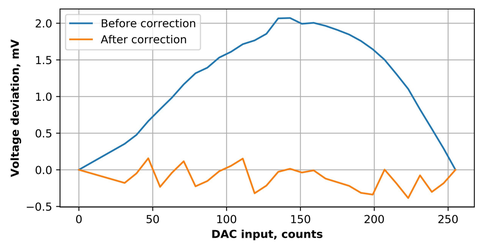


*Fig. 9 INL compensation*

## ADC trim procedure

A technique was developed to determine the individual trimming DAC values required to achieve a pre-defined ADC transfer characteristic. In our case, the uncorrected discriminator thresholds, which exhibit highly non-monotonous behavior, are tuned for linear response over a predefined signal range.

The ADC calibration algorithm implements basically an iterative adjustment of the comparators thresholds (s-curve shape Fig. 10) to certain test signal amplitudes using binary search.

Each comparator on every 4th channel are calibrated simultaneously (within one calibration channel group). This procedure is carried out for each of 31 comparators on 128 channels. The calibration procedure for the ASIC takes approximately 15 minutes and it can be parallelized for multiple chips. Fig. 11 and Fig. 12 demonstrate the results before and after calibration.

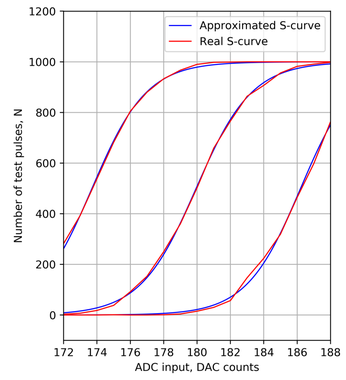


*Fig. 10 Real and approximated comparator S-curves*

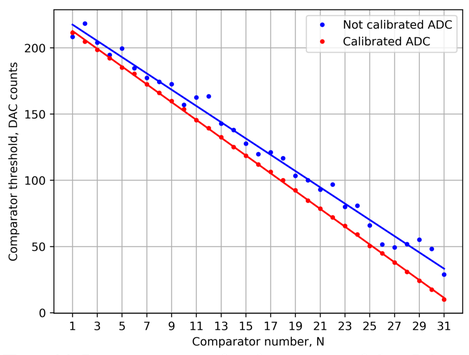


*Fig. 11 Inverse transfer function of the 5-bit flash ADC*

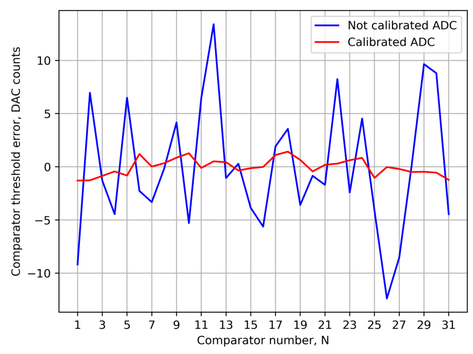


*Fig. 12 Deviation from linearity*

## References

[1] K. Kasinski, W. Zabolotny, R. Szczygiel, W. Zubrzycka, STS/MUCH-XYTER2 Manual v1.29, AGH University of Science and Technology Cracow, 2017.

[2] K. Kasinski, R. Kleczek, R.Szczygiel, P. Otfinowski, Front-End and Back-End Solutions in the CBM STS Readout ASIC, TWEPP 2016.

[3] P. Otfinowskin, P. Grybos, R. Szczygiel, K. Kasinski, Offset correction system for 128-channel self-triggering readout chip with in-channel 5-bit energy measurement functionality, AGH, Av. 30, B1/203, 30-059 Krakow, Poland.