LLRF and synchronization system of the NICA complex

NICA Machine Advisory Committee 10-12 Nov 2021

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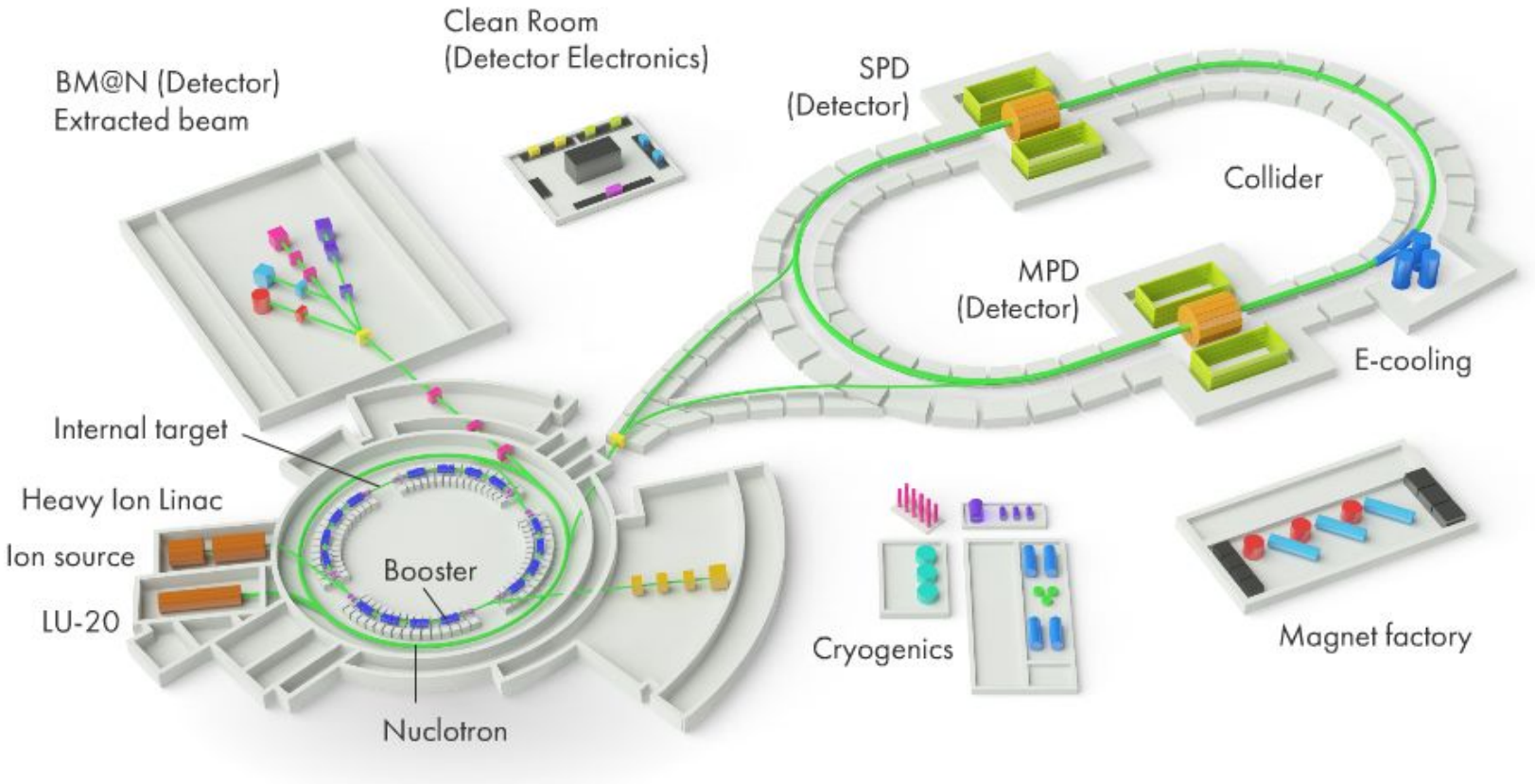
NICA


Clean Room
(Detector Electronics)
BM@N (Detector)
Extracted beam
SPD
(Detector)
Collider
MPD
(Detector)
E-cooling
Internal target
Heavy Ion Linac
Ion source
LU-20
Booster
Nuclotron
Cryogenics
Magnet factory

Project Schedule

Signed contract framework:

Stage 1: Present - May 2022 Synchronization B+N

Stage 2: June-Nov 2022 Synchronization and LLRF B+N

Stage 3: Dec-May 2023 Development for Collider

← Hardware arrives April 2023

Stage 4: June-July 2023 Assembly for Collider

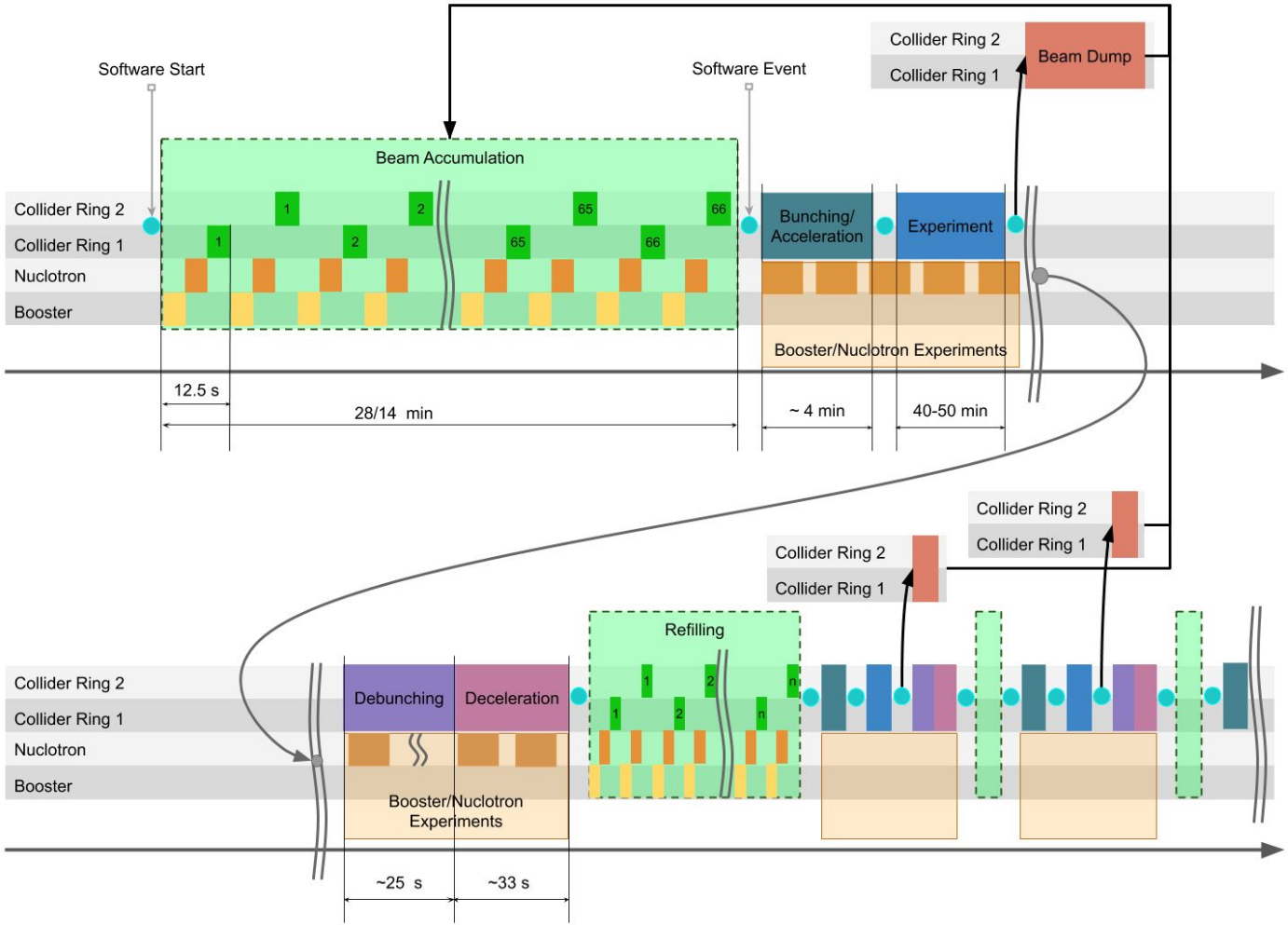
Stage 5: Aug-Nov 2023 Commissioning Collider

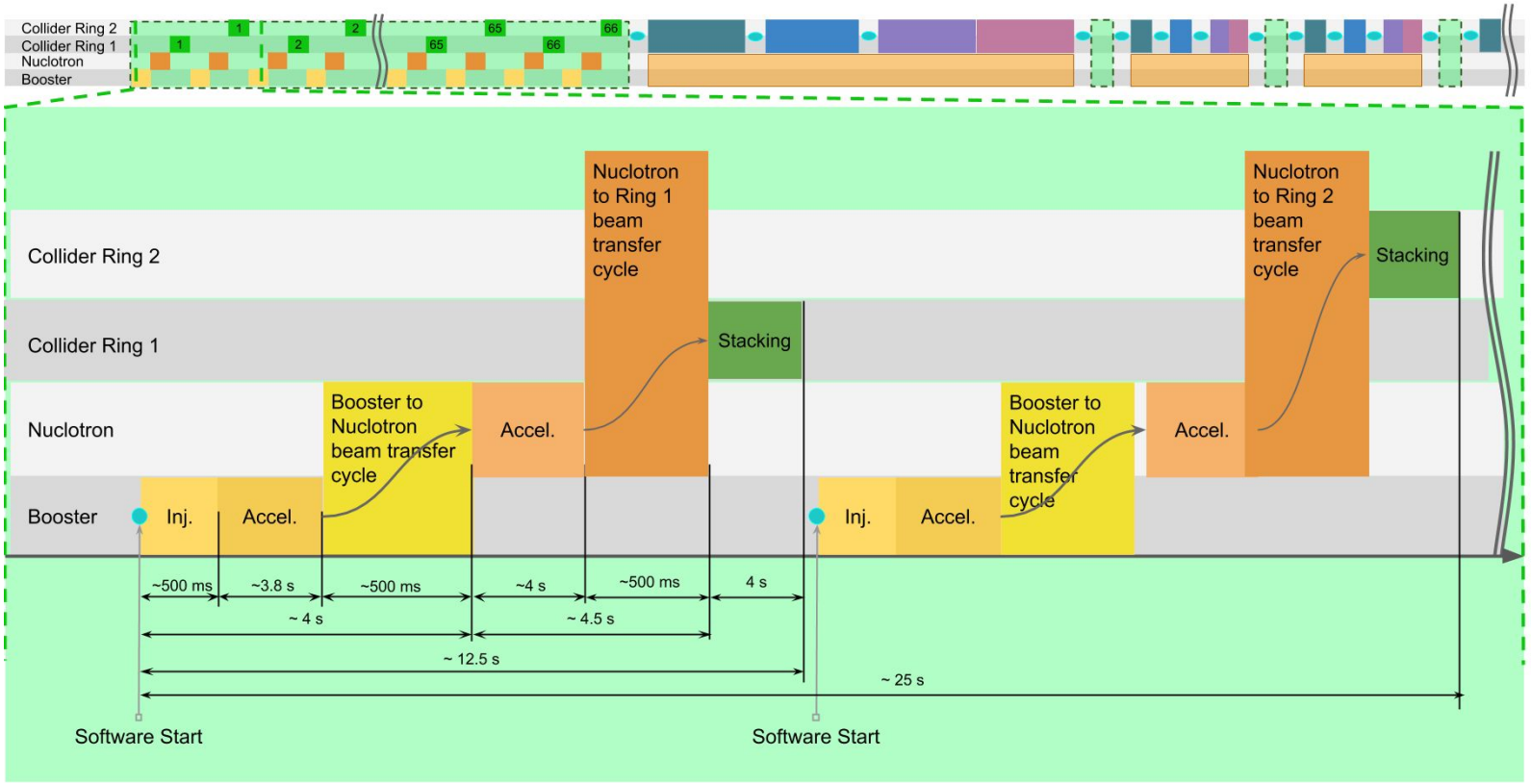
2021	JAN	FEB	MAR	APR	MAY	JUN	JULY	AUG	SEP	OCT	NOV M0	DEC M1
2022	JAN M2	FEB M3	MAR M4	APR M5	MAY M6	JUN M7	JULY M8	AUG M9	SEP M10	OCT M11	NOV M12	DEC M13
2023	JAN M14	FEB M15	MAR M16	APR M17	MAY M18	JUN M19	JULY M20	AUG M21	SEP M22	OCT M23	NOV M24	DEC

Timeline

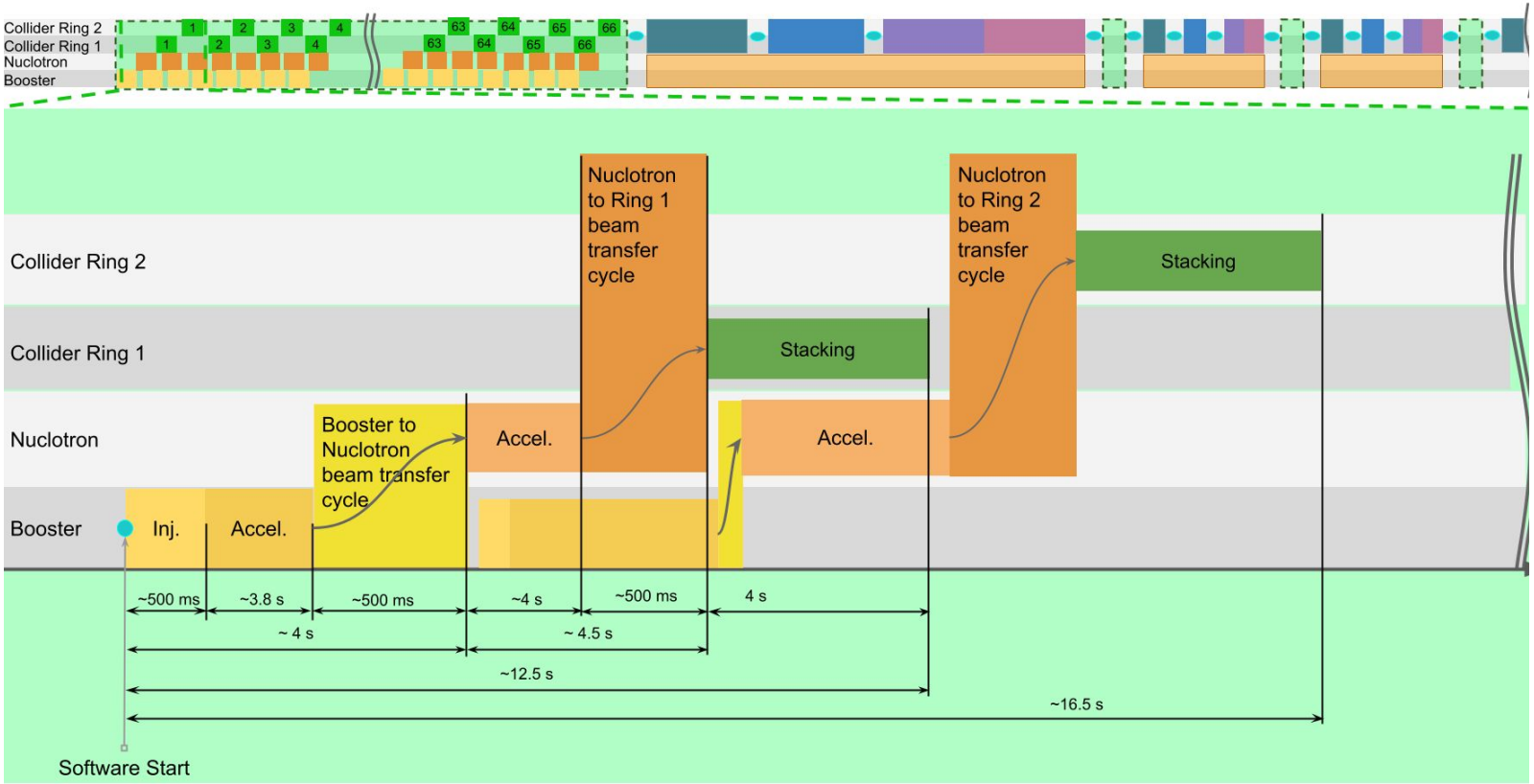
Time Diagrams

Time Diagrams

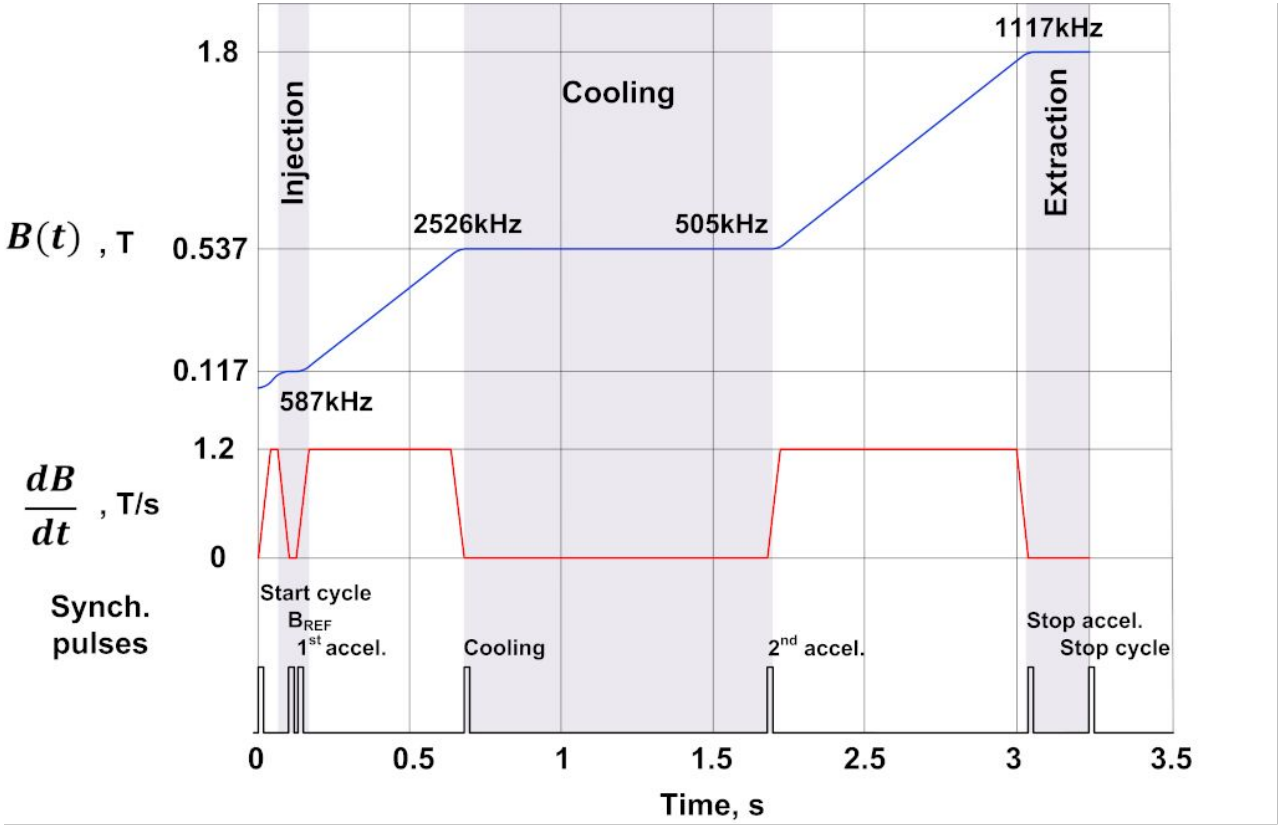




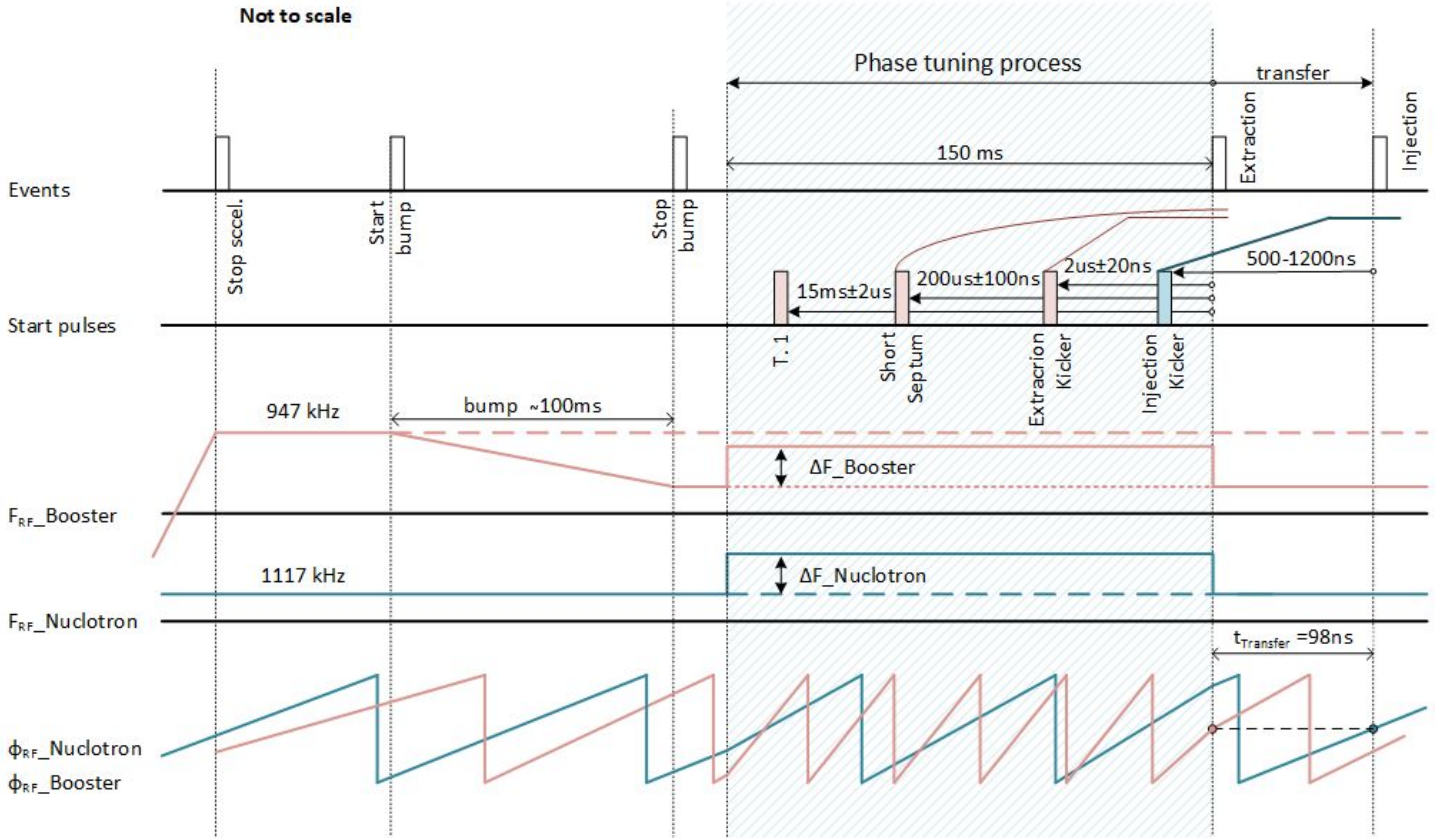
Collider Injection: Manual Mode



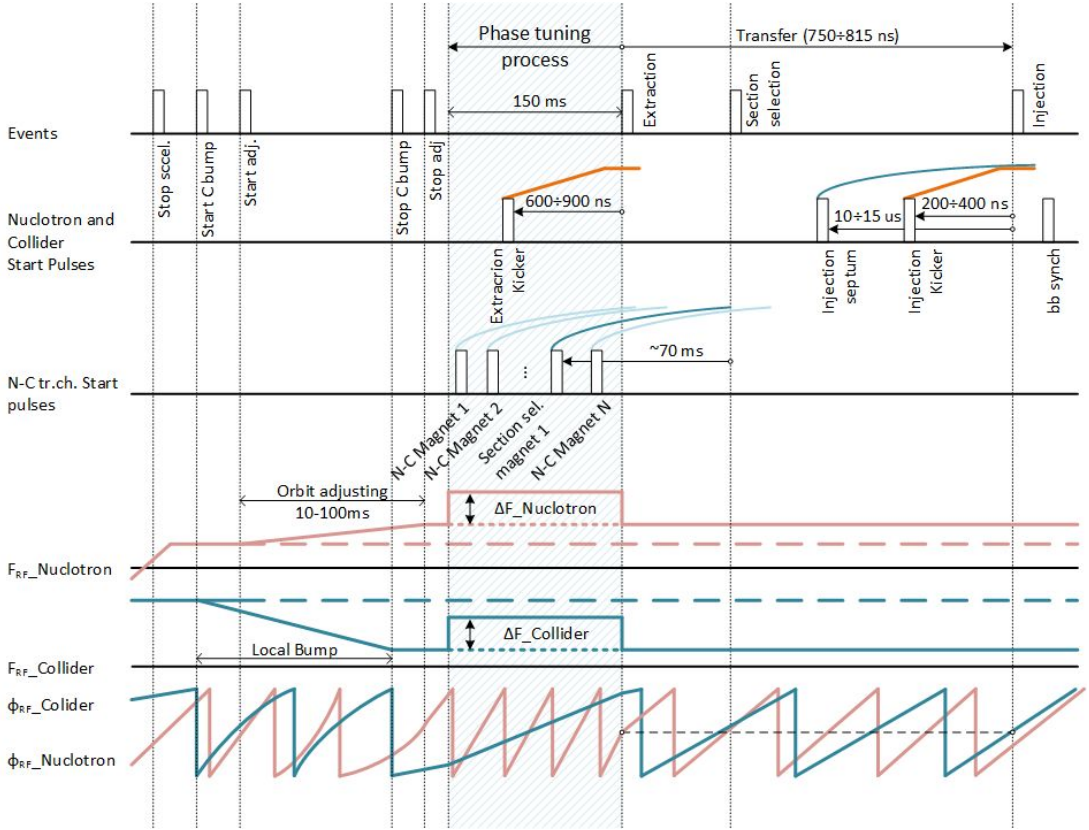
Collider Injection: Automatic Mode



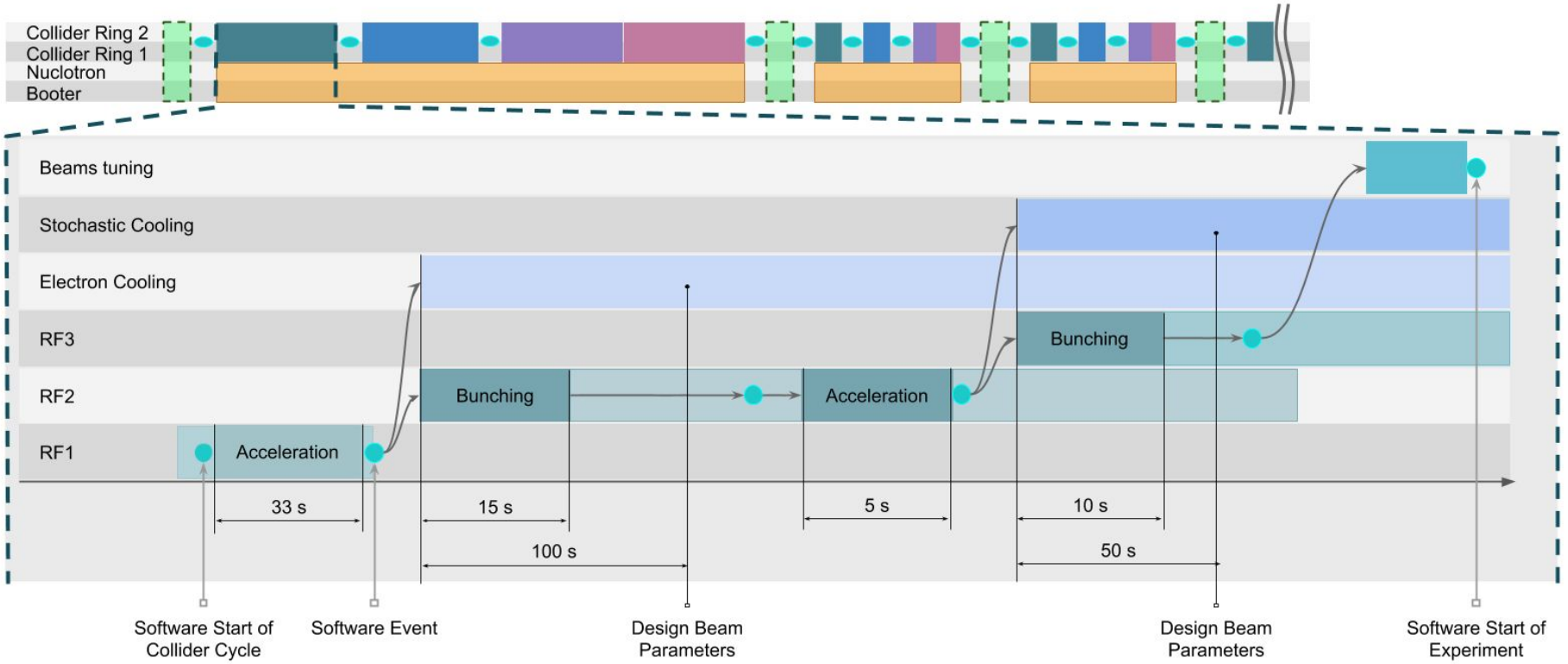
Booster Acceleration



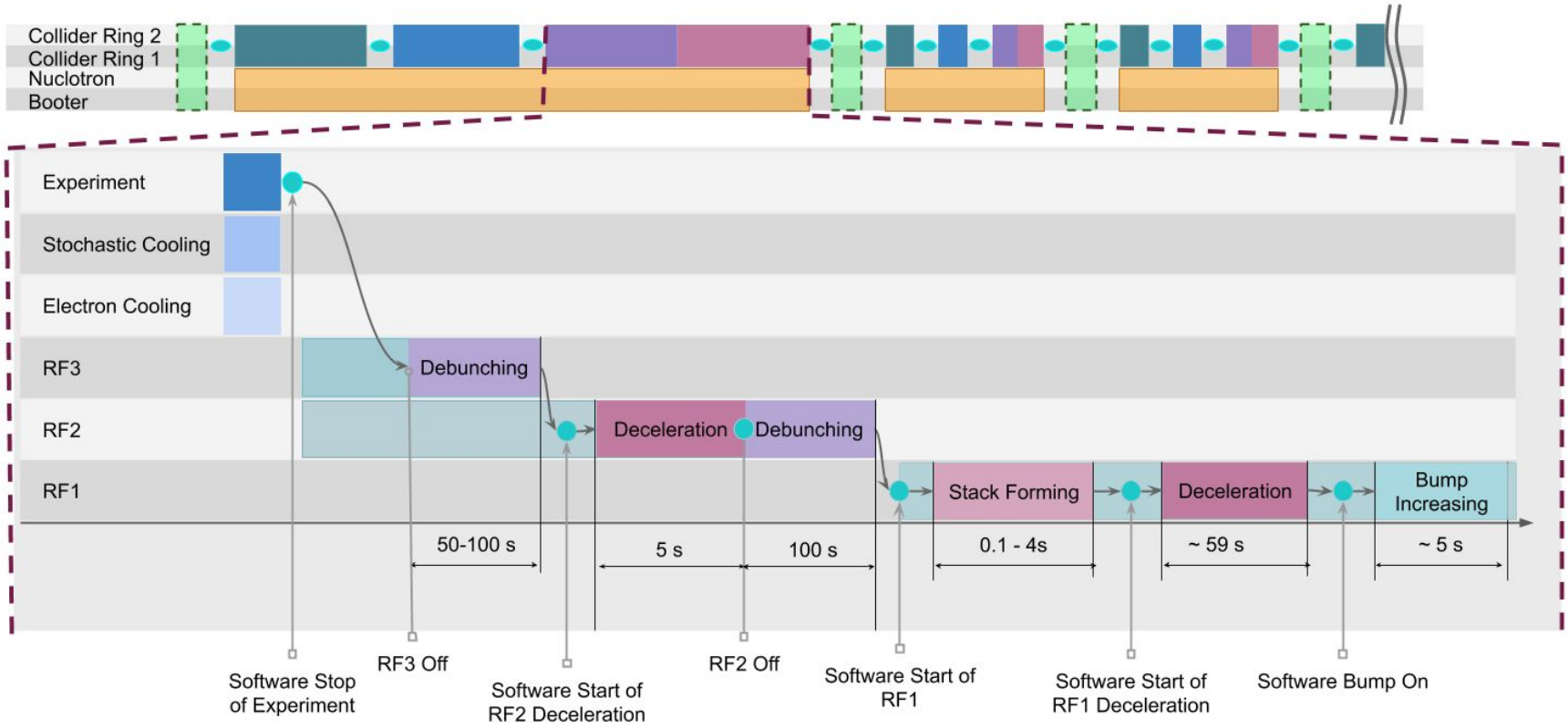
Booster-Nuclotron Injection



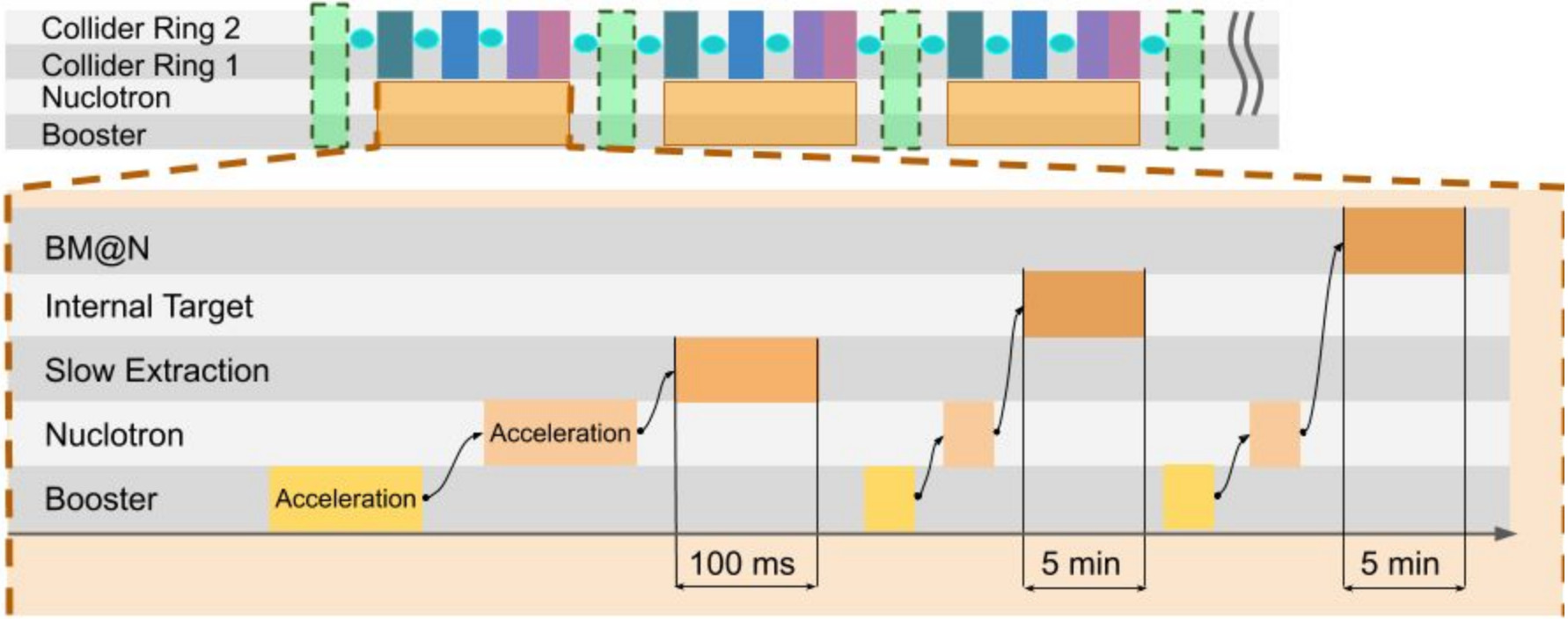
Nuclotron-Collider Injection



Collider Acceleration



Collider Deceleration



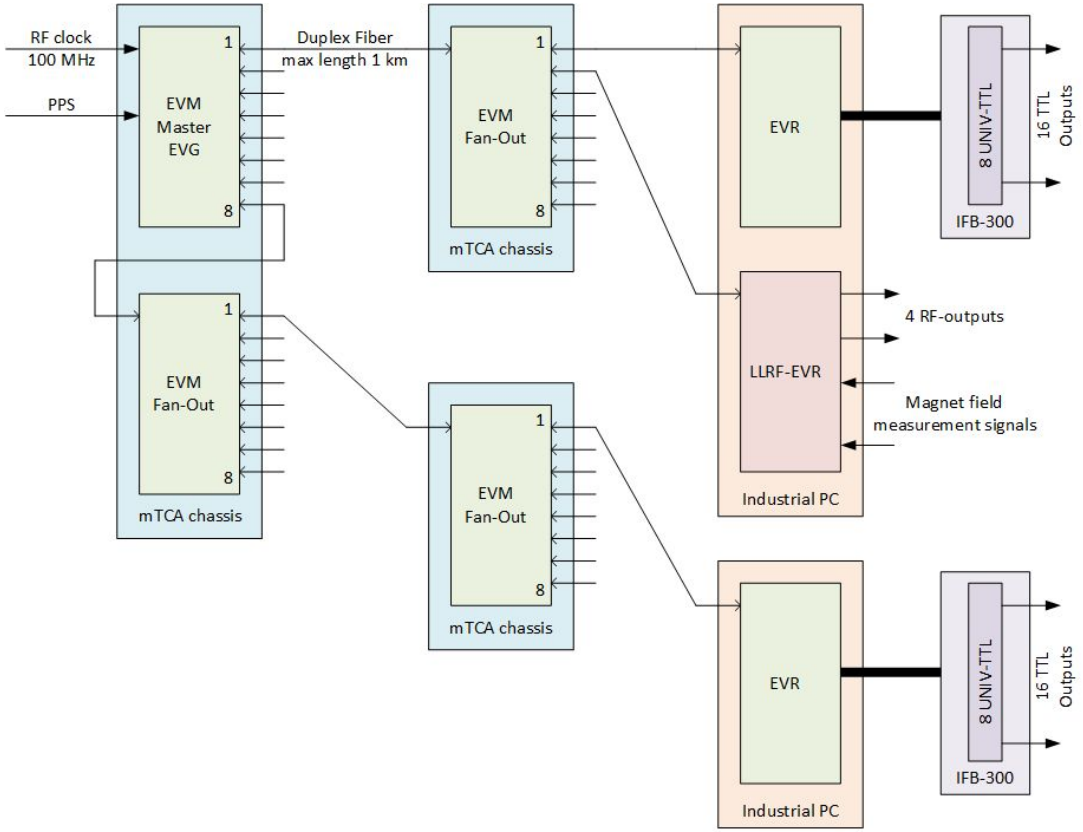
Nuclotron beamlines

Hardware

Multi-level system based on following building blocks:

- mTCA chassis with EVM’s
- Industrial PC’s with:
  - EVR + IFB-300
  - LLRF-EVR

Extensible and reconfigurable



Hardware configuration principle

mTCA Crate:

- Crate Schroff 11890-164
- Power Supply NAT-PM-AC600D (Schroff 11098-547)
- MCH (Carrier hub) NAT-MCH-PHYS48
- CPU module Concurrent AM G64/471-41
- One or several mTCA-EVG-300U

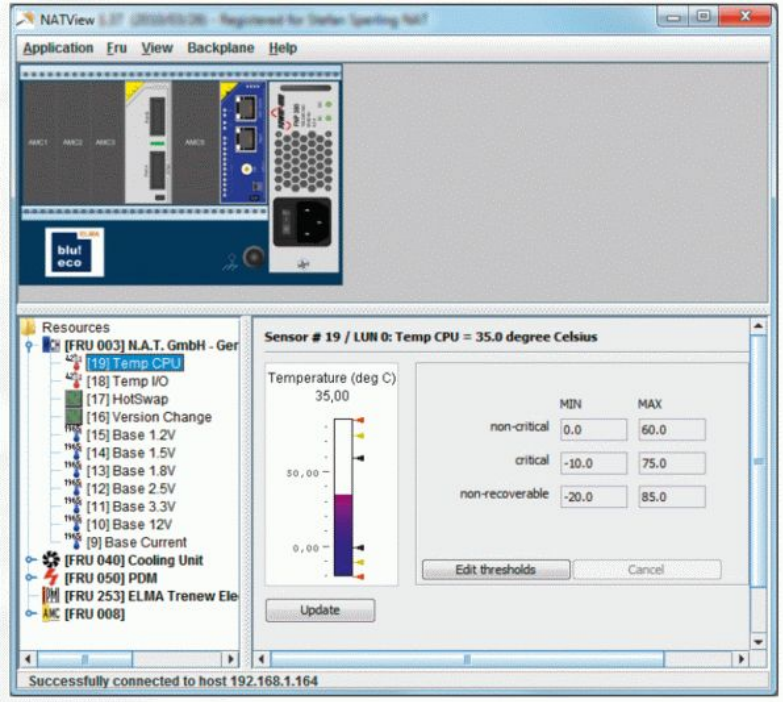
Concurrent AM G64/471-41 CPU module:

- Quad Core 3.0 GHz Intel Xeon E3-1505M v6
- Up to 32 GB ECC DDR4 SDRAM
- Two Gigabit Ethernet front panel ports
- 64 GB SATA micro SSD
- IPMI 2.0 management with IPMI Over LAN
- ...

MTCA Chassis composition

NAT NAT-MCH-PHYS80 MCH interconnector

- MicroTCA Carrier Hub
- Management for 12 AMC modules
- Supports configurable emergency shutdown of AMCs or entire system
- Supports remote Chassis control and maintenance through NATView software



MTCA Chassis composition

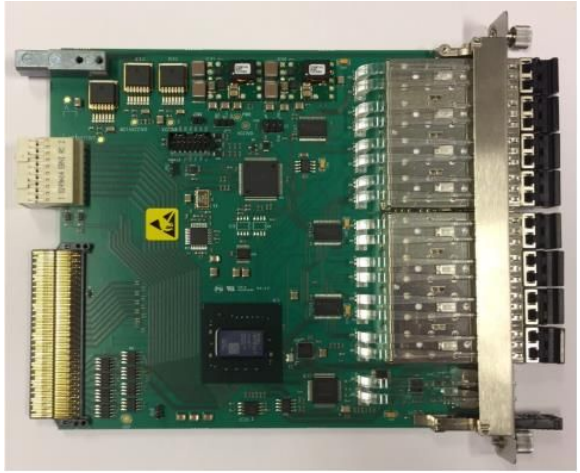
Proposed Industrial PC characteristics:

- Steel enclosure 19" 4U
- Intel Core i5 8400 2.8 GHz
- 2x8Gb DDR4 2400
- Two 10/100/1000 Mbit/s Ethernet
- Watchdog
- 1 PCI Express x1, 2 PCI Express x8 x1, 2 PCI Express x1 (1xPCI Express x4, 1xPCI Express x16)
- Power Supply: Industrial, ATX PS/2 400 W, can be used in a redundand configuration 2x400W
- Intel VPro remote maintenance support (AMT)
- ...

Industrial PC

mTCA-EVM-300:

- mTCA AMC.4 module
- 8 optical links (1 uplink+7 downlinks or 8 downlinks)
- Nested distribution of clocks and Events
- Up to 255 configurable Events
- Data transfer capability
- Industrially proven solution

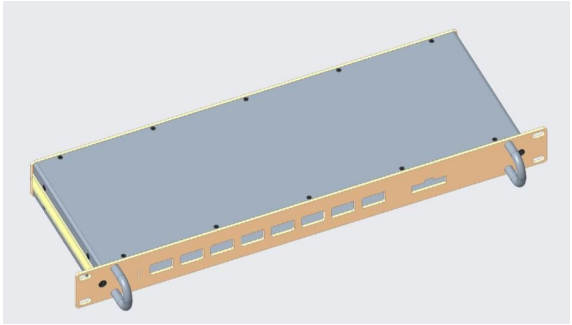


PCIe-EVR-300:

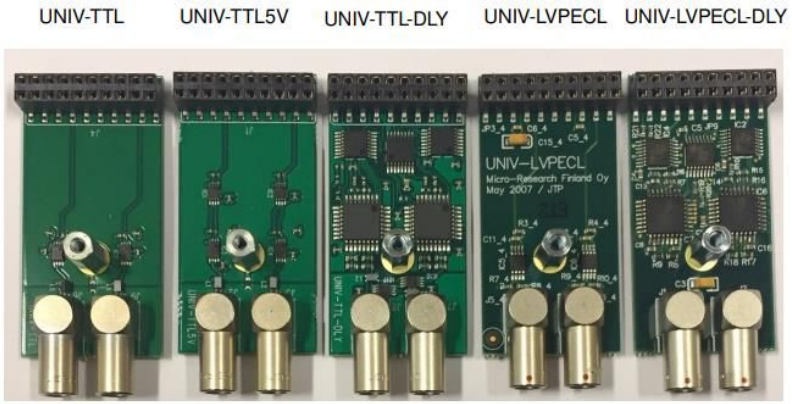
- 2U PCIe module
- Event receiver
- Complex Event reaction configuration

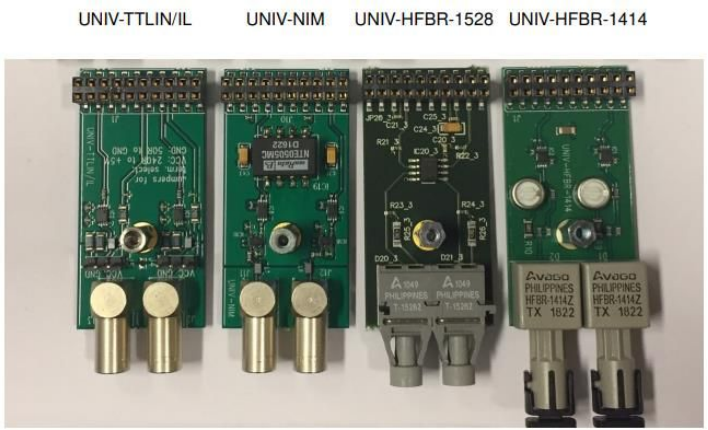
IFB-300:

- 8 MRF-UNIV slots
- High-speed SAMTEC connector
- 4 indication Led’s

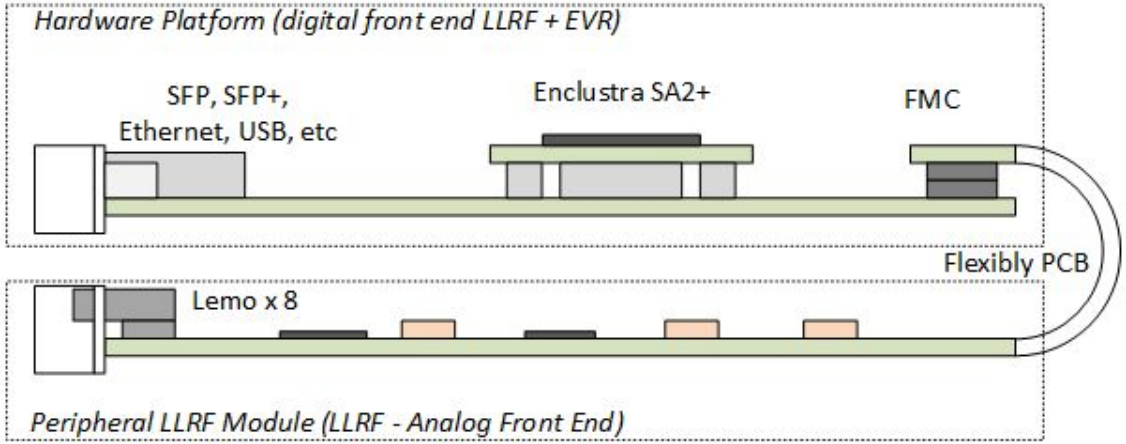


UNIV modules variations:





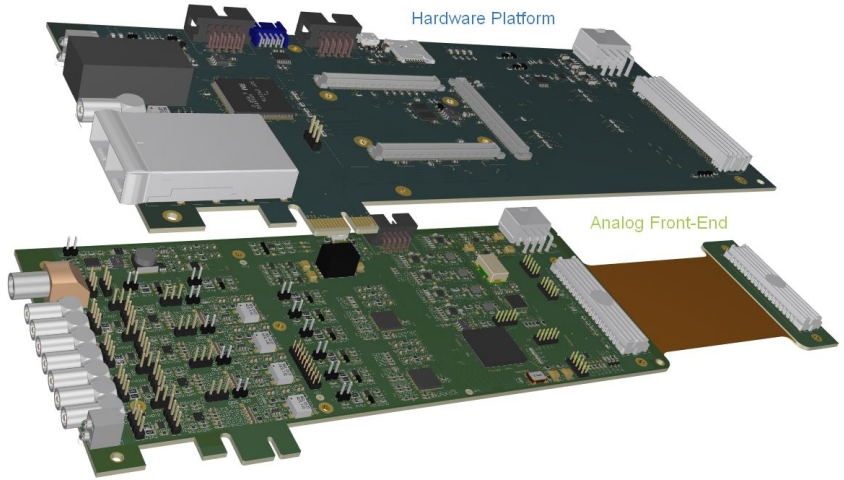
Timing subsystem: IFB-300 + UNIV Boards



$$f(B) = K\frac{Z\rho}{LA_n 10^6}\frac{c^2 B}{\sqrt{m_n^2 + \left(\frac{c^2 Z\rho}{LA_n 10^6}\right)^2 B^2}},$$

LLRF device

- 2U PCIe module
- Event receiver



The LLRF device concept

LLRF I/O channels:

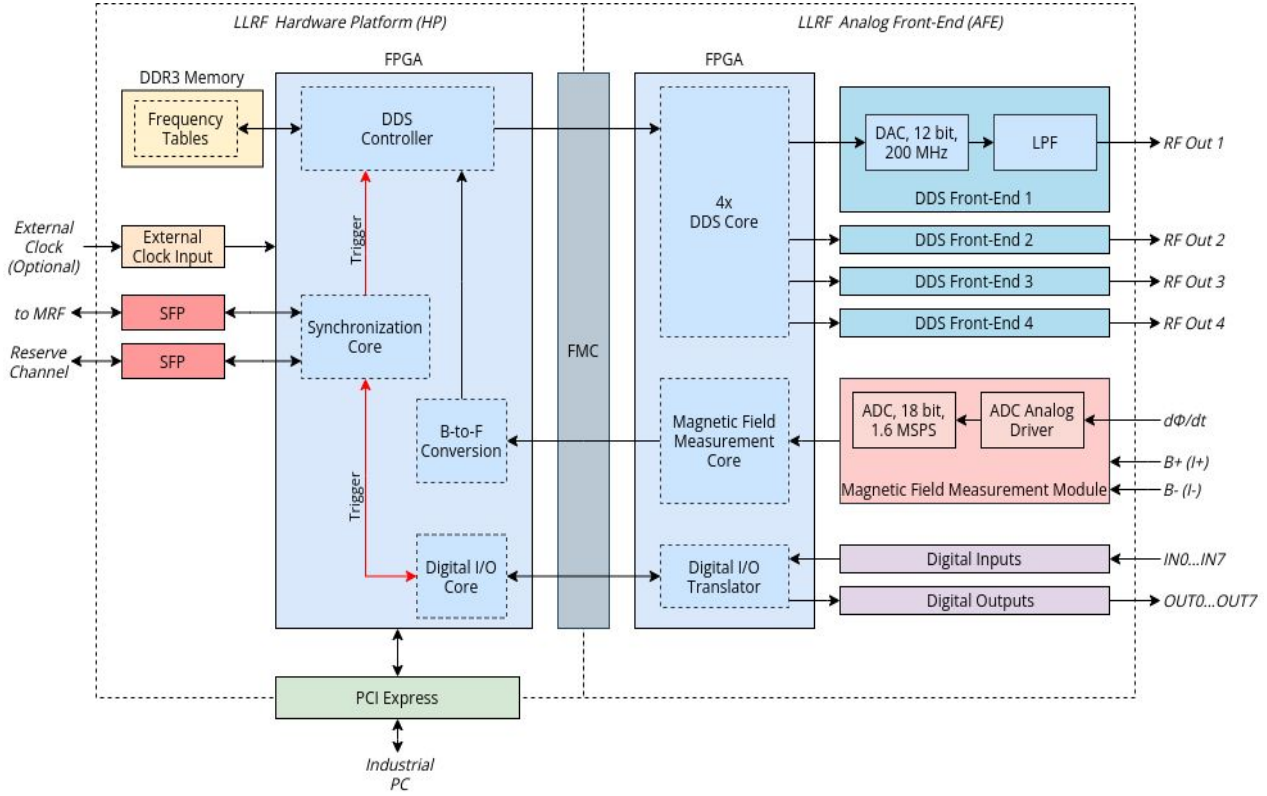
- 4x RF Outputs
- Magnetic field measurement inputs
- Up to 8 Digital Inputs/Outputs
- Optional External Clock Input

LLRF communication interfaces:

- 2x SFP connectors
- PCI Express

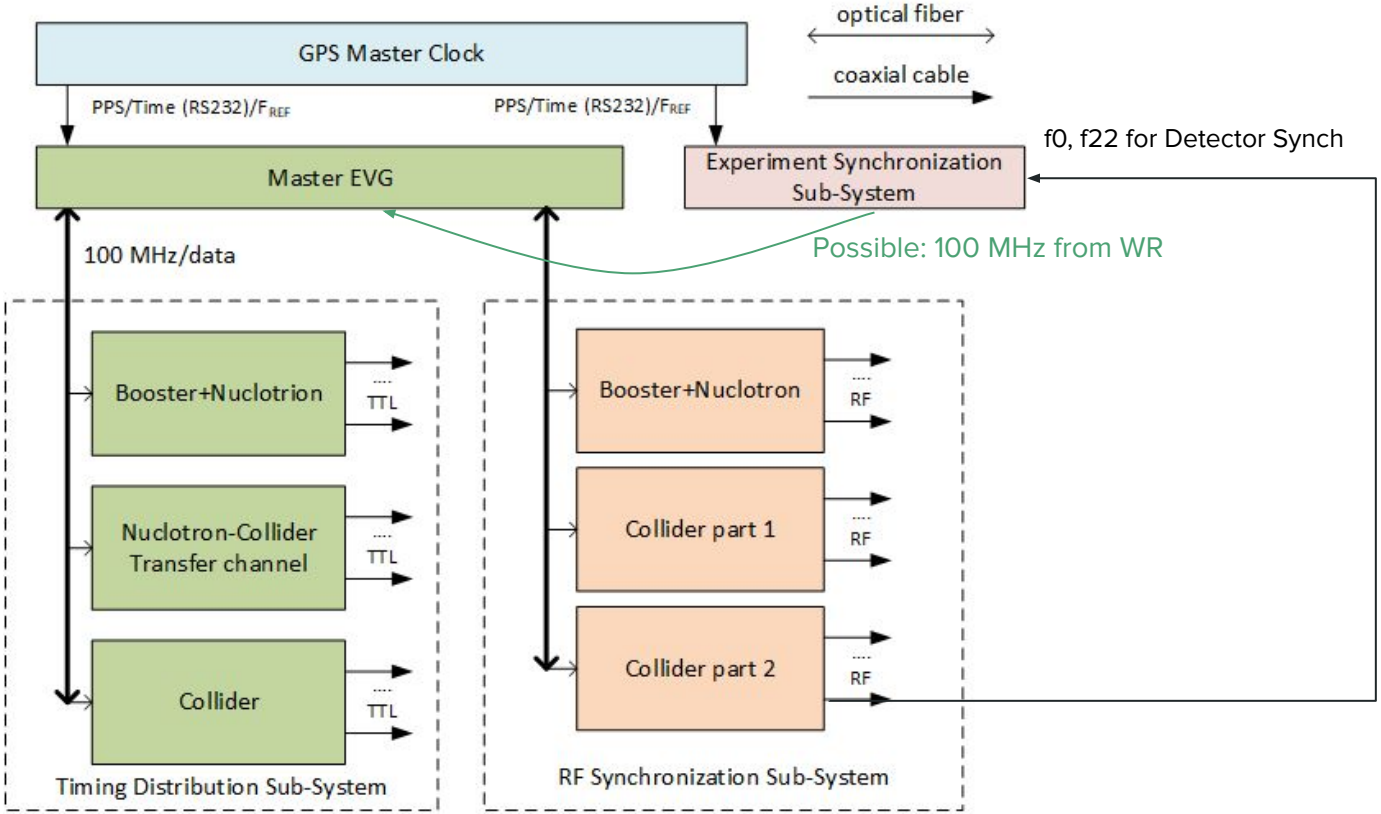
LLRF main functionality:

- Frequency Generation
- Magnetic field to Frequency conversion (Equation/Table)
- Synchronization with MRF Network
- Event-based operation
- Digital I/O control

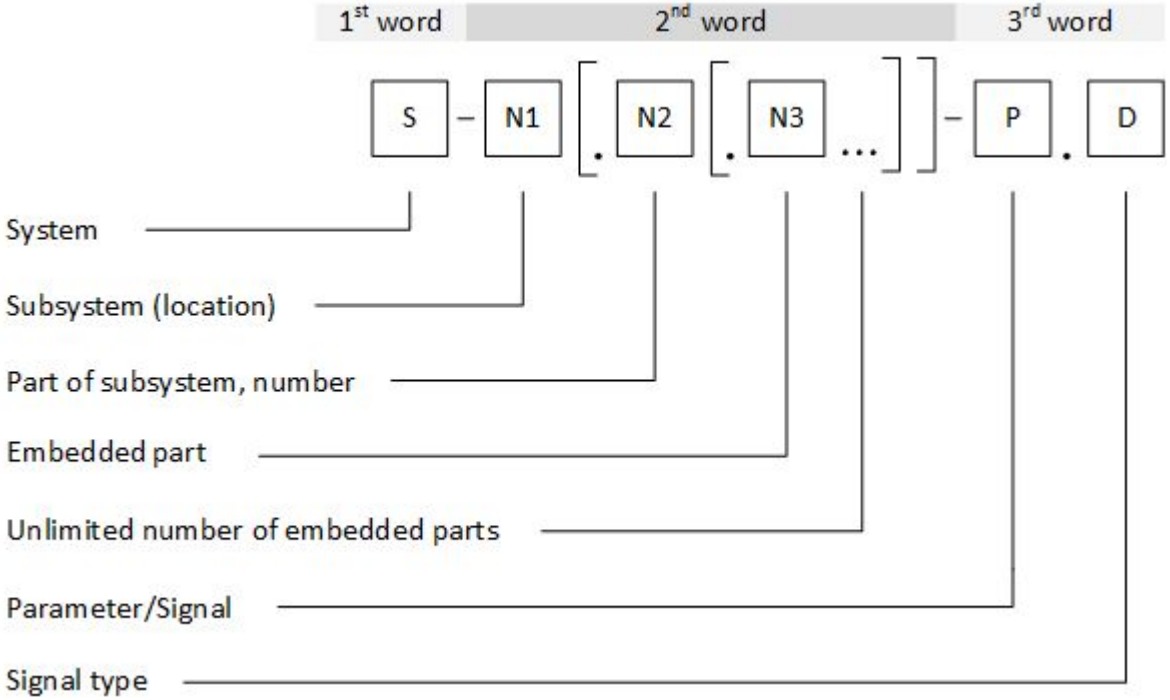


The LLRF Hardware Platform and Analog Front-End

System structure

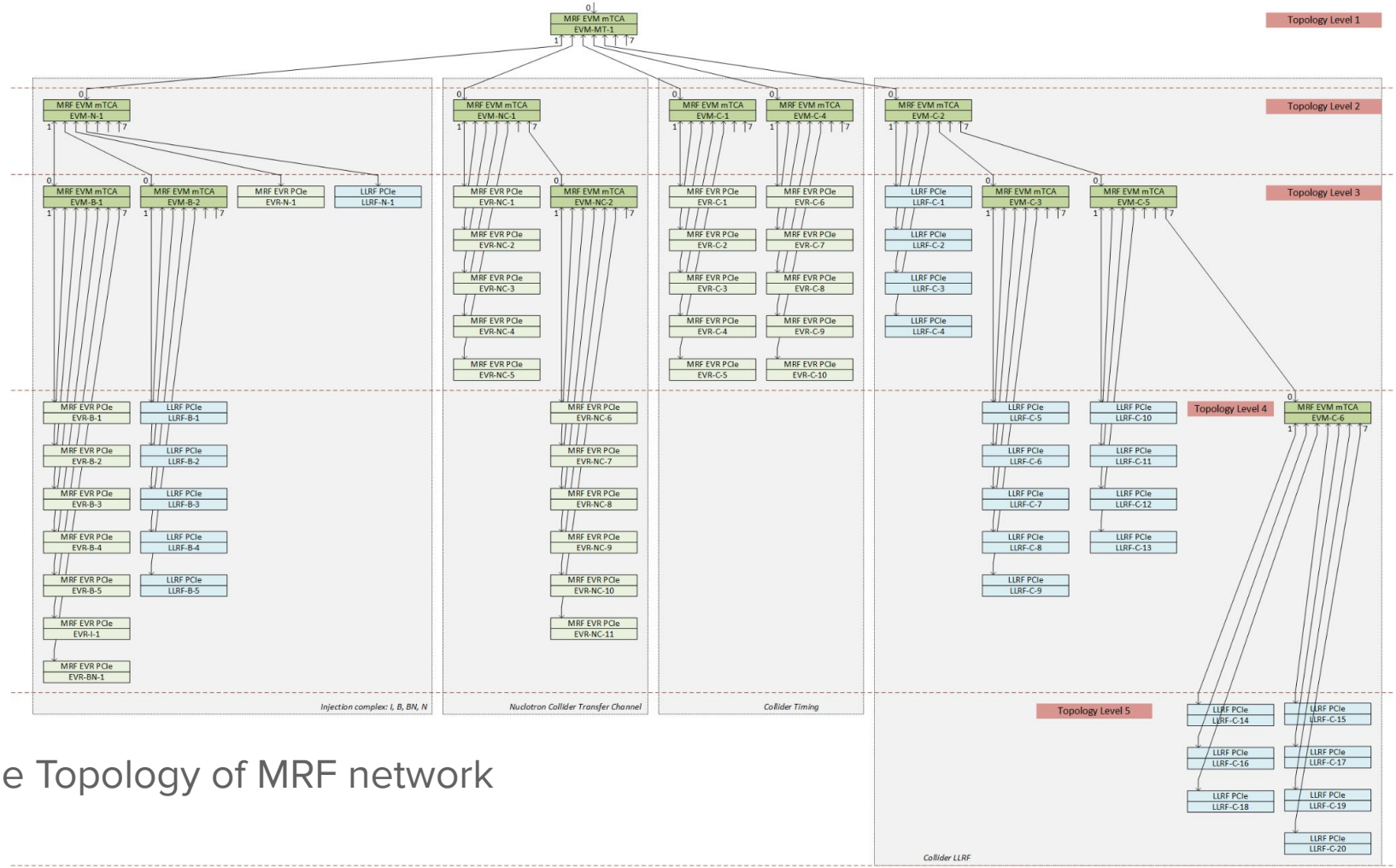


Timing and LLRF Networks Functional Diagram



Example: C-RNG1.RF_1-RF Collider - Ring 1 - RF1 - RF Channel

Channel Naming Principle



The Topology of MRF network

Types	Out channel q-ty	MRF-EVR Q-ty	Location information
B Injector	3	1	Control room
N Injector	2	1	Control room
Booster	57	5	4 (1 for each quadrant) + 1 in central room + 1 HUB
BN channel	3	1	BN channel control room
Nuclotron	16	1	1 in central room
NC channel	128	13	1 for each room (223, 262, 267: x2) + 2 HUB
Collider	108	9	one for each room + 2 HUB
Total	**317**	**31**	

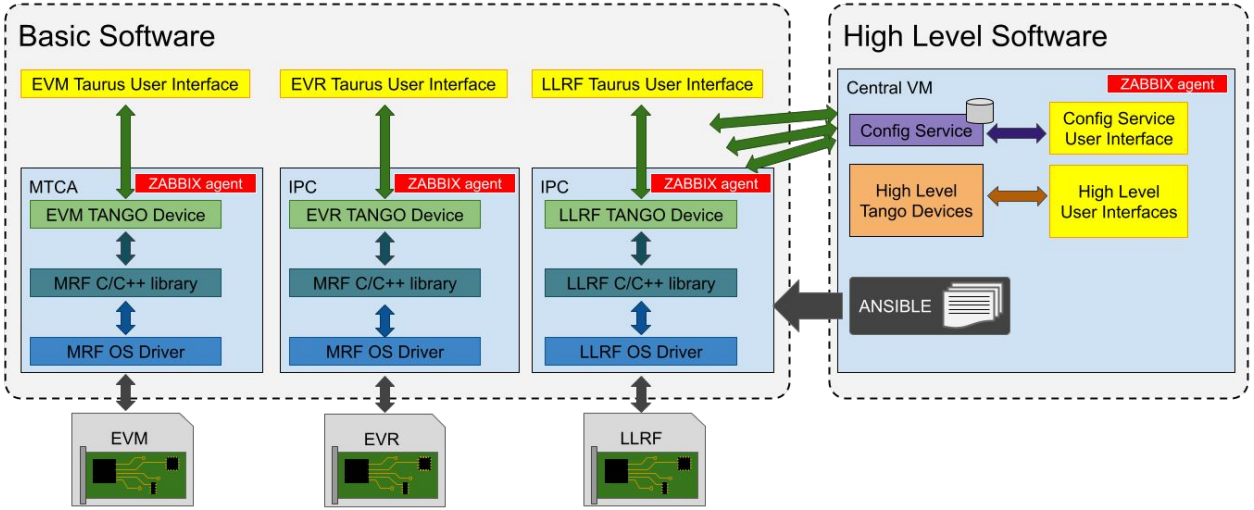
Types	Out channel q-ty	LLRF-EVR q-ty	Lcation information
Booster	18	6	4 (1 for each quadrant) + 1 in central room + 1 HUB
Nuclotron	1	1	1 in central room
Collider	72	23	one for each room + 5 HUB
Total	**91**	**30**	

Number of Channels (Estimated)

Software

Basic Software
- Linux OS Driver
- C/C++ API
- Tango Device
- Device Specific Taurus User Interface

High Level Software
- Configuration Service
- Configuration Service User Interface
- High Level Tango Devices
  - Monitoring
  - Alarm
- High Level User Interfaces



Tango 9.3.4

Taurus 4.6.*

Software

Operating System

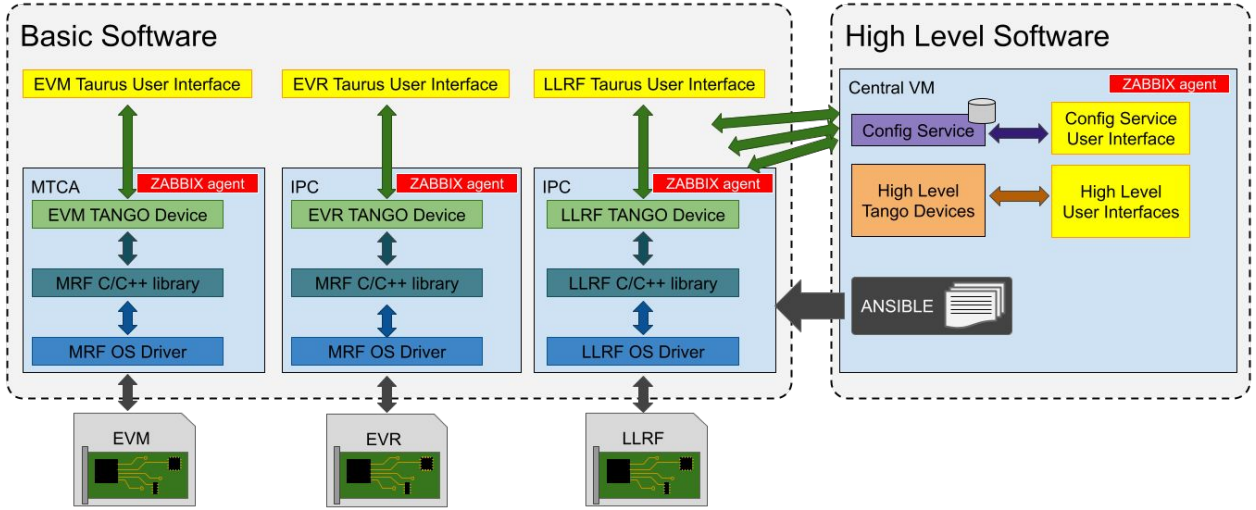
- mTCA Crate
  - CentOS 8/Debian 11
- Industrial PC (IPC)
  - Debian 11
- Central Virtual Machine
  - Debian 11

Deployment

- Ansible

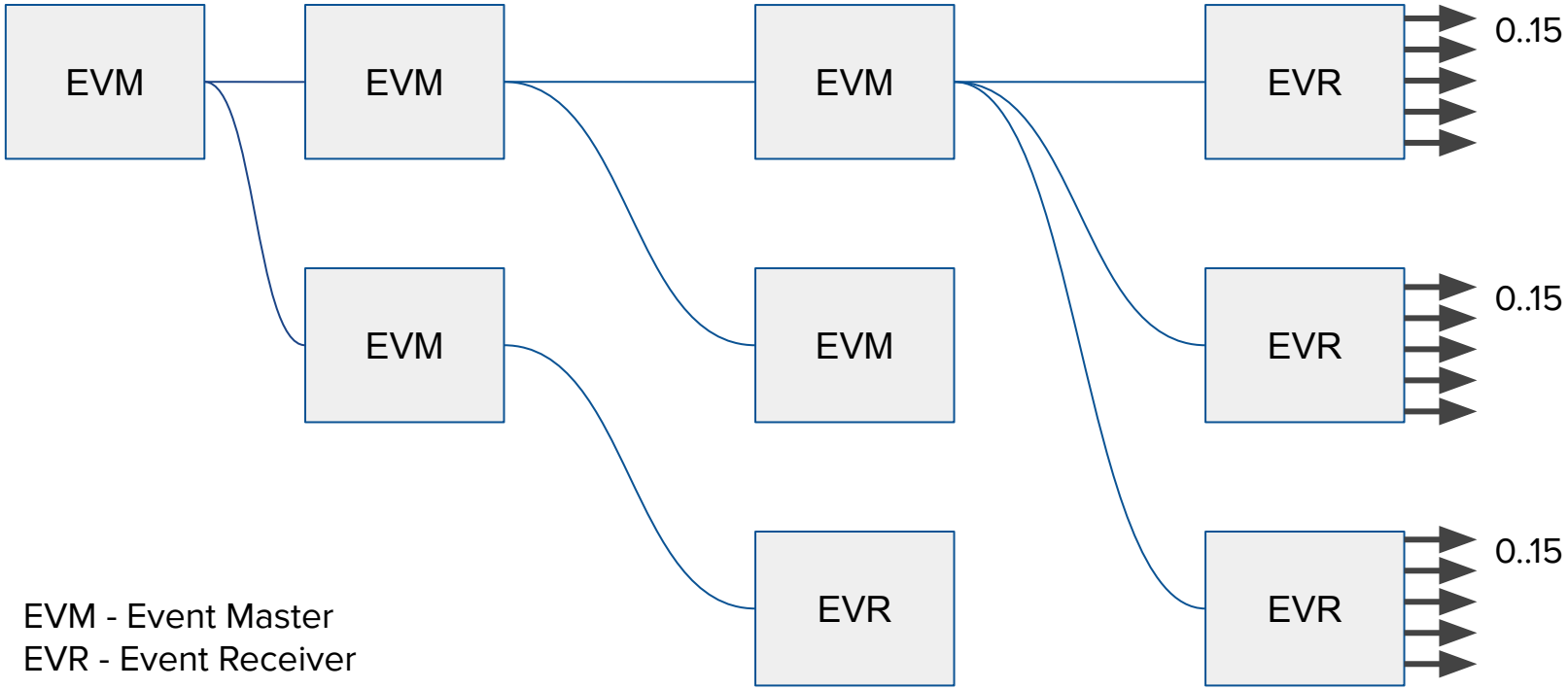
Zabbix Monitoring

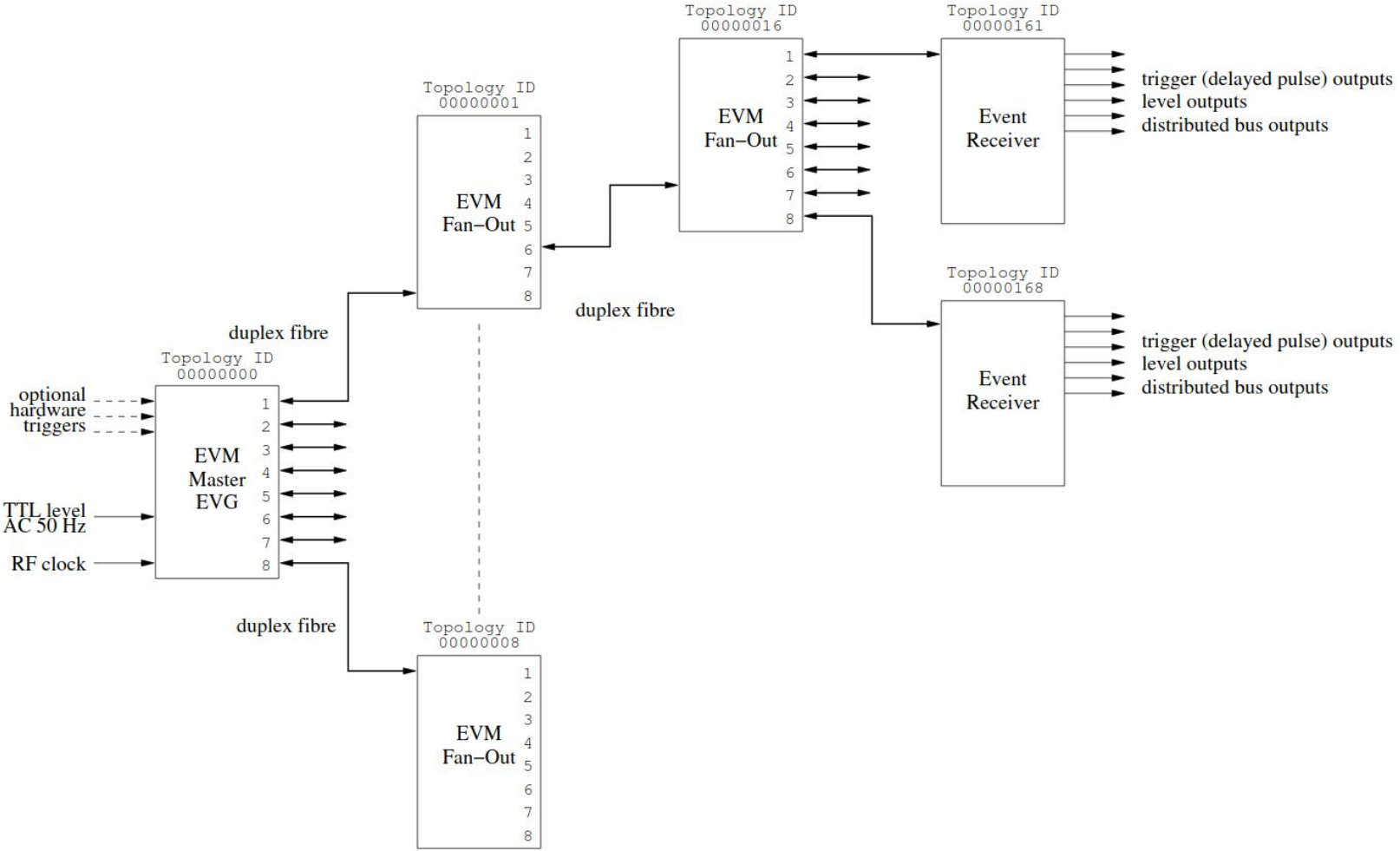
- CPU
- RAM
- Disk
- I/O
- Temperature
- .....

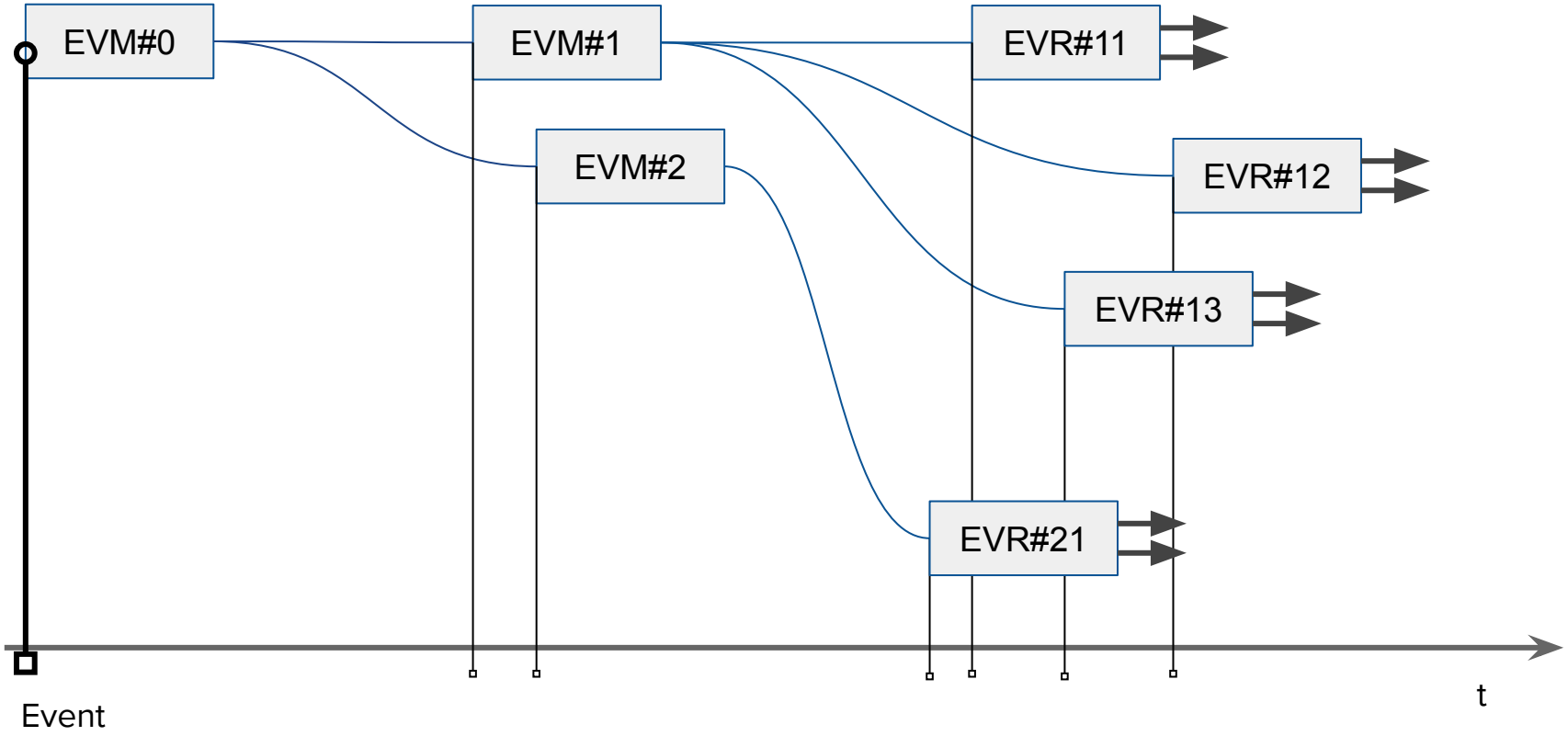


Software

Appendix


EVM
EVM
EVM
EVR
0..15
EVM
EVM
EVR
0..15
EVR
EVR
0..15
EVM - Event Master
EVR - Event Receiver


Topology ID
00000000
EVM
Master
EVG
optional
hardware
triggers
TTL level
AC 50 Hz
RF clock
1
2
3
4
5
6
7
8
duplex fibre
Topology ID
00000001
EVM
Fan–Out
duplex fibre
Topology ID
00000016
EVM
Fan–Out
Topology ID
00000161
Event
Receiver
trigger (delayed pulse) outputs
level outputs
distributed bus outputs
Topology ID
00000168
Event
Receiver
trigger (delayed pulse) outputs
level outputs
distributed bus outputs
duplex fibre
Topology ID
00000008
EVM
Fan–Out


EVM#0
EVM#1
EVM#2
EVR#11
EVR#12
EVR#13
EVR#21
Event
t

t0	Booster Injection
t1	Booster CCE Start
t2	Booster Bump
t3	Booster Injection
t4	Booster Extraction
t5	Nuclotron CCE Start
t6	Inj to Collider Ring1
t7	Inj to Collider Ring2
t8	Collider Bump Off

t9	RF1 Acceleration Start
t10	RF2 Bunching Start
t11	RF2 Acceleration Start
t12	RF3 Bunching Start
t13	RF3 Acceleration Start
t14	IP Tuning +
t15	IP Tuning -
t16	RF3 Stop
t17	RF2 Deceleration

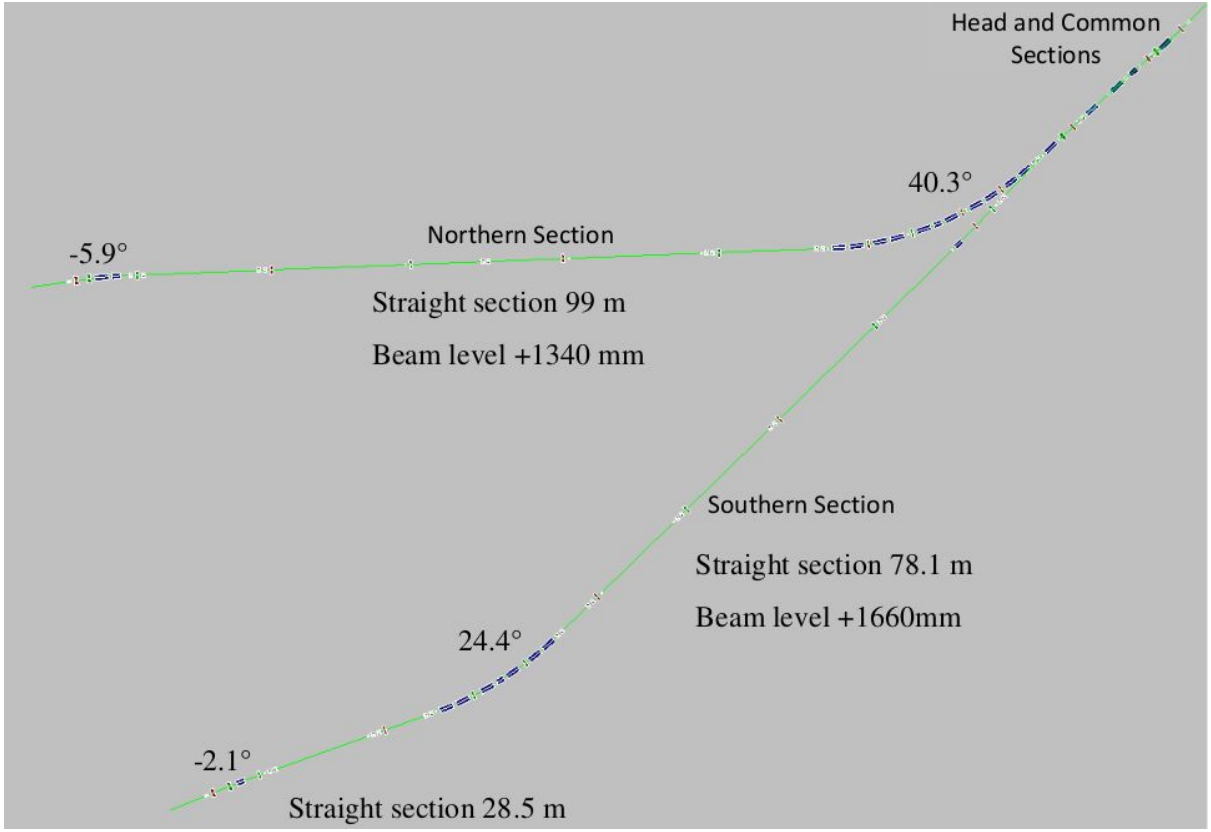
t18	Nuclotron Slow Extraction
t19	Nuclotron Beam Evacuation
t20	Nuclotron to BM@N

*	Collider Bump On
*	Beam Dump
*	Light Ion Injection

Event

8bit
0x01 – 0x6F - User -Defined
0x00 - Null event
0x7f - End of Sequence

EVM: Events



Инжекция Nuclotron-Collider