

# Updated approach for DAQ and Front-End Electronics Interface

Leonid Afanasyev,  
Vyacheslav Tereshchenko

# SPD detectors outputs (CDR version)

Table 7.1: Summary of detectors outputs to DAQ. Information type: T means time, A – amplitude (or charge).

Sub-detector	Information type	Number of channels	Channels per FE card	Number of outputs
Vertex detector 5 DSSD	T + A	460800	640	720
Vertex detector 3 MAPS+ 2 DSSD	T + (T + A)	(3024 + 596)*		864 + 596
Straw tracker	T + A	79200	64	1238
Calorimeter	T + A	30176	64	472
PID-ToF	T	20200	32	632
PID-Aerogel	T + A	320	32	10
BBC (inner+outer)	T + (T + A)	256 + 192	32	8 + 6
Range system	T	106000	192	553
ZDC	T + A	250 + 650	16	57
Total (max)		698044**		4436

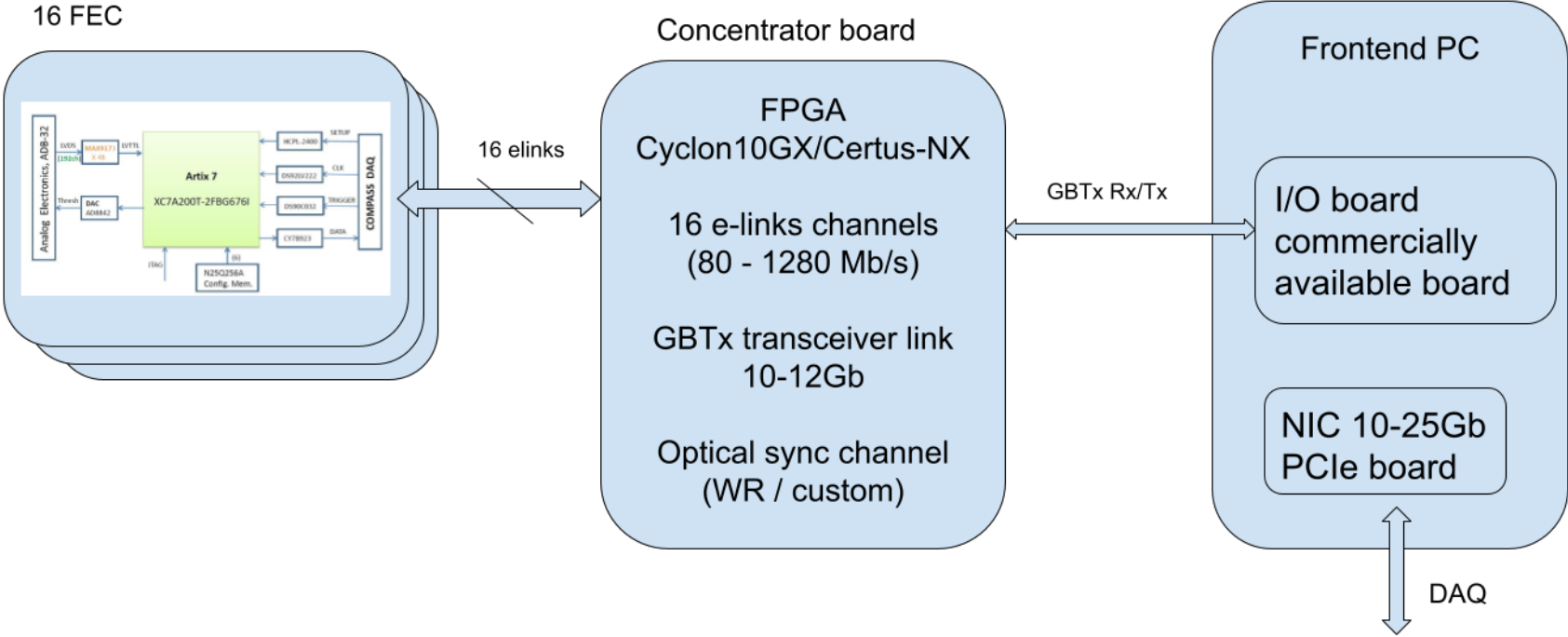
\* – number of sensors, see Section 4 of Chapter 4

\*\* – for DSSD version

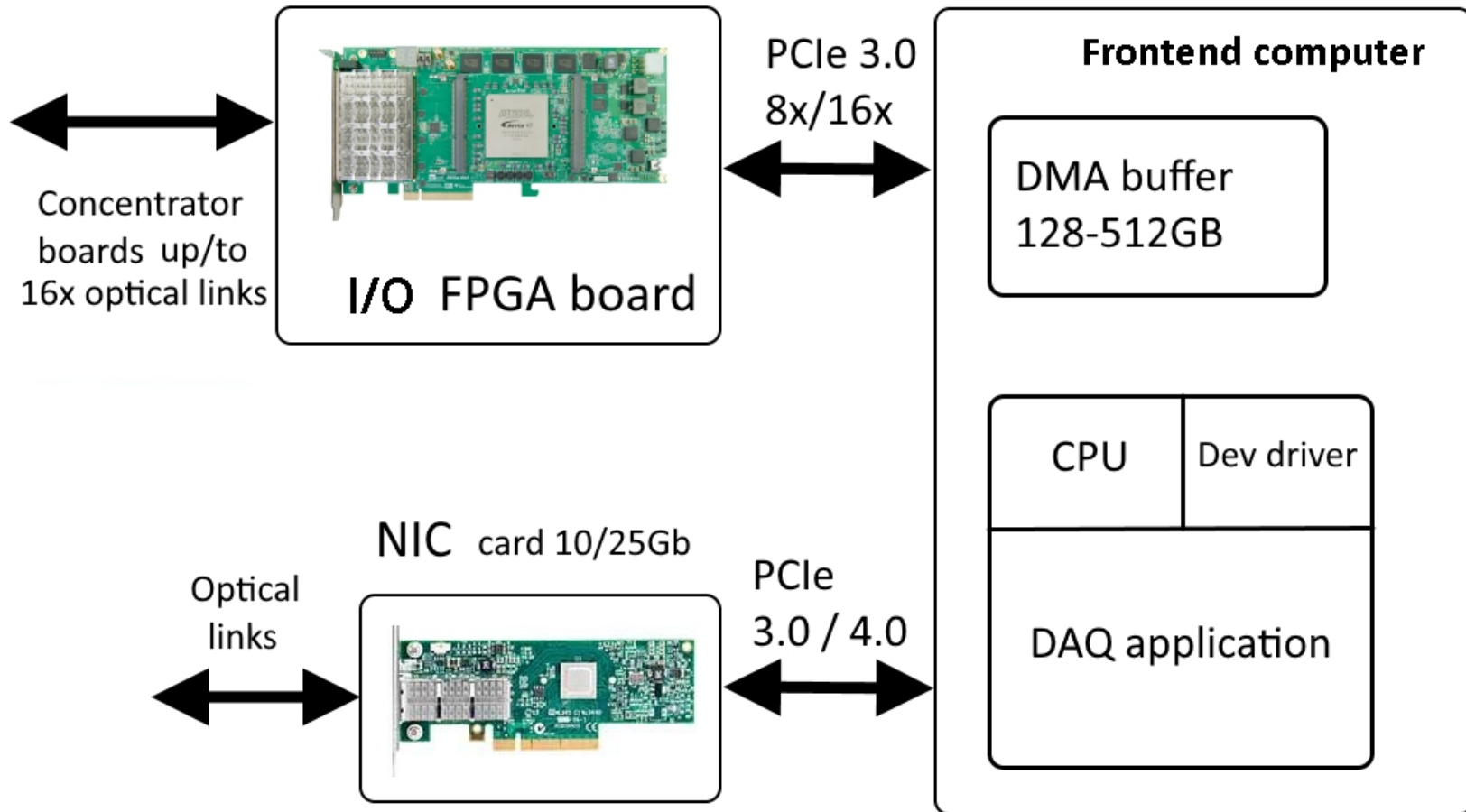
# Parameters of Range System

- Channels number – 106000 (140000 ?)
- Frontend cards – 553 (700)
- Hit rate for the detector(50 wires (event) + noise)  $200 * 4 * 10^6 = 8 * 10^8$  hits/s
- Hit rate for FEE board –  $1.6 * 10^6$  hits/s
- Bits rate for FEE board ~ 40 Mb/s (without headers), so we can use e-link with bit rate 160 – 640 Mb/s

# Frontend DAQ of the Range System

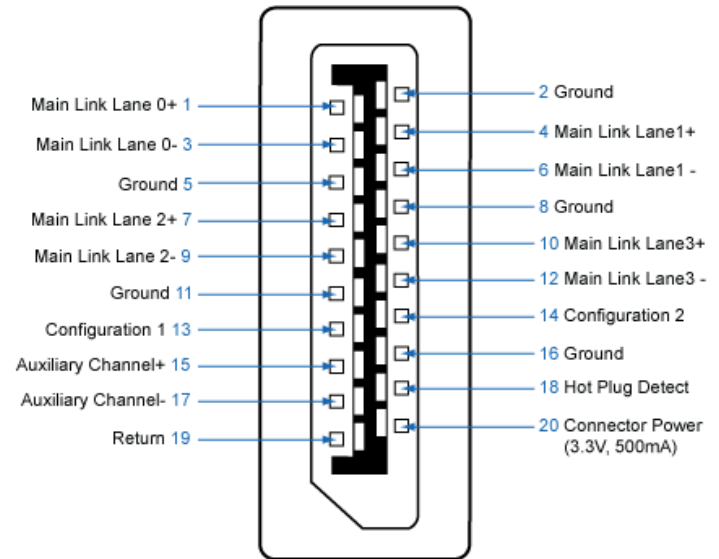


# Frontend computer



# E-link signals for Range System

- Cable/connector – DisplayPort (20 pins)
- 5 differential signals (link 1(2), clock, slice, frame)
- I2C bus
- 3 control signals (reset, hotplug, spare)



# Examples of I/O cards

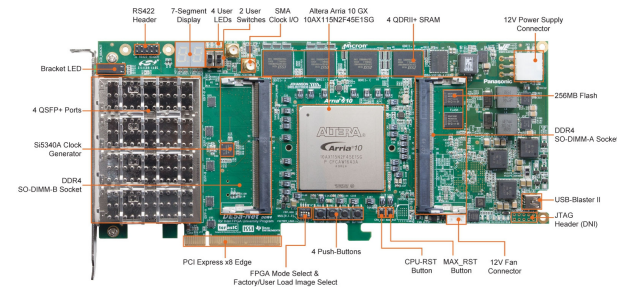
## V5052 16-Port PCI Express FPGA Card

- Four QSFP28 ports
- Xilinx Virtex UltraScale+ FPGA (VU9P)
- One bank of 4GB to 16GB 64-bit up to 1200MHz DDR4 SDRAM
- Supports PCIe Gen3 x 16 and Gen4 x 8

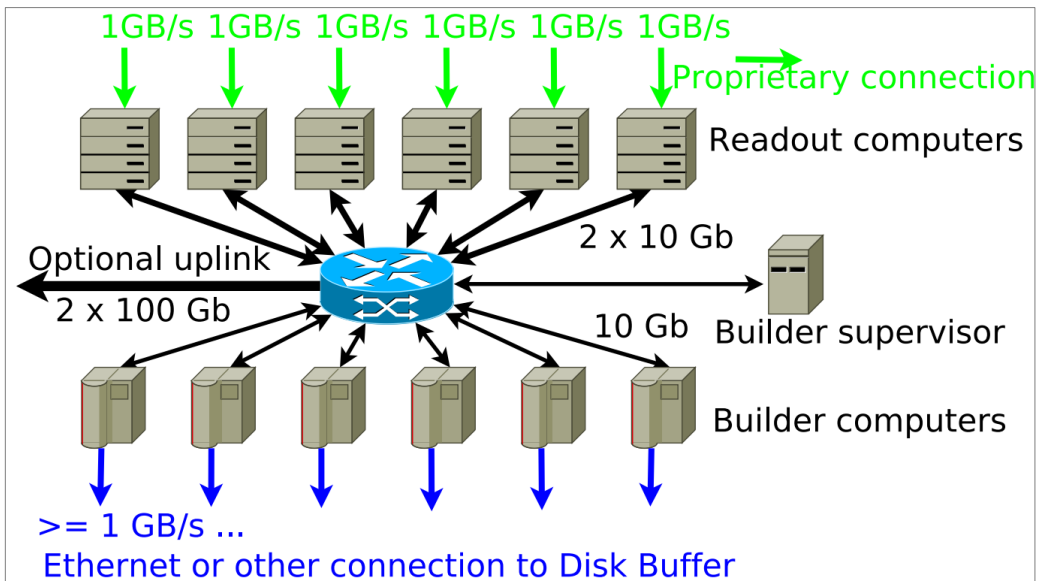


## DE5a-Net-DDR4

- Four QSFP28 ports
- Intel® Arria 10 GX FPGA
- up to 16GB 1200MHz or 32GB 1066MHz DDR4 SODIMM Sockets
- Supports PCIe Gen3 x 8
- Price: \$6,624



# Last stage of slice/frame building



The contiguous set of slices (chunk) or the full frame containing data from all detectors are built by the pool of Builder computers under control of the Builder supervisor.

- Multiplexers which form a sub-slices are installed as extension cards into the readout computers. Number of Multiplexers per one computer can be more than 1, it should be optimized.
- Number of readout computers will be defined by the bandwidth of Multiplexers, now it is estimated as 1 GB/s.
- Readout computer - diskless computer with 128GB RAM and 2 x 10 Gb or 1 x 25 Gb Ethernet.
- Builder computer - diskless computer with 64GB RAM, 10/25 Gb Ethernet and interface to Disk Buffer.
- Number of builder computer will be defined by the loading about 0.5GB/s per 1 builder computer.
- For the input flux of 20GB/s, the Ethernet switch should have at least 80x10 Gb or 60x25 Gb connections and 2x100 Gb uplink connection (if needed). The Disk Buffer is estimated to have 2PB with 50GB/s read/write access.