Silicon Tracking System of BM@N experiment (BM@N STS)

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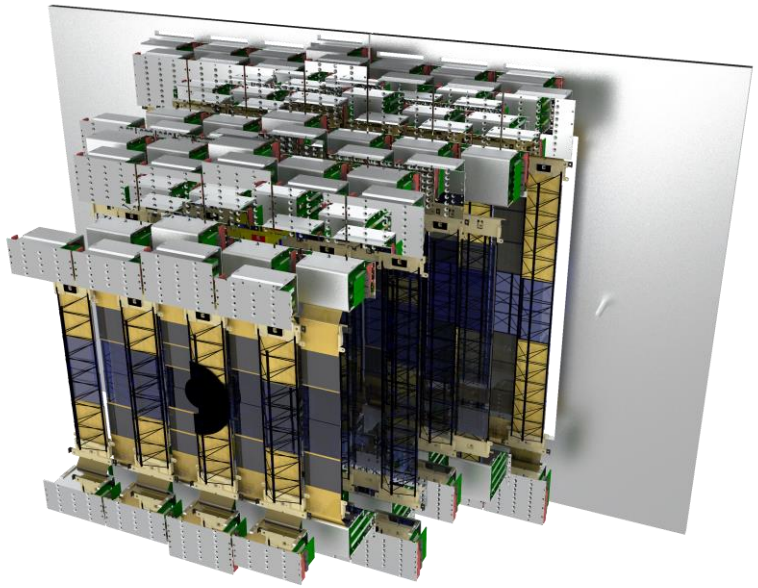
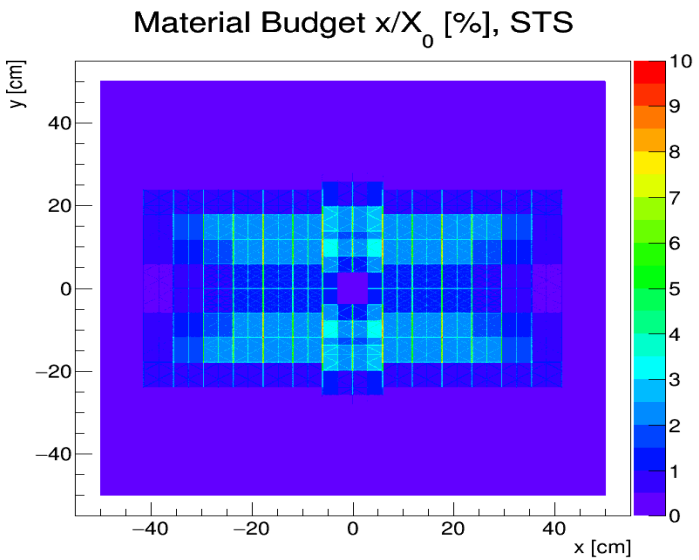
Silicon Tracking System (STS)





STS material budget

4 x STS stations

34 x Ladders

292 x Modules

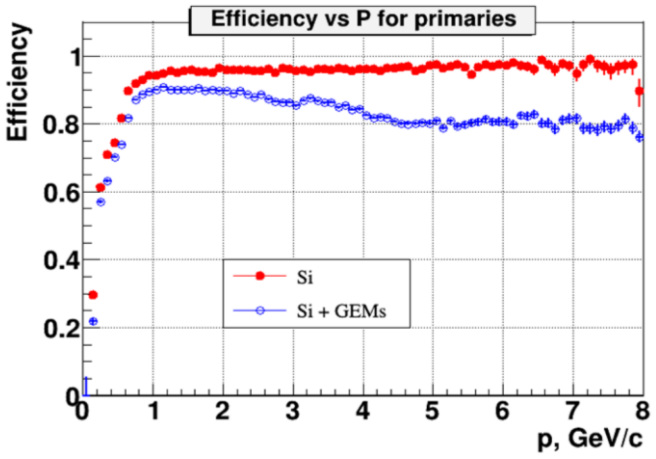
STS team

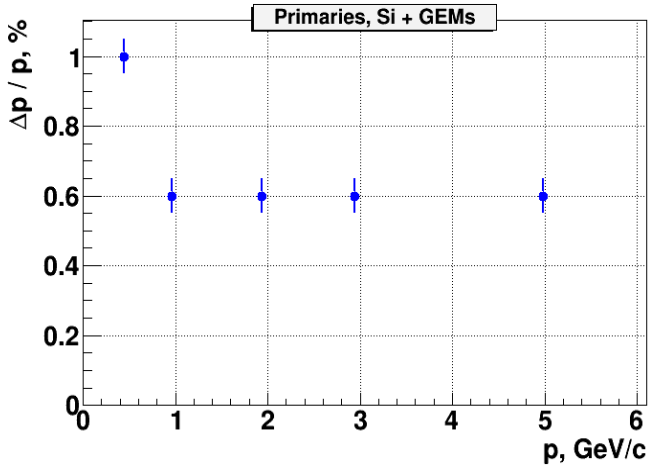
Technical solutions:

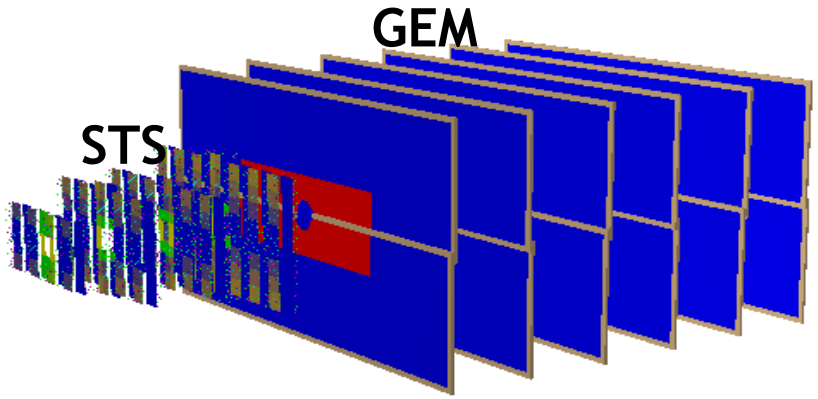
- double-sided silicon microstrip sensors
  - hit spatial resolution ≈ 25 μm
  - material budget per tracking station: ≈ 0.3% - 2% X_0
  - radiation tolerance up to 1 × 10^{14} n/cm^2 (1 MeV equivalent)
- self-triggering front-end electronics, time-stamp resolution ≈ 12,5 ns
- low-mass detector modules/ladders

The project is being implemented as a joint effort of CBM and BM@N STS teams under the GSI-JINR Roadmap Agreement

Performance simulations

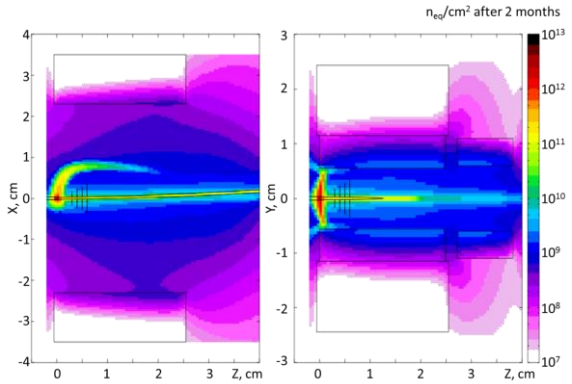




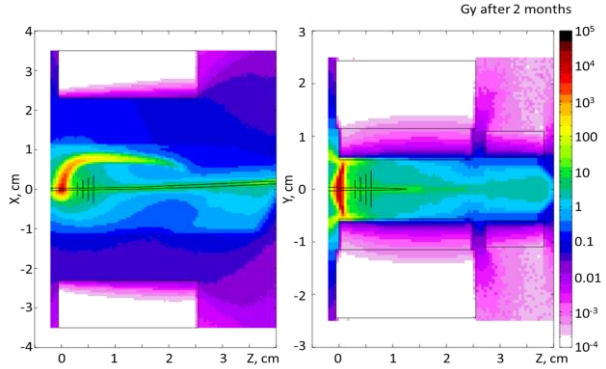


DCM-QGSM model, Au+Au, T_0=4 AGeV

- Eff. >90% for 1 < P < 2.5 GeV/c, 80% for P > 4 GeV/c;
- Δp/p ~ 0.6%



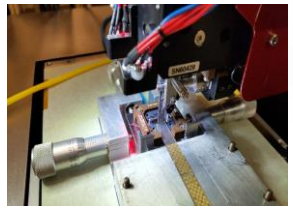
Equivalent neutron fluence n_{eq}/cm^2



Ionizing dose in Gray

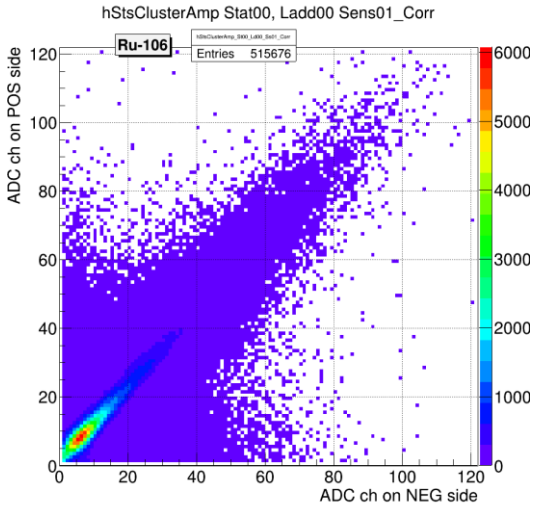
- Ionizing dose ~ 100 Gy/lifetime;
- The equivalent neutron life time fluence of 10^{11} n_{eq}/cm^2

STS Modules



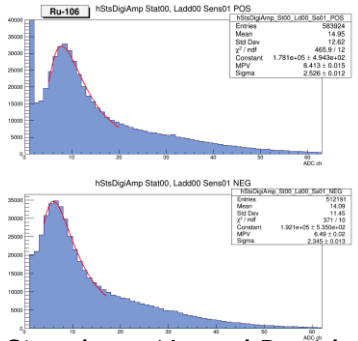
Performance:

- noise: ~700 e^- (N-side);
  ~500 e^- (P-side);
- r/o threshold: ~5000 e^-;
- signal-to-noise: > 25;
- hit detection eff.: > 95%;

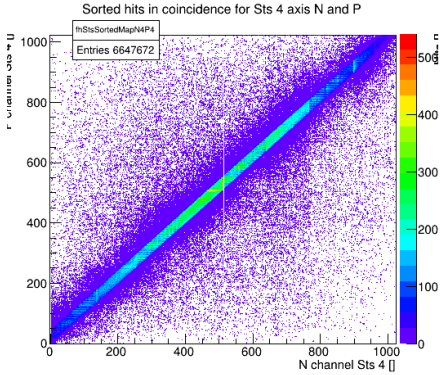


Signals on N- and P- sides

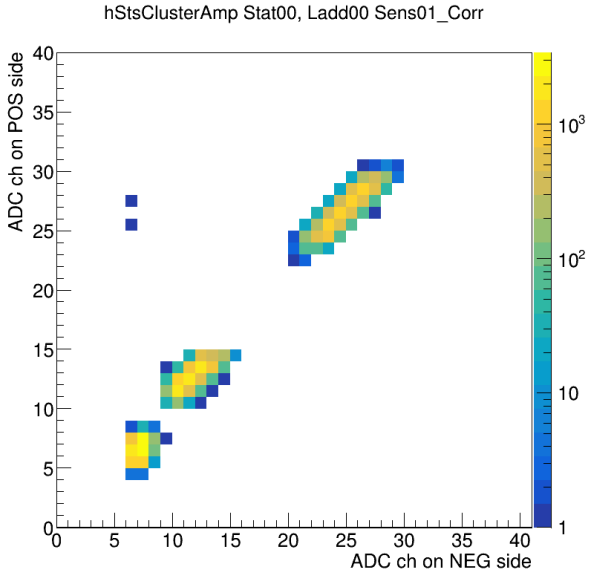
Tests with Ru-106 source



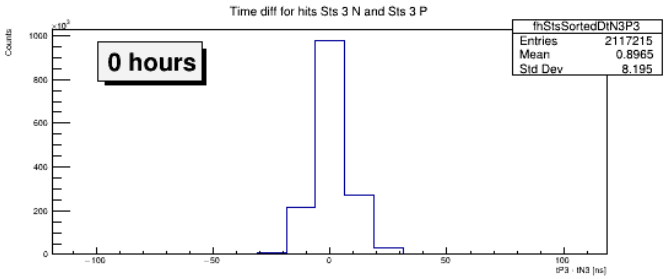
Signals on N- and P- sides

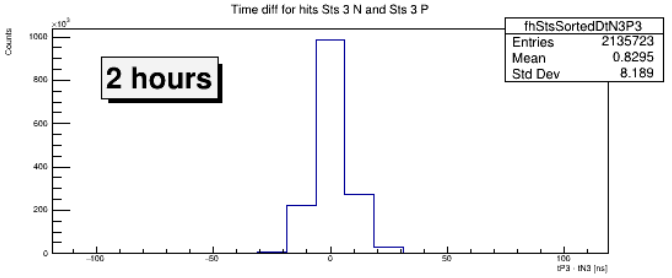


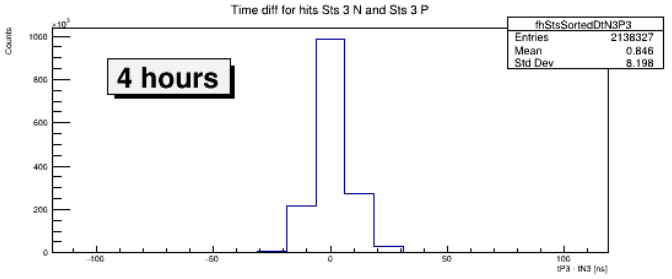
Correlations between N- and P- sides

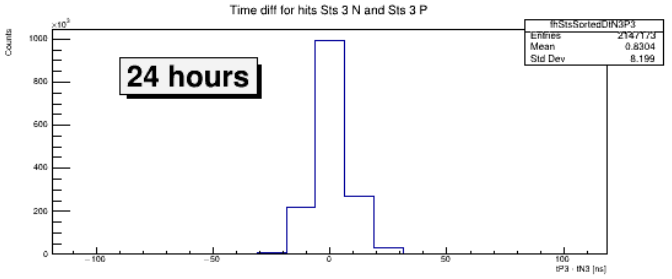


Signals from IR laser pulses
(diff. amplitudes)
On P- and N- sides



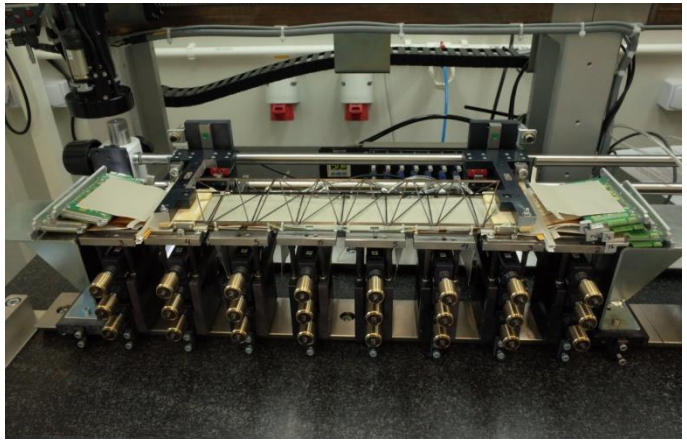


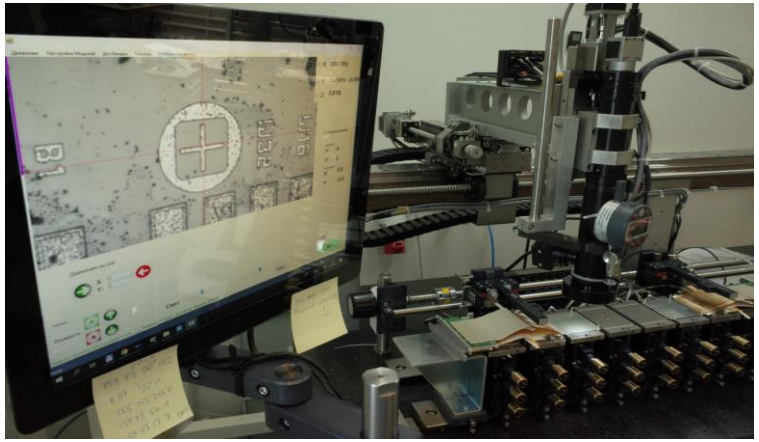


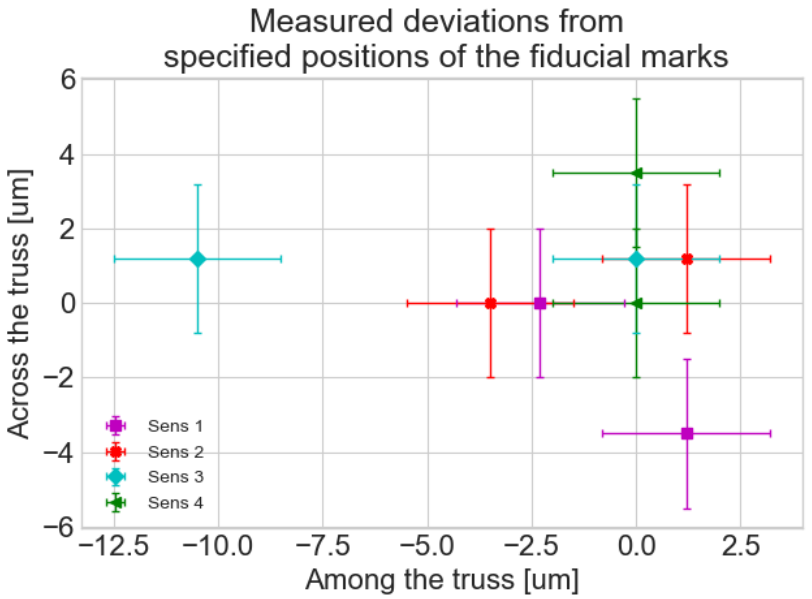


Long term stability test: quality of the time synchronization between ASICs on the P- and N- sides of the module

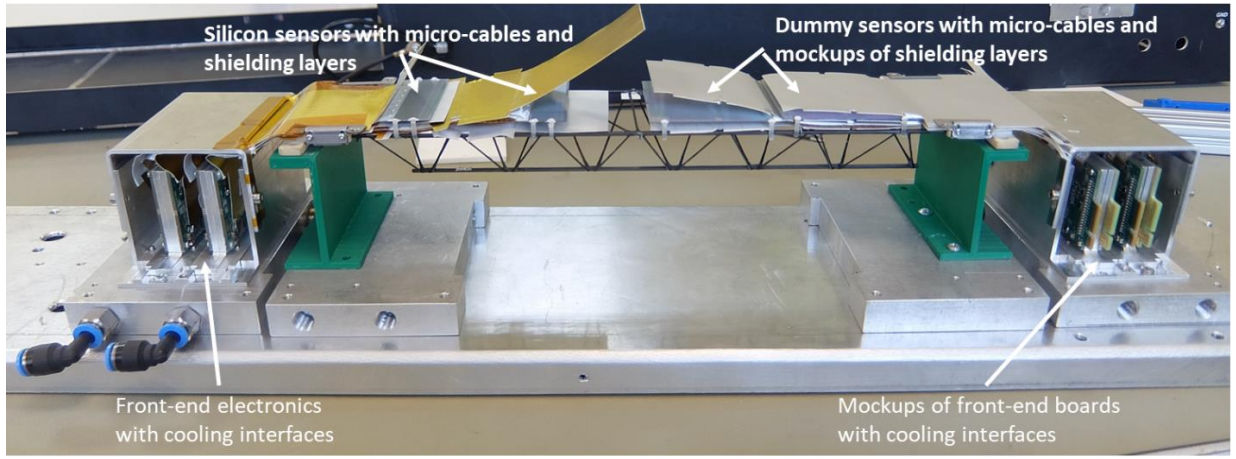
Ladder assembly

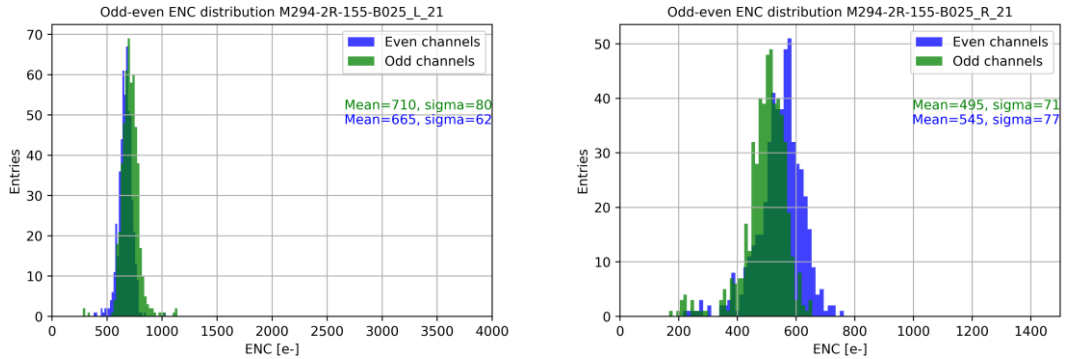






Each sensor has fiducial marks on its surface. Position of each mark is specified for each module on a specific ladder.
Deviation of the measured position of the fiducial from the specified one are shown on the right plot.

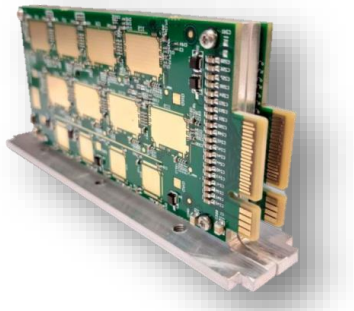


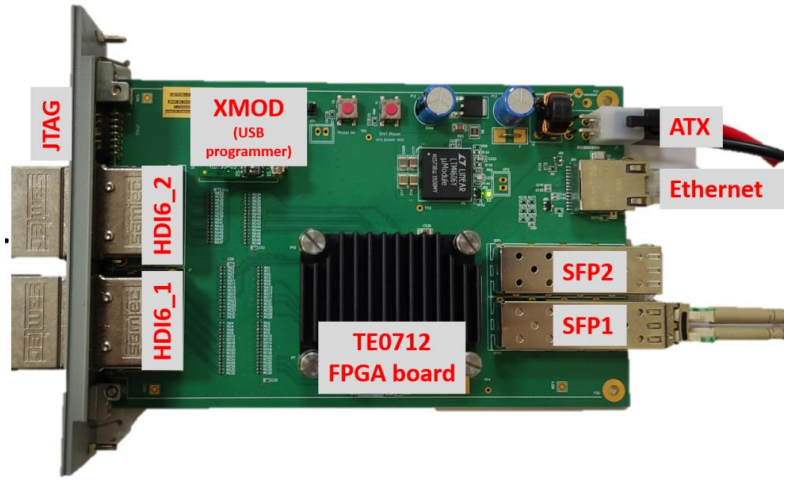


Measured noise per channel distribution for the module on ladder

Signal/Noise > 25

Readout electronics





TFC
Timing and Fast
Control

Computing System

FEB-8
FEE

elinks
2.35 MHit/s/elink

Data,
Synch,
commands

GBTxEMU

FPGA based
emulator of CERN
GBTx
serializer and data
combiner chip
48 x 80 Mbit/s
to 3.84 Gbit/s optical

48 e-links
3 x Sensors

Gbit opt.

Data,
Synch,
commands

GERI-Board
FPGA based
PCIe Interface to
computer system

BM@N
Data center

Thank you for your attention!

Backup slides >>>>