Mass tests of silicon photomultiplier (SiPM) arrays for the TAO experiment

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TAO experiment

Figure 1. JUNO-TAO location

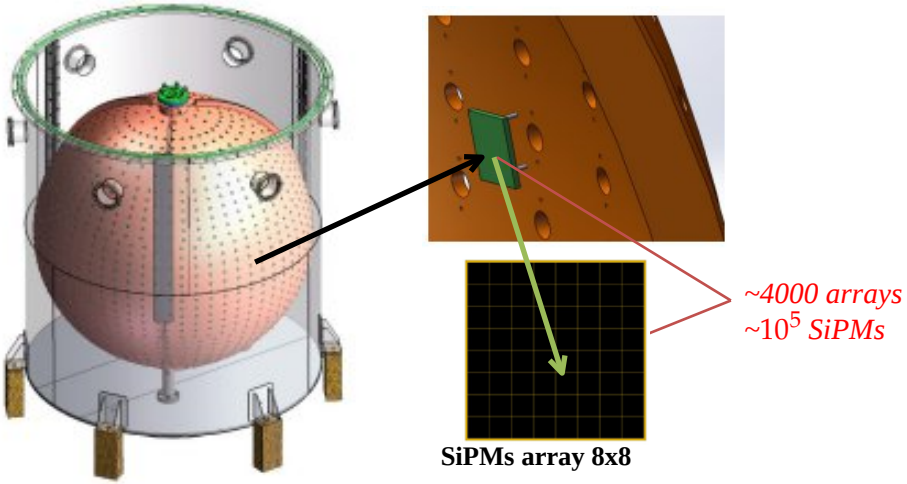


Figure 3. TAO detector design

The main purpose of the TAO experiment is to provide a reference spectrum for JUNO, eliminating the possible model dependence due to fine structure in the reactor antineutrino spectrum in determining the neutrino mass ordering.

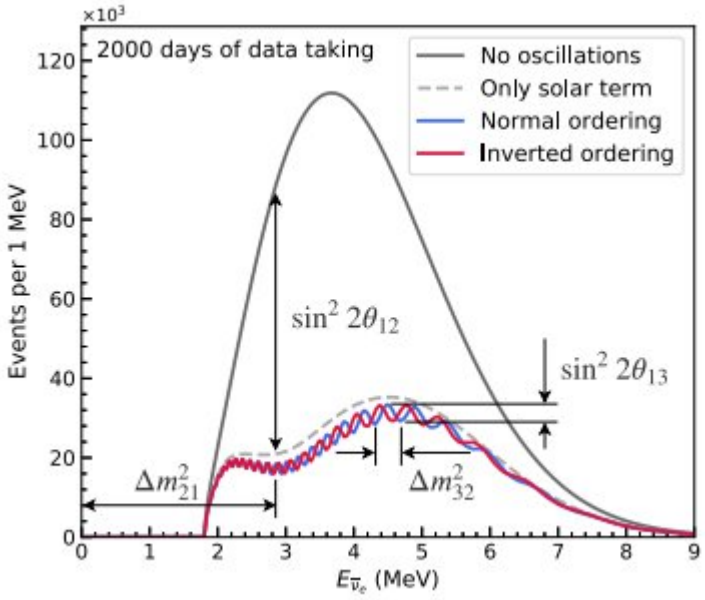


Figure 2. The expected antineutrino energy spectrum weighted by IBD cross-section with and without oscillation at the JUNO experiment for normal ordering and inverted ordering assuming 2000 days of data-taking. Dependence on the four oscillation parameters is shown

Mass tests of SiPM arrays

Parameters	Specification
PDE	≥ 50%
Dark count rate	≤ 100 Hz/mm^2
Probability of correlated noise	≤ 10% (at -50°C)
Uniformity of V_{bd}	≤ 10%
Size of the SiPM device	≥ 6 x 6 mm^2
SiPM coverage within tiles	≤ 94%

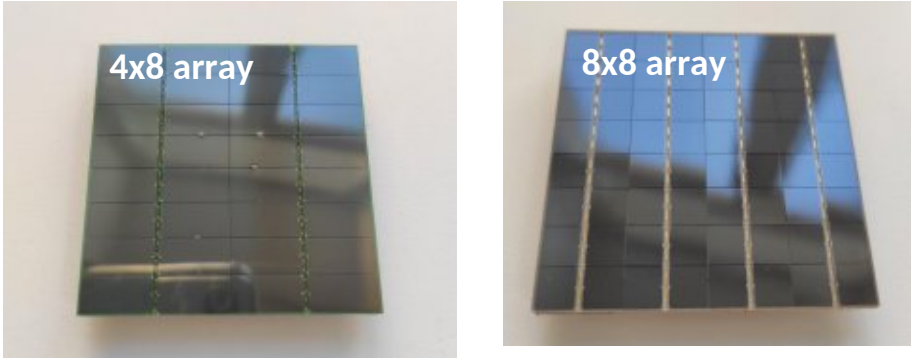
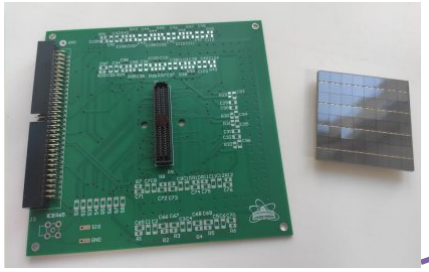


Figure 4. Tile samples

32-channel PCB for 4x8 tile prototype



64-channel PCB for 8x8 tile prototype

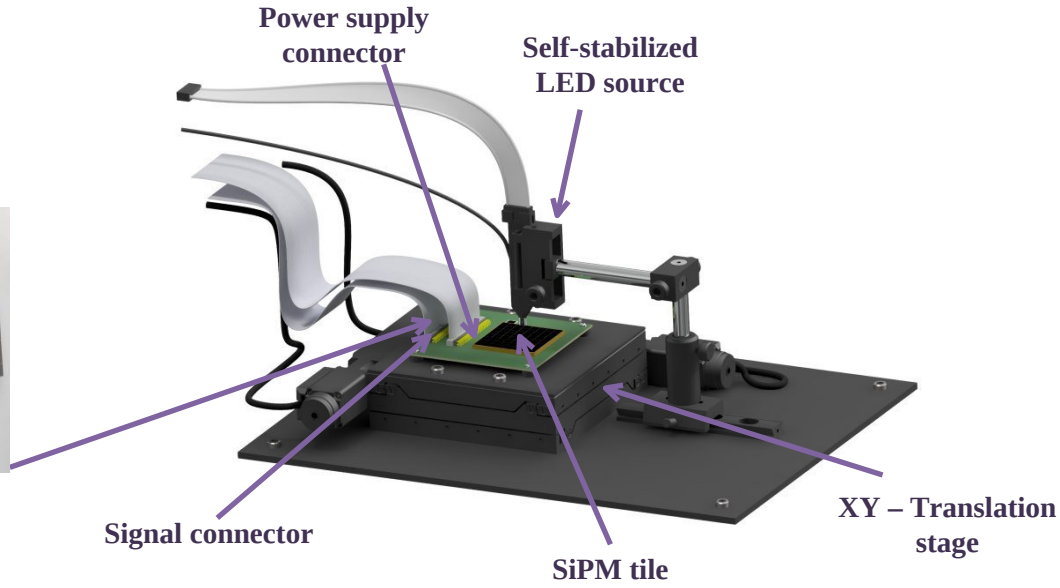


Figure 5. Design of the pre-measurement stand for single SiPM tile studies

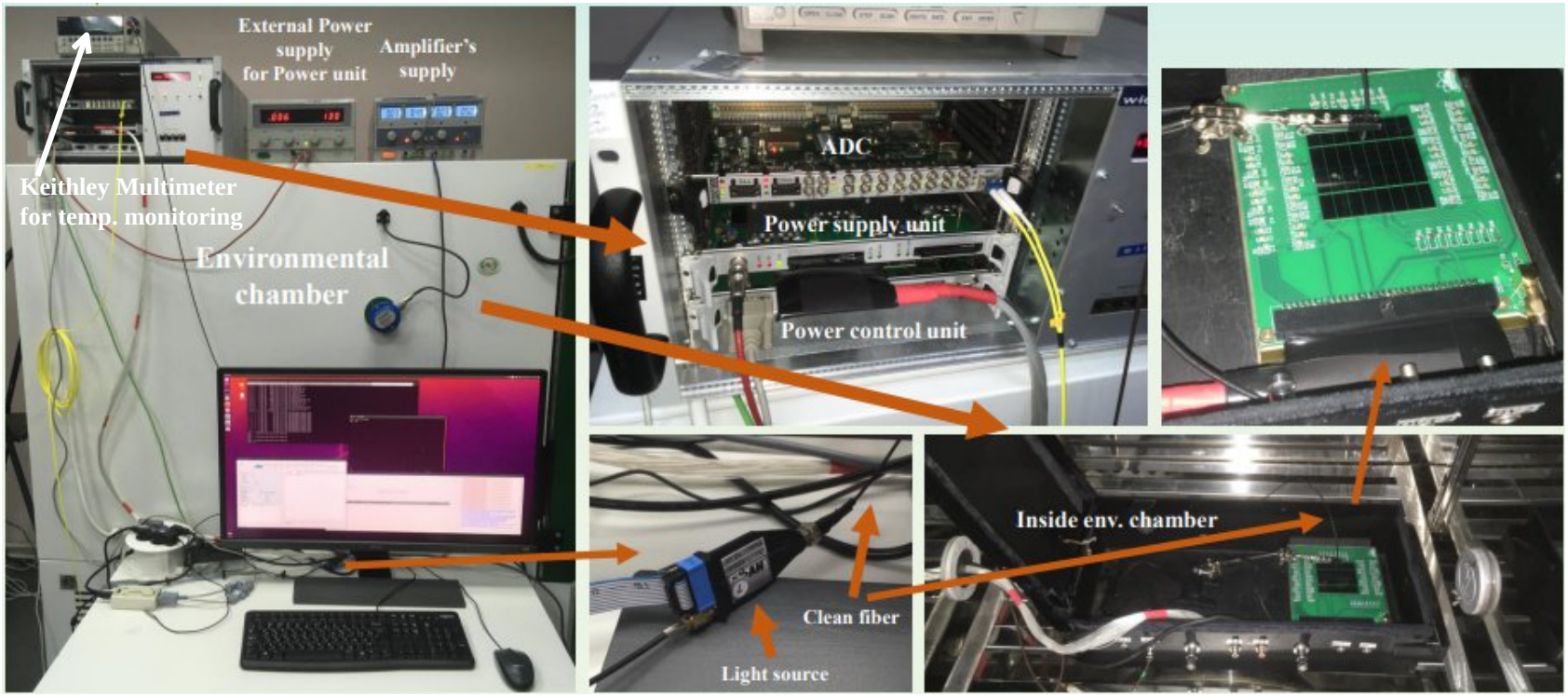


Figure 6. Stand for testing SiPM arrays

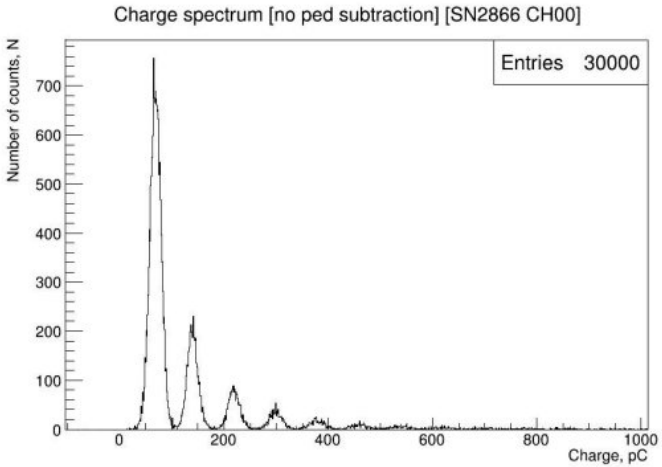


Figure 7. Charge spectrum of SiPM

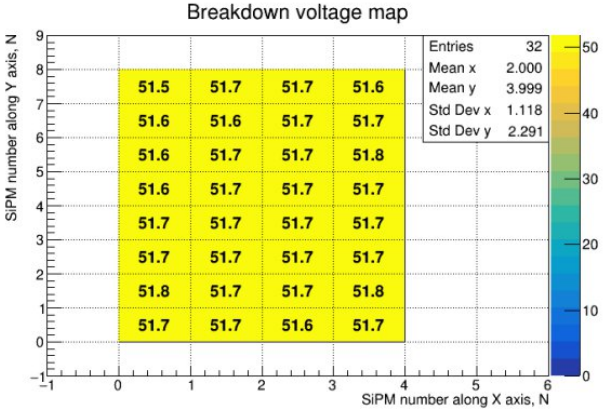


Figure 8. Array breakdown voltage map

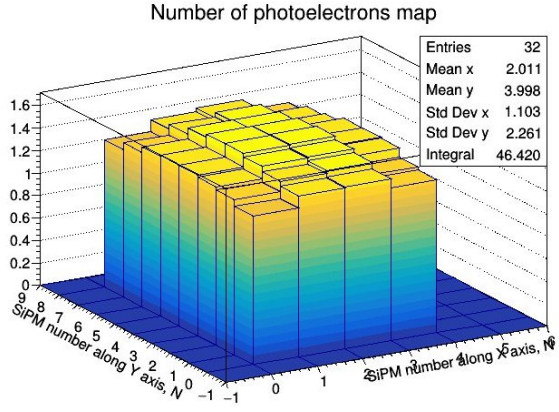


Figure 9. Array photoelectron distribution map

Control and power units

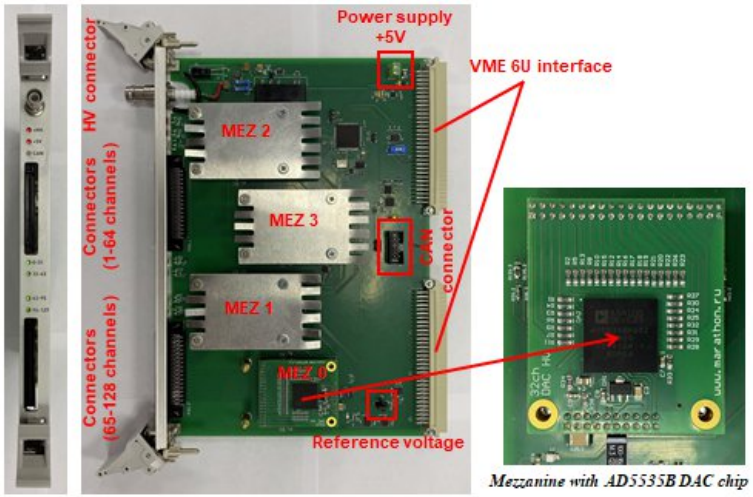


Figure 10. Power unit

Main Features:

- VME mechanics
- 128 channels
- Based on AD5535B chip
- Voltage up to 200 V, 14-bit
- Max current 500 µA/ch
- 1xSHV connector
- 2x68pin IDC connectors
- PCB power supply ±12V, +5V by VME
- CAN-open protocol
- CAN interface on VME bus

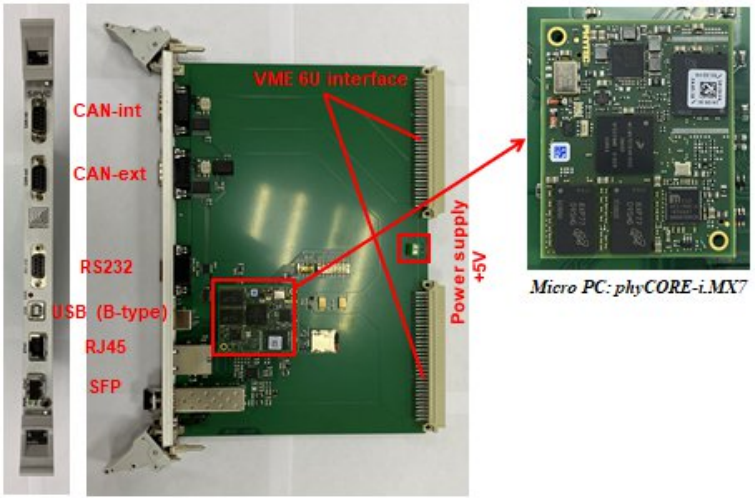


Figure 11. Control unit

Main Features:

- VME mechanics
- Micro PC: phyCORE-i.MX7
- CAN-int, CAN-ext
- 2x connecion interfaces; 1GBPS (SFP) and 100MBPs (RJ45)
- COM port (RS232) and USB (B-type) for direct access to the micro PC
- PCB power supply ±12V, +5V by VME
- CAN-open protocol
- CAN interface on VME bus

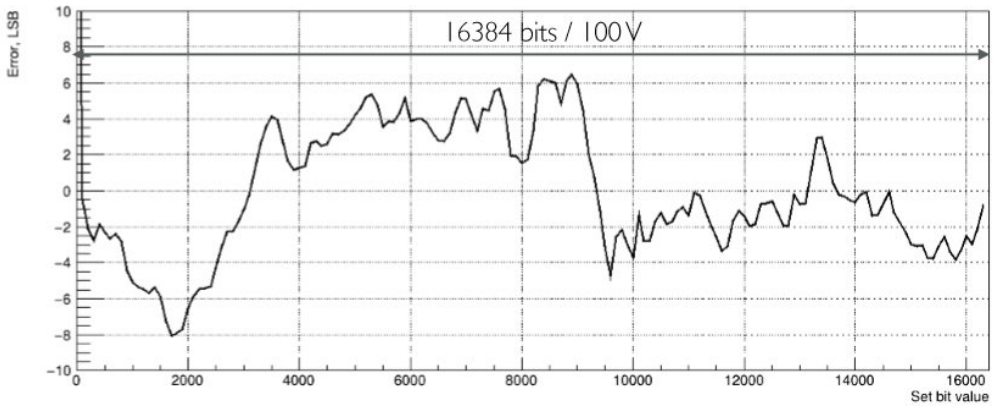


Figure 12. Integral nonlinearity example for single DAC channel

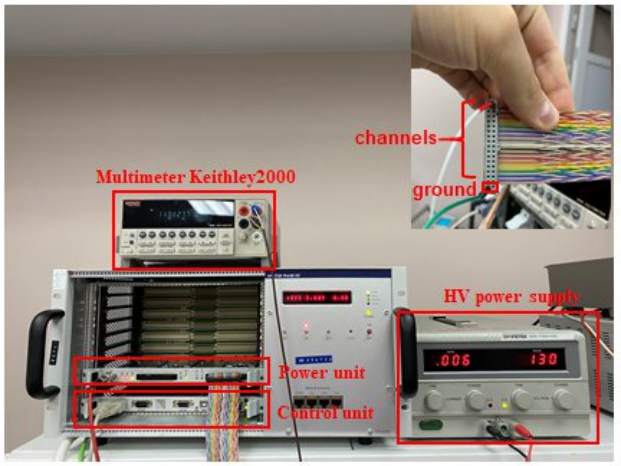


Figure 13. Stand for calibration of power units

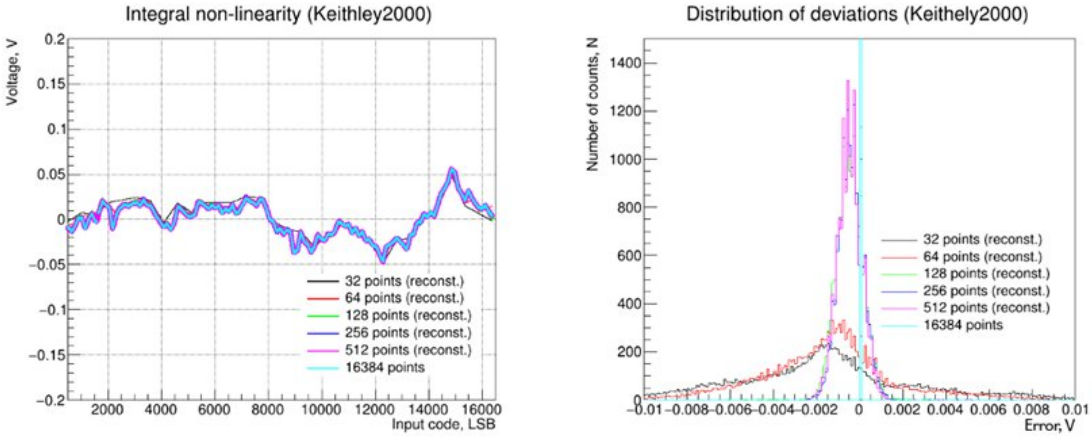


Figure 14. Reconstructed of intermediate points of real data using the spline algorithm

- Over 128 points must be acquired for calibration of a single channel;
- time: ~10 min/128 points is required;
- 128ch*10min ~ 20h/Power Unit;
- Switching channels in automatic mode is needed (multiplexer).

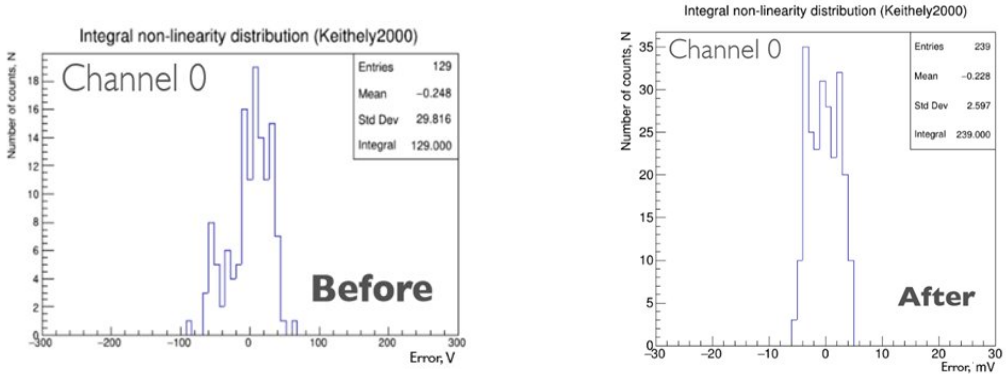


Figure 15. The results of setting the voltage on the channel: a) without calibration; b) with calibration

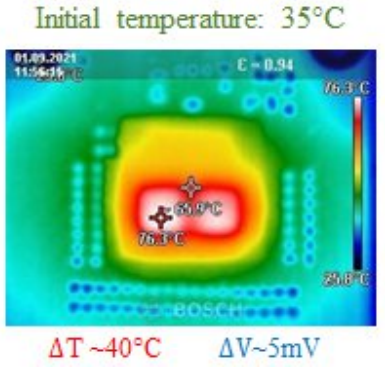


Figure 16. Chip temperature stability