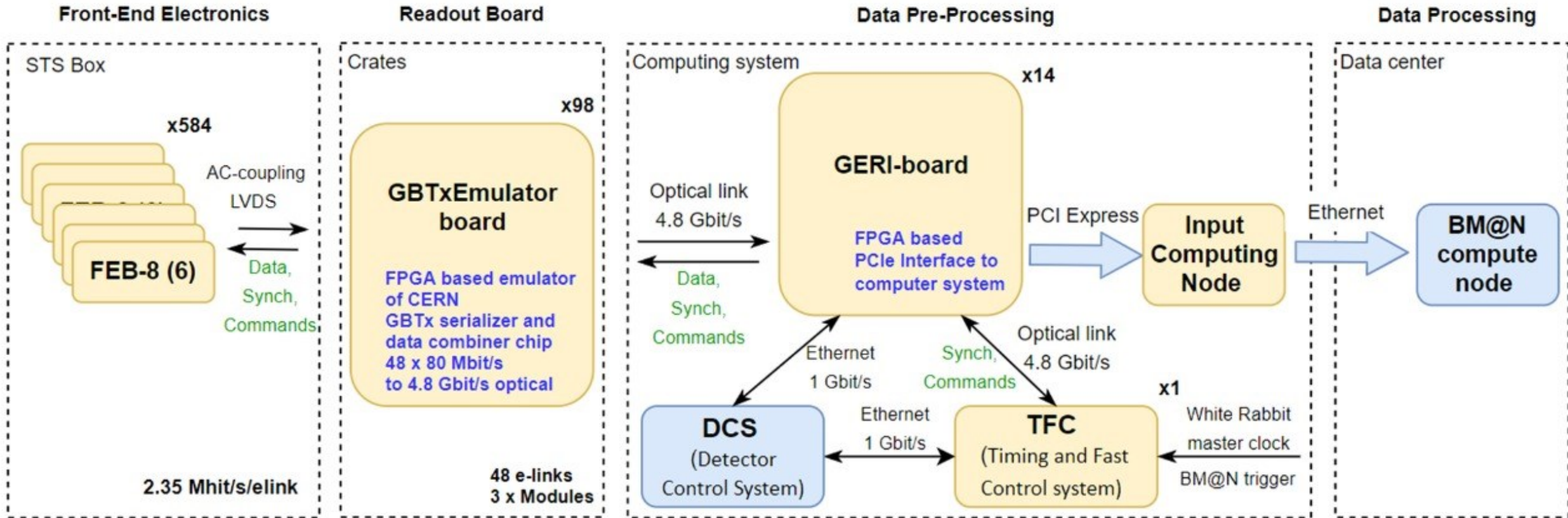


Tasks related to the integration of the Timing and Fast Control system (TFC) in the **BM@N** readout chain.

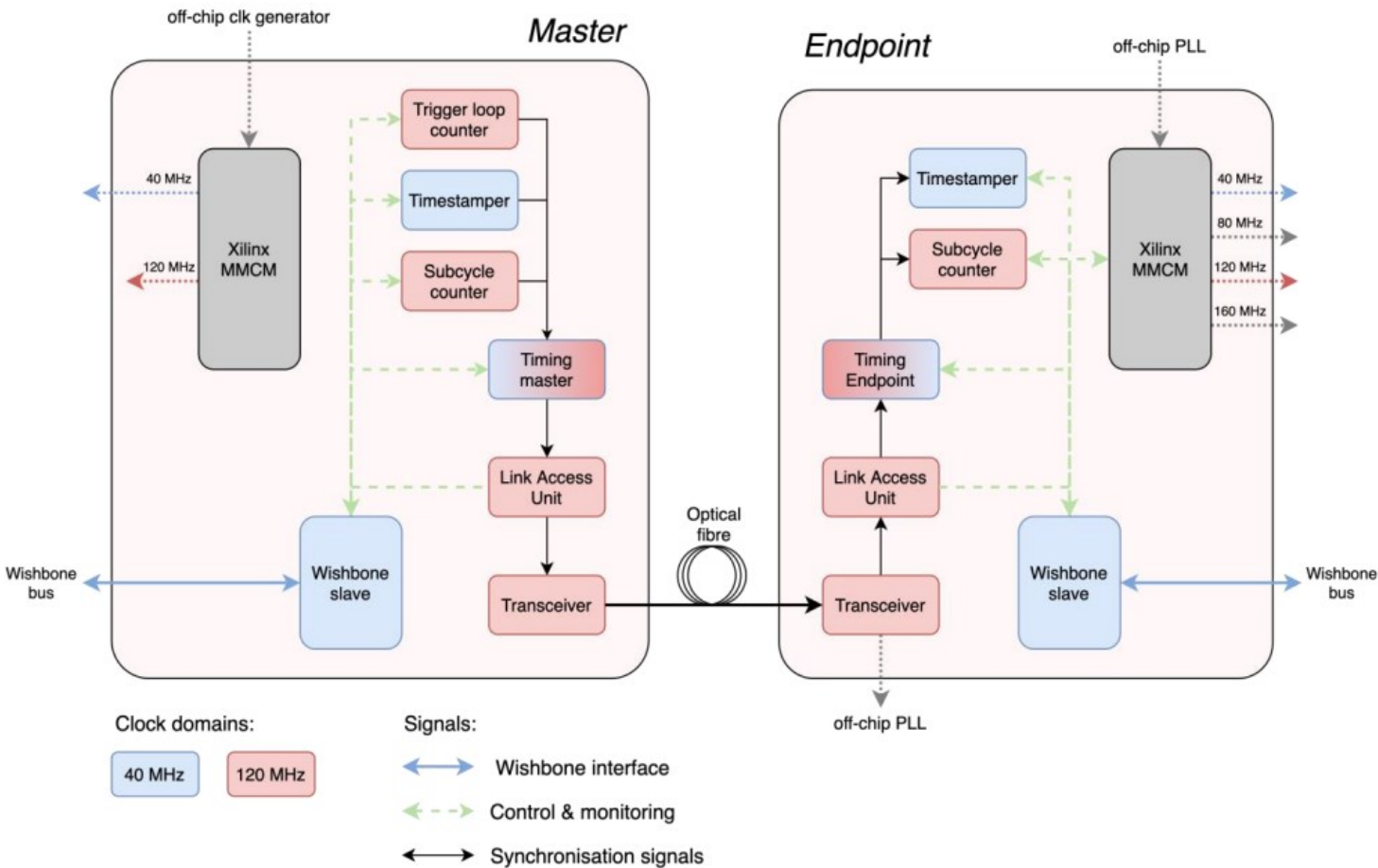


- 1. Selection of the hardware platform for the TFC.**
- 2. Implement the basic control interface based on the IPBus protocol.**
- 3. Implement a solution to synchronize the system to the Clock and Timing Network.**
- 4. Assembly and testing procedure LDO v2.1 at JINR lab.**



- 1. Selection of the hardware platform for the TFC.**

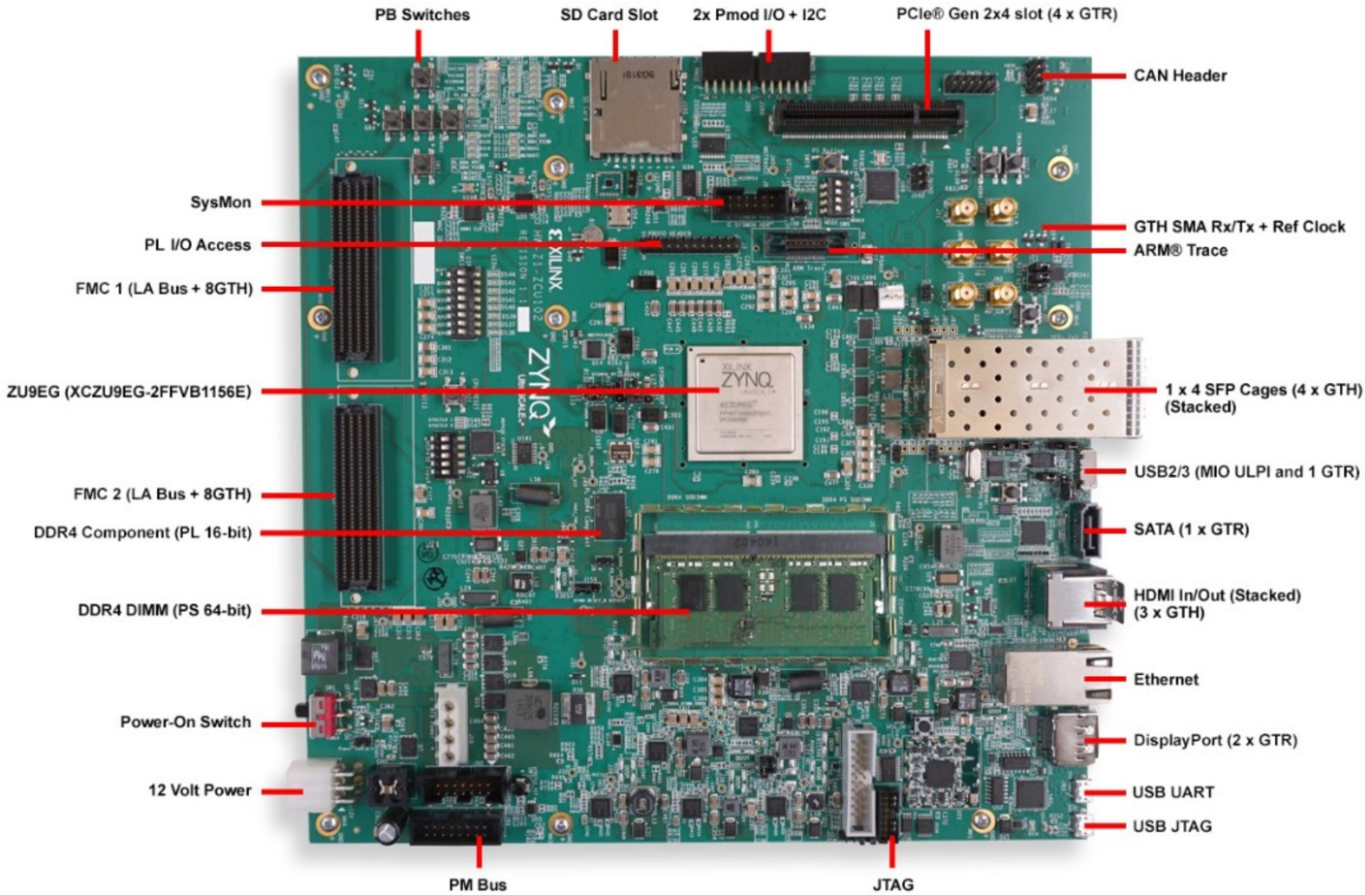
Architecture of Master and Endpoint TFC cores.



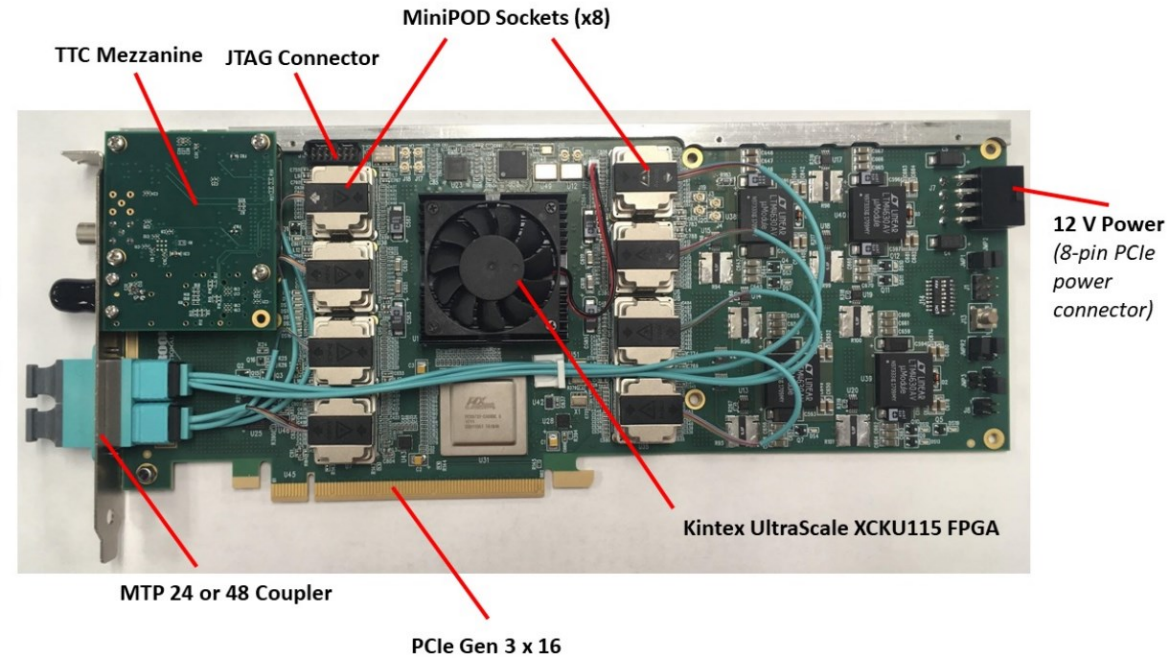
- Platform board: BNL-712
- Mezzanine cards:
- Master - WR TMC
- Endpoint - TTC-PON TMC

https://indico.cern.ch/event/1019078/contributions/4444397/attachments/2312299/3935290/twepp_sidorenko.pdf

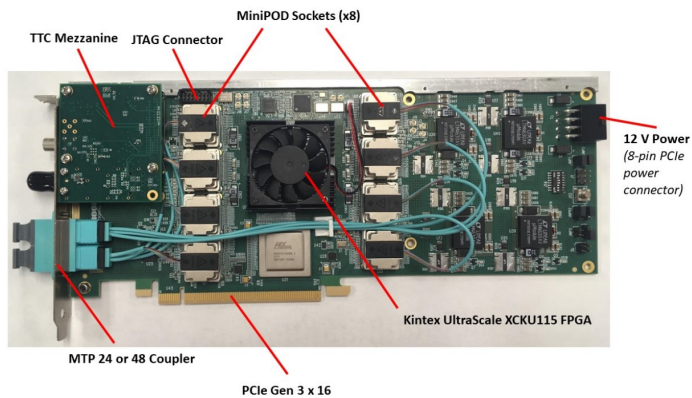
ZCU102 Evaluation Kit



BNL-712 board



BNL-712 board



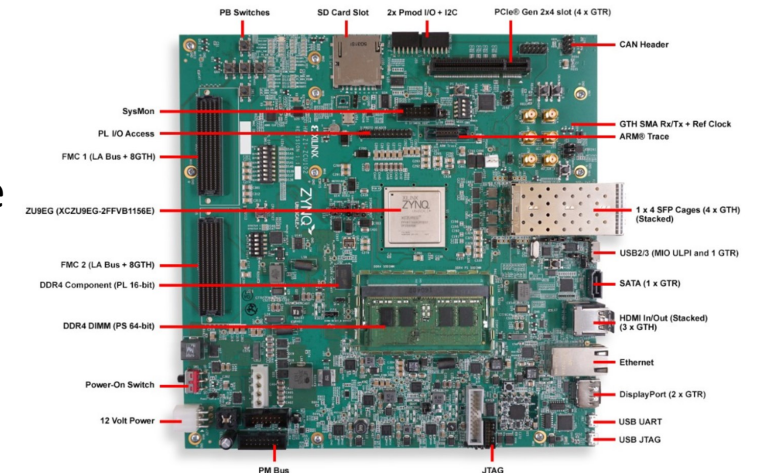
- Interactive operation from Python console
- AGWB-base Wishbone infrastructure
- Firmware develop base on fusesoc tool

- PICE + Wishbone register access
- GTH Ultrascale transceivers

CBM TFC-master repository :

https://git.cbm.gsi.de/daq/fpga-firmware/tfc/cri-tfc/-/tree/tfc_devel/projects/tfc2_master

ZCU102 Evaluation Kit

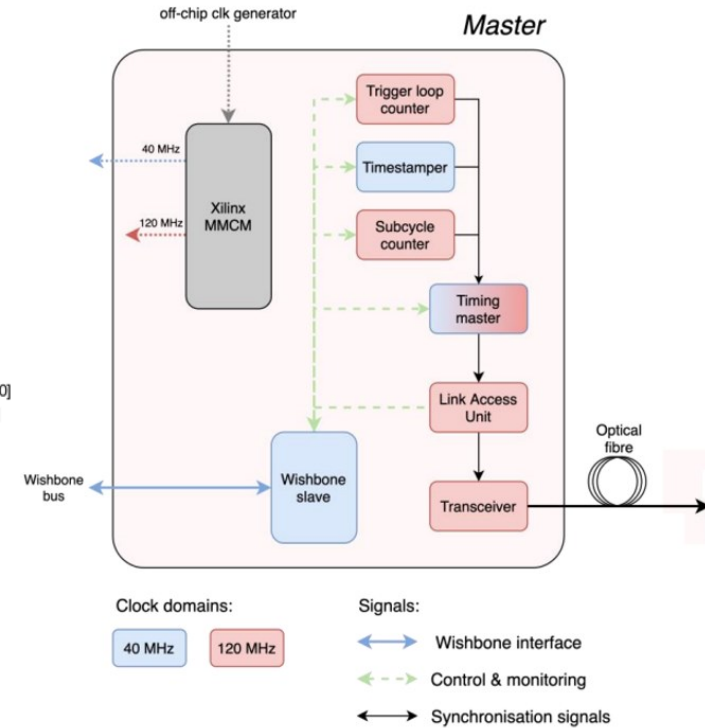
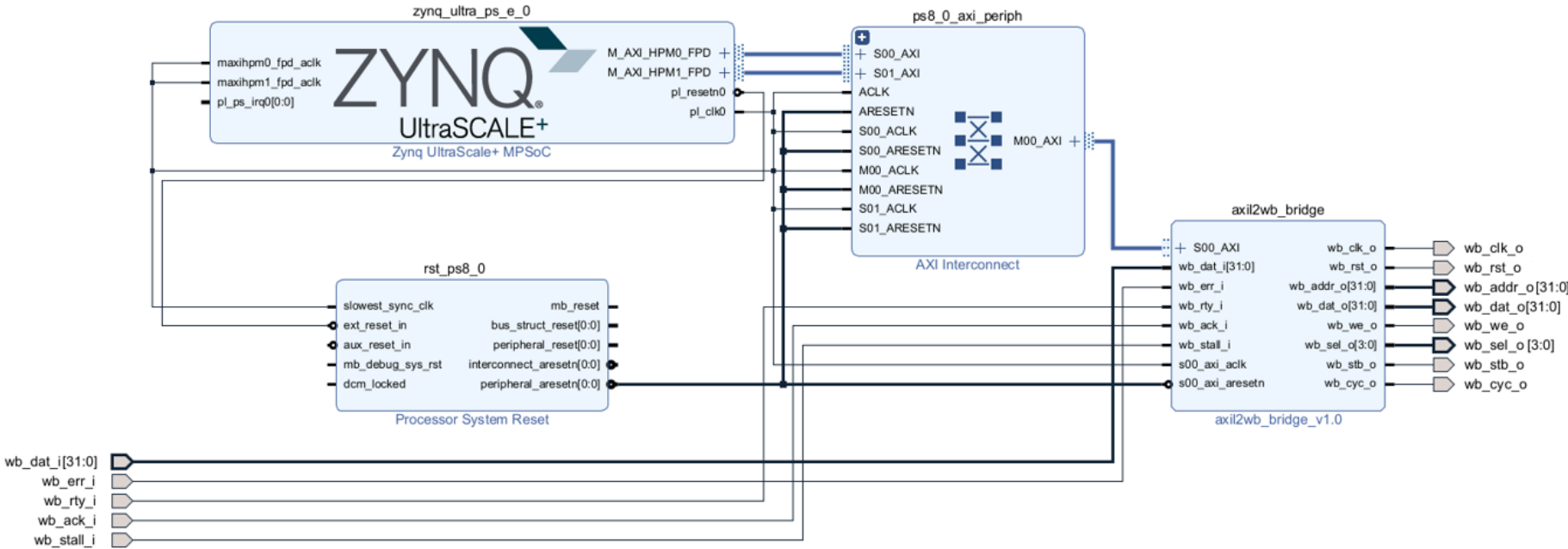


- Zynq + Wishbone register access
- GTH Ultrascale+ transceivers

- 2. Implement the basic control interface, based on the IPBus protocol.**

Zynq + AXIL to Wishbone bridge.

Architecture of Master TFC core.



The FreeRTOS LwIP UDP IPBus Server application creates a UDP server to provide connections to IPBus client running on host machine. Once the remote client connects with this server, the UDP server will start decoding data from client according to the IPbus 2.0 protocol.

```
root@DESKTOP-3VN27K1:/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb
[root@DESKTOP-3VN27K1 fusesoc-bd-axil2wb]# python test_ipbus_example.py
16-01-22 20:20:55.525563 [139783302940480] INFO - Reading XML address file "/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb/ipbus_example.xml"
16-01-22 20:20:55.526176 [139783302940480] INFO - ConnectionManager created node tree:
+ Node "", Address 0x00000000, Module "/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb/ipbus_example.xml"
+ Node "ID", SINGLE register, Address 0x00004000, Mask 0xFFFFFFFF, Permissions r-, Module "/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb/ipbus_example.xml"
+ Node "VER", SINGLE register, Address 0x00004001, Mask 0xFFFFFFFF, Permissions r-, Module "/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb/ipbus_example.xml"
+ Node "TEST_RW", SINGLE register, Address 0x00004004, Mask 0xFFFFFFFF, Permissions rw, Module "/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb/ipbus_example.xml"
+ Node "TEST_WO", SINGLE register, Address 0x00004005, Mask 0xFFFFFFFF, Permissions rw, Module "/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb/ipbus_example.xml"
+ Node "TEST_RO", SINGLE register, Address 0x00004006, Mask 0xFFFFFFFF, Permissions rw, Module "/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb/ipbus_example.xml"
+ Node "TEST_TOUT", SINGLE register, Address 0x00004007, Mask 0xFFFFFFFF, Permissions rw, Module "/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb/ipbus_example.xml"
+ Node "freq_mon_0", SINGLE register, Address 0x00004008, Mask 0xFFFFFFFF, Permissions r-, Module "/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb/ipbus_example.xml"
+ Node "freq_mon_1", SINGLE register, Address 0x00004009, Mask 0xFFFFFFFF, Permissions r-, Module "/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb/ipbus_example.xml"
+ Node "freq_mon_2", SINGLE register, Address 0x0000400A, Mask 0xFFFFFFFF, Permissions r-, Module "/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb/ipbus_example.xml"
+ Node "timestamp_l", SINGLE register, Address 0x00004011, Mask 0xFFFFFFFF, Permissions r-, Module "/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb/ipbus_example.xml"
+ Node "timestamp_h", SINGLE register, Address 0x00004012, Mask 0xFFFFFFFF, Permissions r-, Module "/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb/ipbus_example.xml"
+ Node "tstamp_corr_l", SINGLE register, Address 0x00004013, Mask 0xFFFFFFFF, Permissions rw, Module "/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb/ipbus_example.xml"
+ Node "tstamp_corr_h", SINGLE register, Address 0x00004014, Mask 0xFFFFFFFF, Permissions rw, Module "/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb/ipbus_example.xml"
+ Node "sync_period", SINGLE register, Address 0x00004015, Mask 0xFFFFFFFF, Permissions rw, Module "/mnt/d/work/vivado_proj/ZCU102/fusesoc-bd-axil2wb/ipbus_example.xml"
16-01-22 20:20:55.527969 [139783302940480] INFO - URI "ipbusudp-2.0://192.168.1.10:50001" parsed as:
> protocol : ipbusudp-2.0
> hostname : 192.168.1.10
> port : 50001
> path :
> extension :
> arguments :

Getting REGISTER-ID
REGISTER-ID : 0x1ed91fca

Getting REGISTER-VER
REGISTER-VER : 0xc7a36906

Getting REGISTER-freq_mon_0
REGISTER-freq_mon_0 : 119956559

Getting REGISTER-freq_mon_1
REGISTER-freq_mon_1 : 119956559

Getting REGISTER-freq_mon_2
REGISTER-freq_mon_2 : 12000643

Setting REGISTER-TEST_RW = 0x10
REGISTER-TEST_RW : 0x10

[root@DESKTOP-3VN27K1 fusesoc-bd-axil2wb]#
```

5 Commits 1 Branch 0 Tags 399 KB Files 399 KB Storage

This project implements an IPBus UDP server for zynq ultracale+ ps, through a 1000 Mbps ethernet interface. The current implementation runs on the ZCU102 evaluation board and the IPbus 2.0 protocol is decoded and processed by FreeRTOS based software

Auto DevOps
It will automatically build, test, and deploy your application based on a predefined CI/CD configuration.
Learn more in the Auto DevOps documentation
Enable in settings

master zcu102-tfc-master / + History Find file Web IDE Clone

Update README.txt
Raul Arteche Diaz authored 1 week ago 1dc1a878

Upload File README Add LICENSE Add CHANGELOG Add CONTRIBUTING Add Kubernetes cluster
Set up CI/CD Configure Integrations

Name	Last commit	Last update
fusesoc_cores/bd/readout_stb	Initial commit	1 week ago
src	Update README.txt	1 week ago
submodules	update submodules path	1 week ago
tcl	Initial commit	1 week ago
.gitattributes	Initial commit	1 week ago
.gitignore	Initial commit	1 week ago

<https://git.jinr.ru/v.sidorenko/zcu102-tfc-master>

3. Implement a solution to synchronize the system to the Clock and Timing Network.



WHITE RABBIT LEN WR-LEN

It is the competitive WR alternative capable of supporting **daisy chain** configurations. It allows a cost effective solution to distribute **PPS/10MHz** signals or **IRIG-B** protocol to your equipment.

The WR-LEN is also available in its OEM version in order to integrate accurate timing synchronization into your product.

Optional: 2xμ-DB9 connector for PPSs & 10MHz fan-out or configurable output triggers.



(+34) 958 285 024
C/ Periodista Rafael Gómez Montero, 2
Oficina 13 - Edif. CETIC
18014 Granada, SPAIN.

Technical Specifications / WR-LEN

Management ports	
10/100/1000 ETH	Ethernet copper to fiber links data retransmission, node management
USB-UART	ToD, management
Software	
CLI	Command line interface for configuration and status information
Timing protocols/interfaces	
PTPv2 /White-Rabbit	Dual optical fiber Ethernet 1G interfaces
IRIG-B / PPS I/O	Digital LVTTTL (3.3V). Selectable operation
Frequency I/O	10 MHz programmable input/output

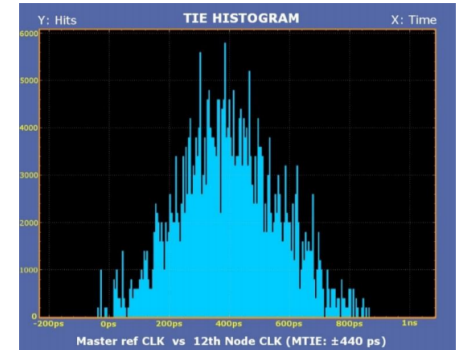
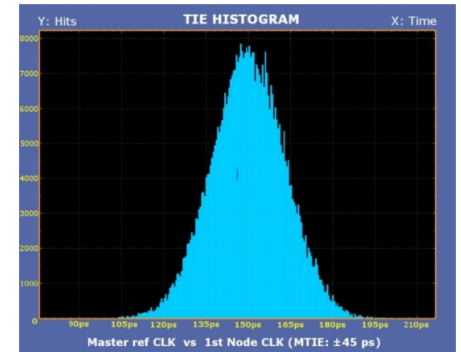
Certifications	
Product	RoHS, FCC, CE, SE
Others	ISO-9001, ISO-14001
Physical Specification	
Dimension	54 x 105 x 135 mm
Color	Black (Metallic)
Power supply	
Voltage, current and power	5V DC, 1.5A - 7.5W max
Environmental Conditions	
Temperature	-10°C ~ +50°C
Humidity	0% ~ 90% RH
Under request extras	
2 x μDB9 connectors + converters to SMA	PPSs & 10MHz fanout or Configurable output triggers

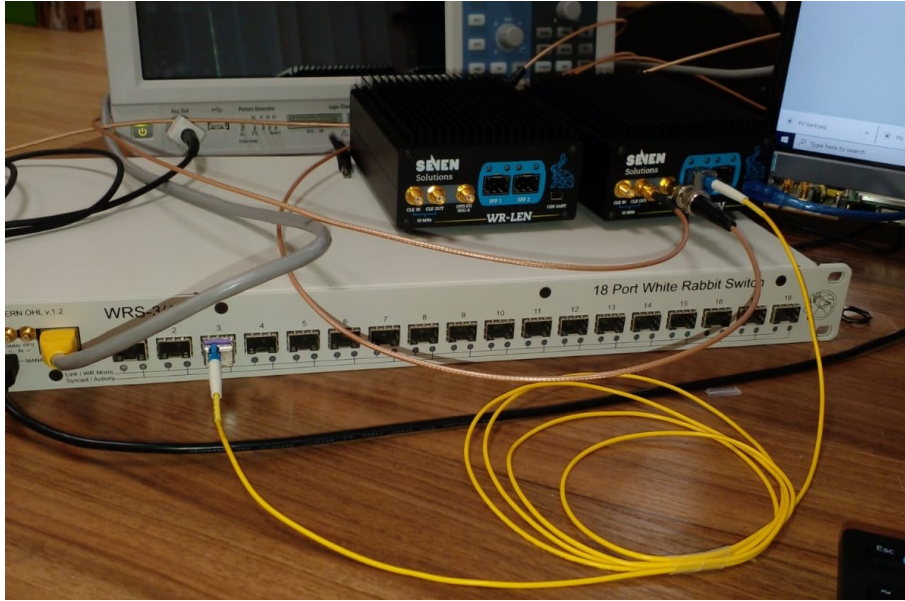


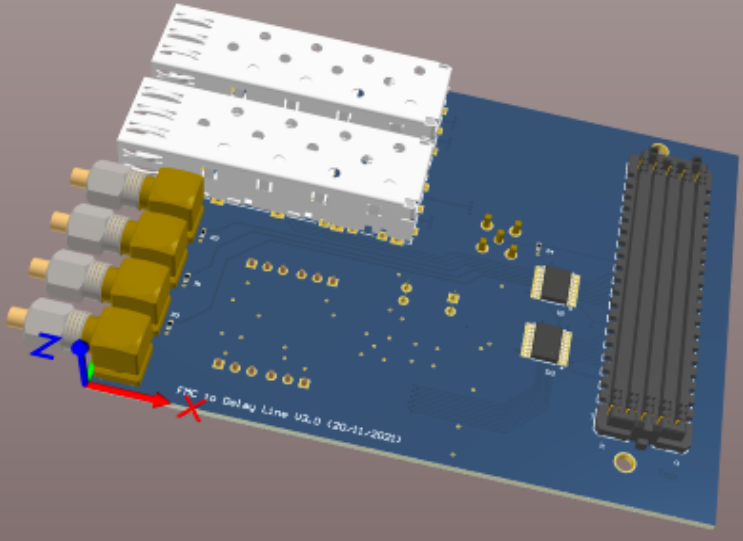
HIGHLIGHTS
✓ Sub-nanosecond time accuracy
✓ Compact size
✓ Distance range: over 80 km using fiber
✓ Dynamic calibration
✓ Cost effective
✓ Time and frequency distribution
✓ Optional fan-out of PPS/10MHz

* Available in its OEM version!

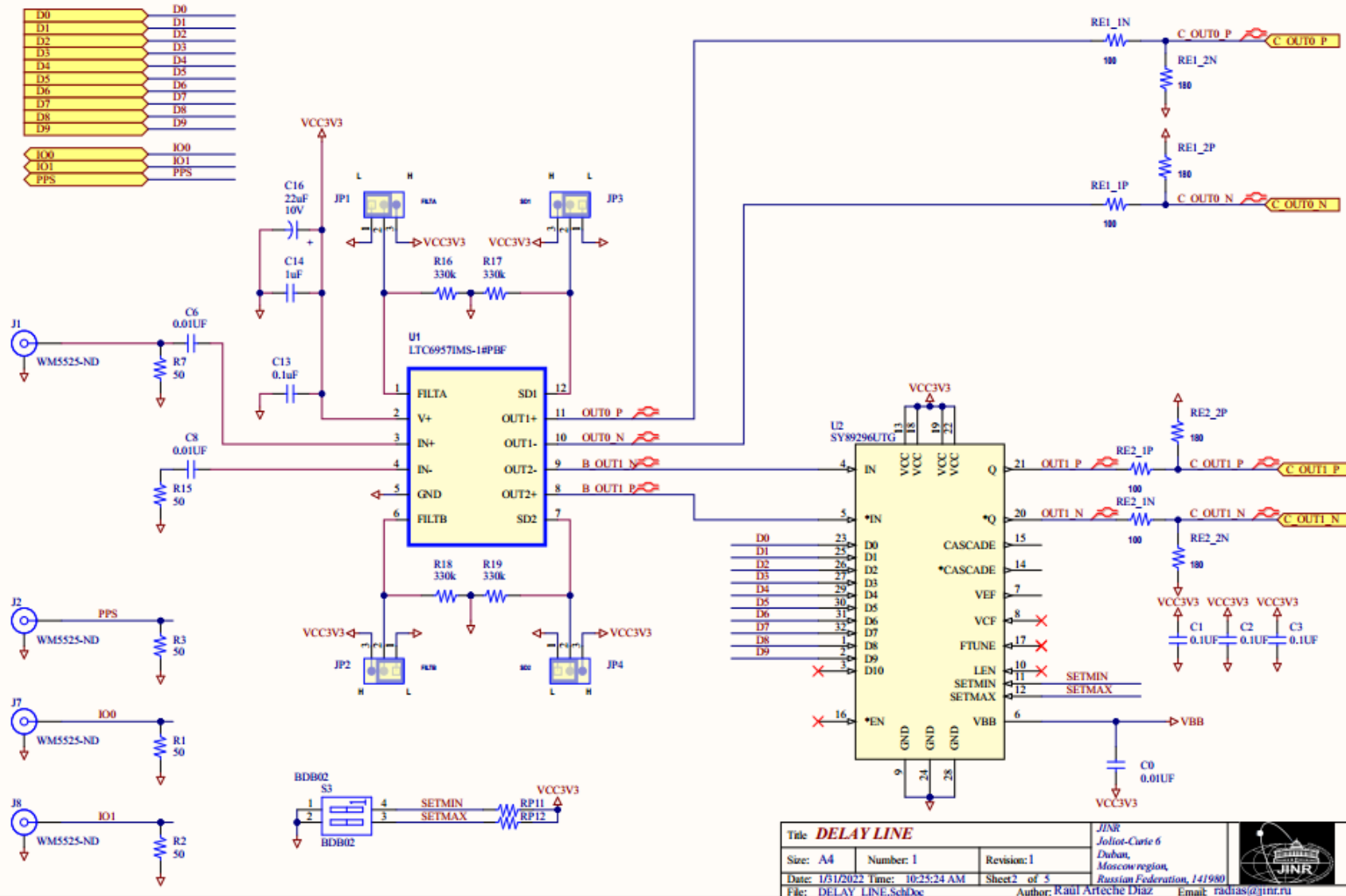
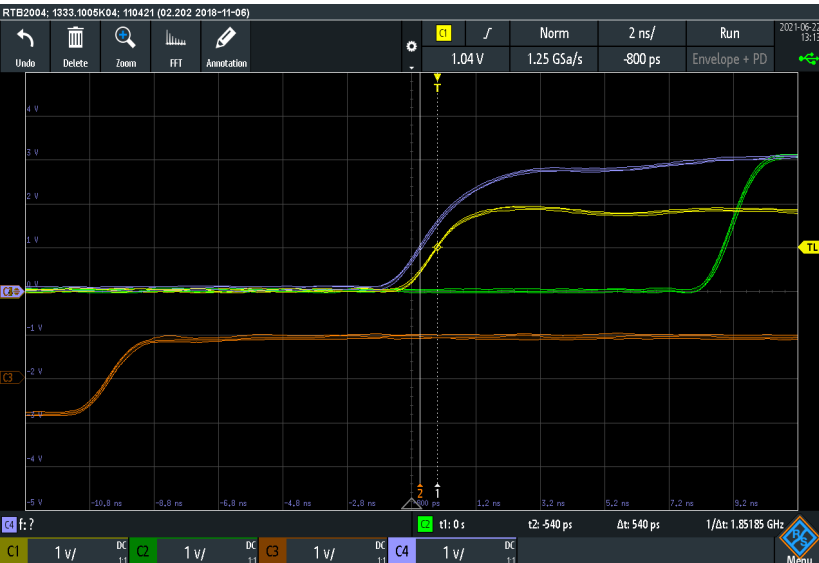
Master reference clock (10MHz) vs Nodes Clock (10 MHz) in a daisy chain configuration







wr_clk delay range 3.2ns to 14.8ns in 10ps increments



4. Assembly and testing procedure LDO v2.1 at JINR lab.

KEITHLEY 2380-500-15 DC ELECTRONIC LOAD (BM&N LDO test program)

VISA resource name: KEITHLEY-2380

Function: FEB-# P001, Enable Output (0:OFF) ON

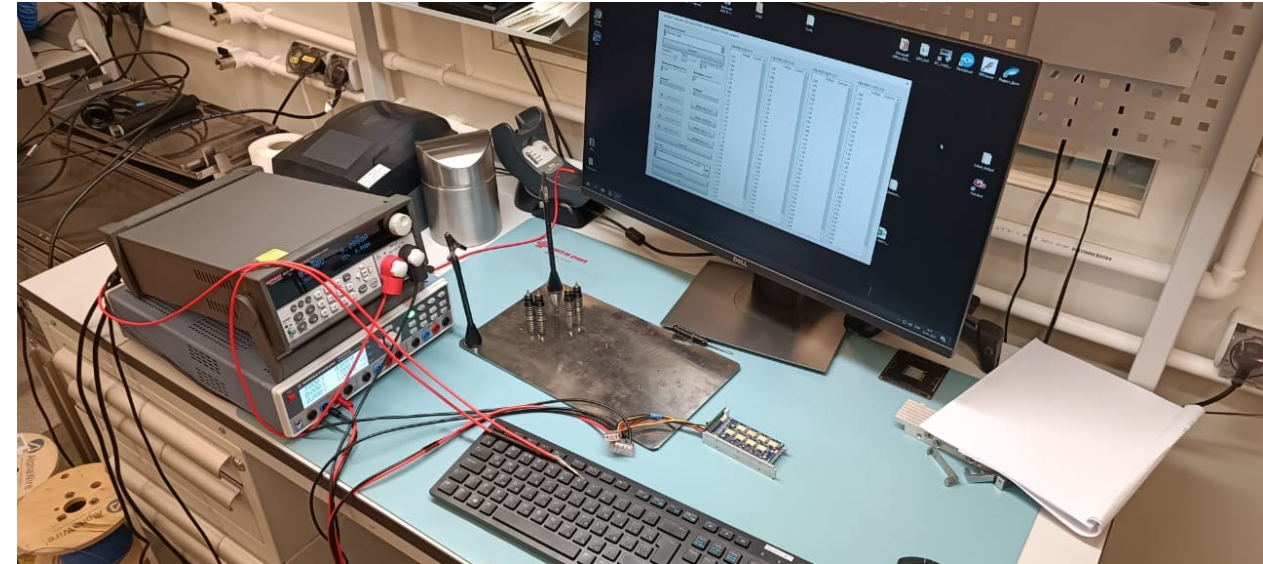
Resistance Range (ohm): 1500, Resistance (ohm): 2

Current?: 0, Voltage?: 0

Buttons: REC LDO1.8-T, ERASE LDO1.8-T, REC LDO1.8-B, ERASE LDO1.8-B, REC LDO1.2-T, ERASE LDO1.2-T, REC LDO1.2-B, ERASE LDO1.2-B, Erase All, Save, Exit

save path: E:\JINR.Disk\STS Module Assembly\LDO_test\tt

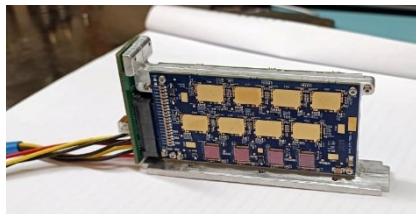
FEB-P001-LDO1.8-T			FEB-P001-LDO1.8-B			FEB-P001-LDO1.2-T			FEB-P001-LDO1.2-B		
Voltaje	Current		Voltaje	Current		Voltaje	Current		Voltaje	Current	
2,00	1,8093	0,8822	2,00	1,8063	0,8808	2,00	1,2281	0,5988	2,00	1,2277	0,5985
1,95	1,8095	0,8822	1,95	1,8065	0,8809	1,95	1,2286	0,5990	1,95	1,2277	0,5985
1,90	1,8099	0,9047	1,90	1,8065	0,9030	1,90	1,2287	0,6125	1,90	1,2277	0,6158
1,85	1,8101	0,9280	1,85	1,8065	0,9229	1,85	1,2290	0,6302	1,85	1,2275	0,6291
1,80	1,8099	0,9549	1,80	1,8065	0,9505	1,80	1,2290	0,6464	1,80	1,2273	0,6498
1,75	1,8099	0,9778	1,75	1,8063	0,9750	1,75	1,2287	0,6659	1,75	1,2273	0,6631
1,70	1,8093	1,0104	1,70	1,8059	1,0047	1,70	1,2286	0,6821	1,70	1,2269	0,6879
1,65	1,8093	1,0334	1,65	1,8059	1,0315	1,65	1,2279	0,7056	1,65	1,2269	0,7006
1,60	1,8090	1,0559	1,60	1,8059	1,0649	1,60	1,2279	0,7220	1,60	1,2264	0,7187
1,55	1,8088	1,0957	1,55	1,8055	1,0939	1,55	1,2279	0,7509	1,55	1,2264	0,7305
1,50	1,8084	1,1247	1,50	1,8053	1,1370	1,50	1,2275	0,7670	1,50	1,2260	0,7654
1,45	1,8084	1,1664	1,45	1,8051	1,1643	1,45	1,2271	0,7876	1,45	1,2258	0,7924
1,40	1,8082	1,2253	1,40	1,8048	1,1953	1,40	1,2267	0,8176	1,40	1,2256	0,8168
1,35	1,8078	1,2482	1,35	1,8048	1,2441	1,35	1,2264	0,8426	1,35	1,2252	0,8497
1,30	1,8076	1,2909	1,30	1,8044	1,3099	1,30	1,2260	0,8769	1,30	1,2250	0,8746
1,25	1,8071	1,3188	1,25	1,8042	1,3360	1,25	1,2262	0,9079	1,25	1,2246	0,8975
1,20	1,8067	1,3895	1,20	1,8036	1,3869	1,20	1,2258	0,9282	1,20	1,2241	0,9413
1,15	1,8063	1,4273	1,15	1,8034	1,4171	1,15	1,2254	0,9801	1,15	1,2239	0,9716
1,10	1,8057	1,5044	1,10	1,8030	1,5021	1,10	1,2250	1,0055	1,10	1,2235	1,0191
1,05	1,8053	1,5553	1,05	1,8025	1,5399	1,05	1,2244	1,0643	1,05	1,2229	1,0586
1,00	1,8044	1,6400	1,00	1,8021	1,6380	1,00	1,2239	1,1015	1,00	1,2225	1,1108
0,95	1,8042	1,7053	0,95	1,8017	1,6954	0,95	1,2231	1,1646	0,95	1,2218	1,1603
0,90	1,8034	1,8033	0,90	1,8011	1,8007	0,90	1,2225	1,2146	0,90	1,2210	1,2269
0,85	1,8028	1,8954	0,85	1,8007	1,8794	0,85	1,2216	1,2859	0,85	1,2208	1,2846
0,80	1,8017	2,0107	0,80	1,7996	1,9996	0,80	1,2212	1,3542	0,80	1,2200	1,3703
0,75	1,8015	2,1188	0,75	1,7992	2,1093	0,75	1,2204	1,4410	0,75	1,2195	1,4340
0,70	1,8005	2,2765	0,70	1,7986	2,2539	0,70	1,2189	1,5232	0,70	1,2183	1,5520
0,65	1,7994	2,3988	0,65	1,7981	2,3962	0,65	1,2179	1,6417	0,65	1,2176	1,6226
0,60	1,7981	2,5233	0,60	1,7960	2,5932	0,60	1,2168	1,7371	0,60	1,2162	1,7196
0,55	1,7967	2,7629	0,55	1,7946	2,7606	0,55	1,2145	1,9104	0,55	1,2151	1,7894
0,50	1,7937	2,9510	0,50	1,7921	3,0322	0,50	1,2135	2,0211	0,50	1,2132	2,0127
0,45	1,7634	3,1823	0,45	1,7298	3,1745	0,45	1,2111	2,1702	0,45	1,2118	2,2129
0,40	1,6498	2,5004	0,40	1,6452	3,2669	0,40	1,2095	2,2829	0,40	1,2088	2,4174
0,35	1,6084	0,0000	0,35	1,7595	0,0000	0,35	1,1929	2,6332	0,35	1,1902	2,6593
0,30	0,0003	0,0000	0,30	0,0005	0,0000	0,30	1,1253	2,7709	0,30	1,0915	2,7489



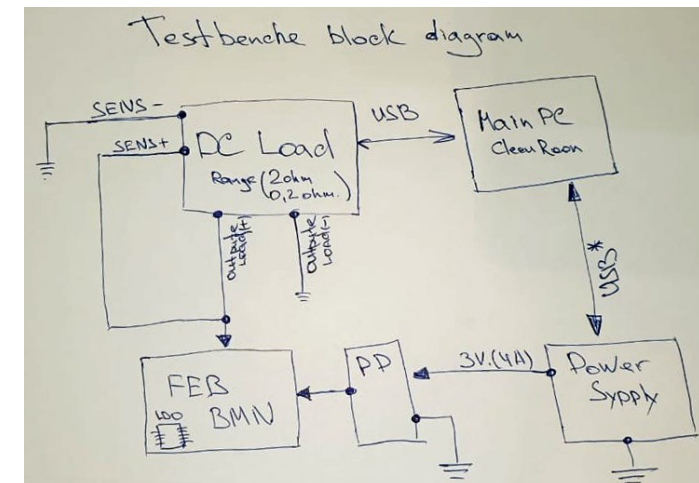
Power supply Rohde & Schwarz Model HMP2020

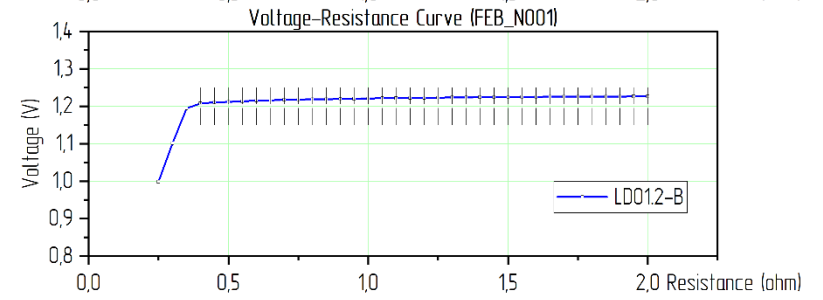
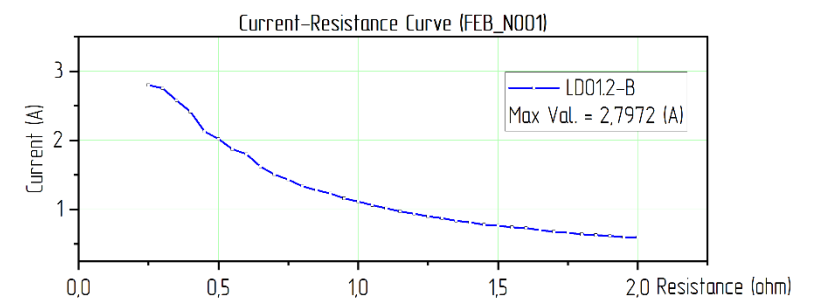
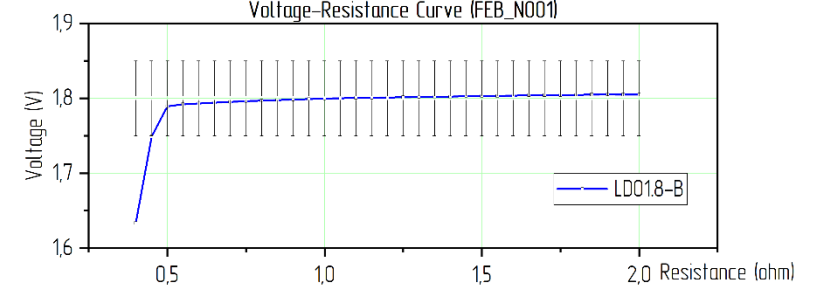
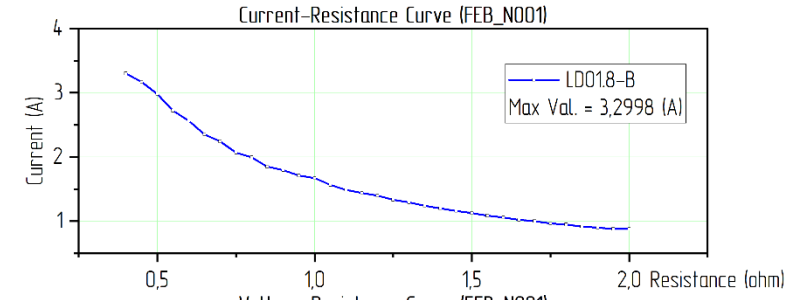
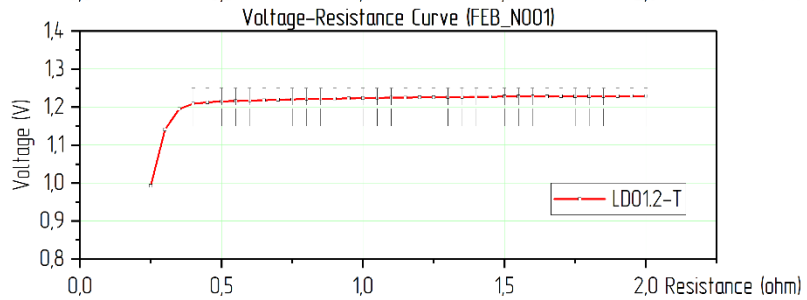
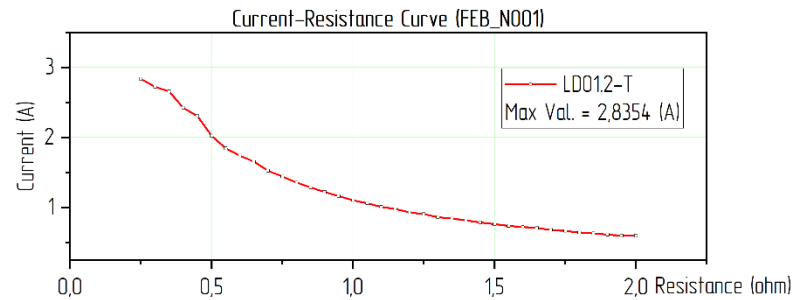
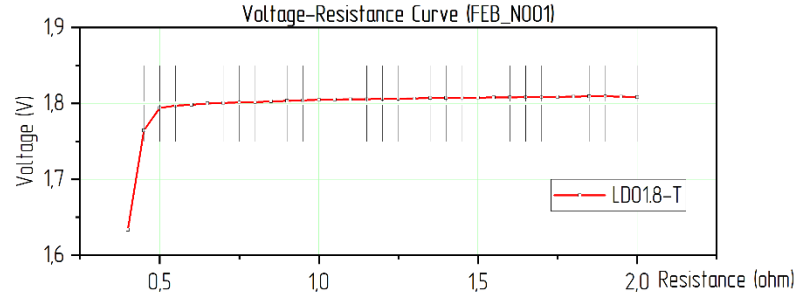
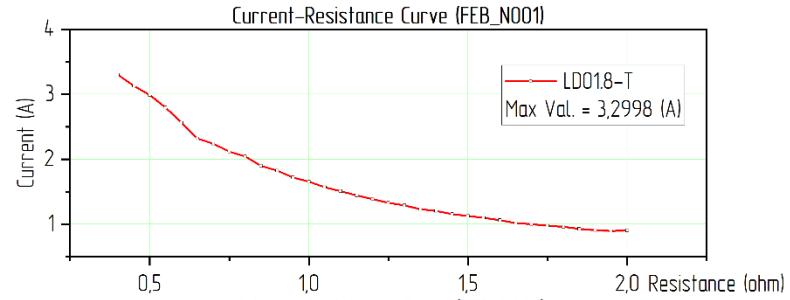


FEB BM@N



Keithley programmable DC electronic load Model 2380-500





- ZCU102 was selected as TFC hardware platform.
- A basic control interface, based on the IPBus protocol was developed.
- A solution base on WR-LEN is going to be used to synchronize the system to the Clock and Timing Network.

- The testing procedure LDO v2.1 at JINR lab was decreased from 30 minute to 1 minute with the help of the new testbench

Backup Slides

- Read transaction (Type ID = 0x0)
- write transaction (Type ID = 0x1)
- Non-incrementing read transaction (Type ID = 0x2)
- Non-incrementing write transaction (Type ID = 0x3)

https://ipbus.web.cern.ch/doc/user/html/_downloads/d251e03ea4badd71f62cffb24f110cfa/ipbus_protocol_v2_0.pdf