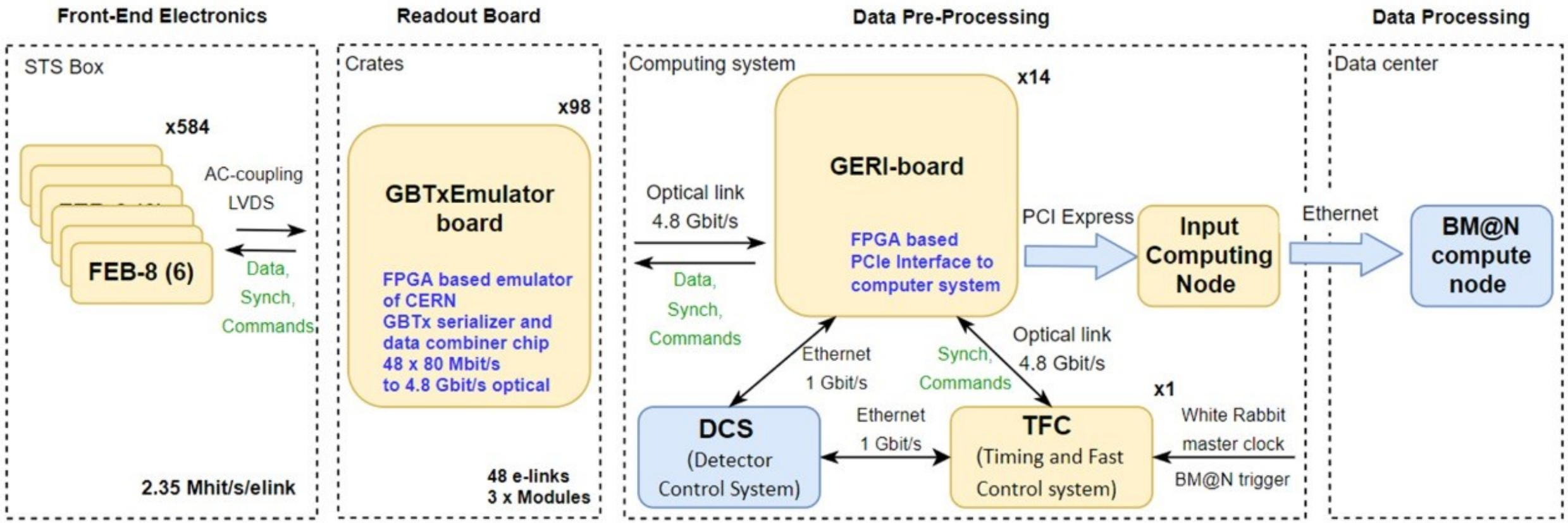
Tasks related to the integration of the Timing and Fast Control system (TFC) in the BM@N readout chain.

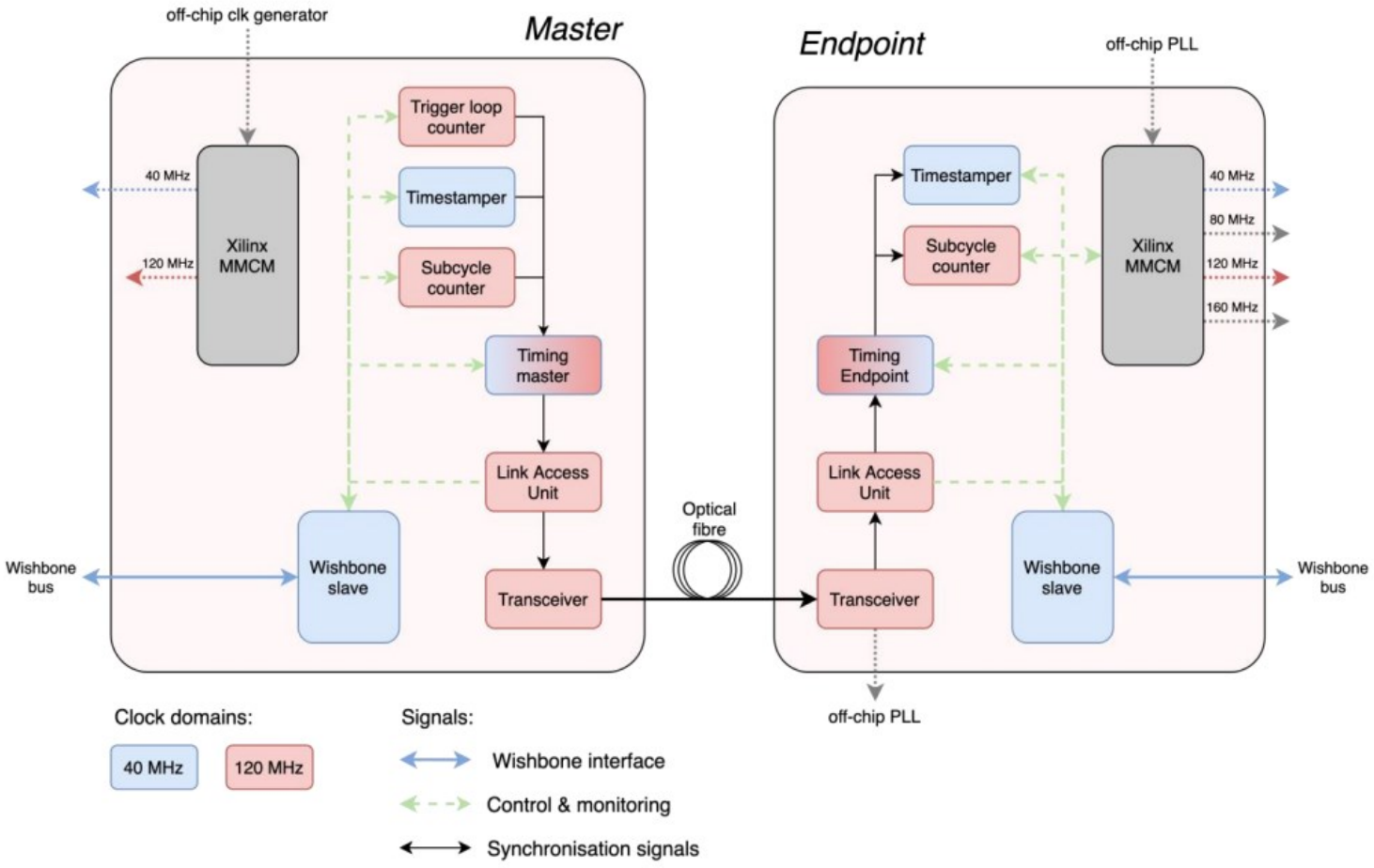
Raúl Arteche Díaz (JINR/CEADEN)

1. **Selection of the hardware platform for the TFC.**
2. **Implement the basic control interface based on the IPBus protocol.**
3. **Implement a solution to synchronize the system to the Clock and Timing Network.**
4. **Assembly and testing procedure LDO v2.1 at JINR lab.**


Front-End Electronics
Readout Board
Data Pre-Processing
Data Processing
STS Box
x584
FEB-8 (6)
AC-coupling
LVDS
Data,
Synch,
Commands
2.35 Mhit/s/elink
Crates
x98
GBTxEmulator board
FPGA based emulator of CERN GBTx serializer and data combiner chip 48 x 80 Mbit/s to 4.8 Gbit/s optical
48 e-links
3 x Modules
Computing system
x14
GERI-board
FPGA based PCIe Interface to computer system
Optical link
4.8 Gbit/s
Data,
Synch,
Commands
PCI Express
Input Computing Node
Ethernet
Data center
BM@N compute node
Ethernet
1 Gbit/s
Synch,
Commands
Optical link
4.8 Gbit/s
x1
DCS
(Detector Control System)
Ethernet
1 Gbit/s
TFC
(Timing and Fast Control system)
White Rabbit
master clock
BM@N trigger

1. Selection of the hardware platform for the TFC.

Architecture of Master and Endpoint TFC cores.



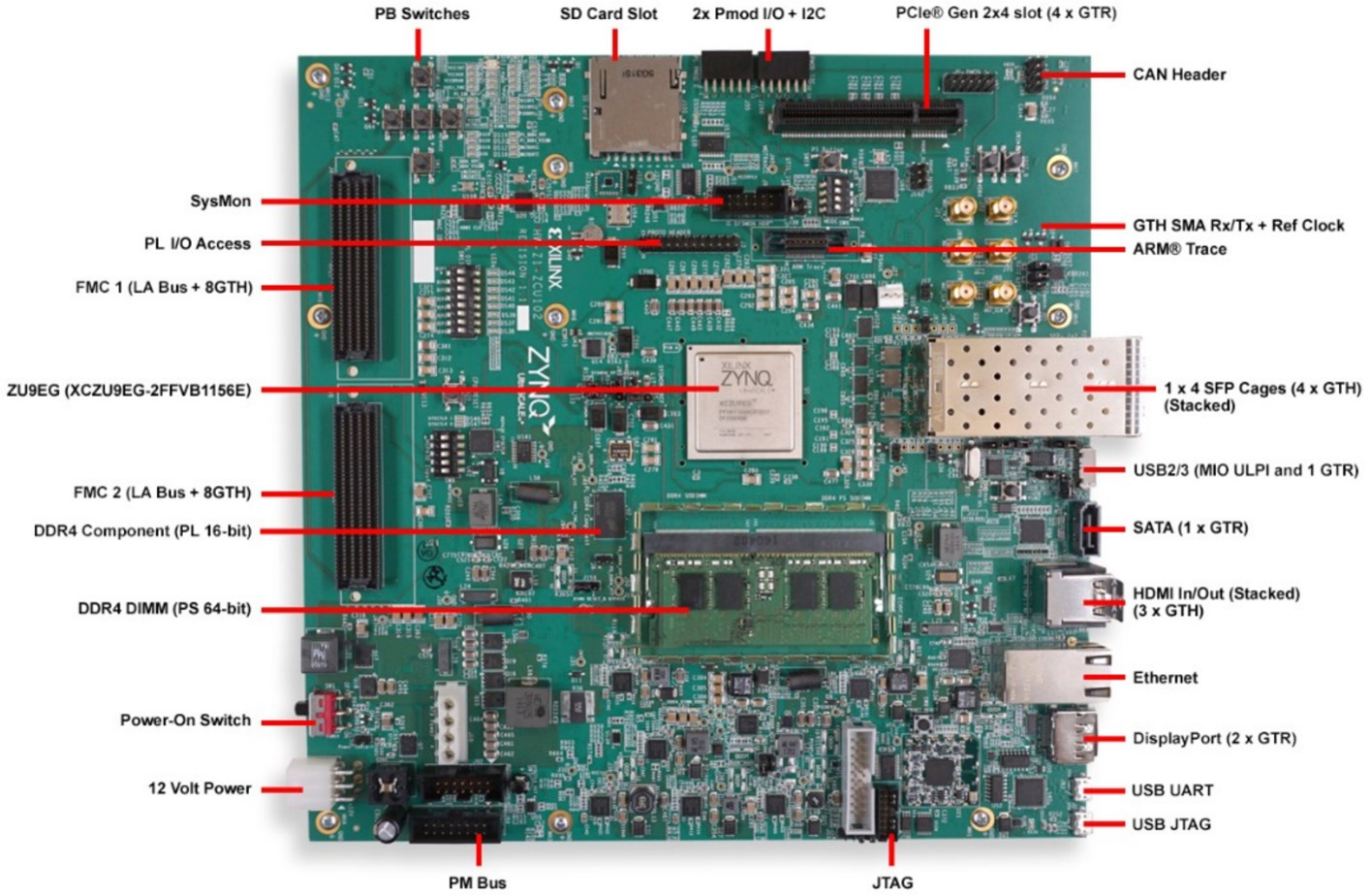
- Platform board: BNL-712

Mezzanine cards:

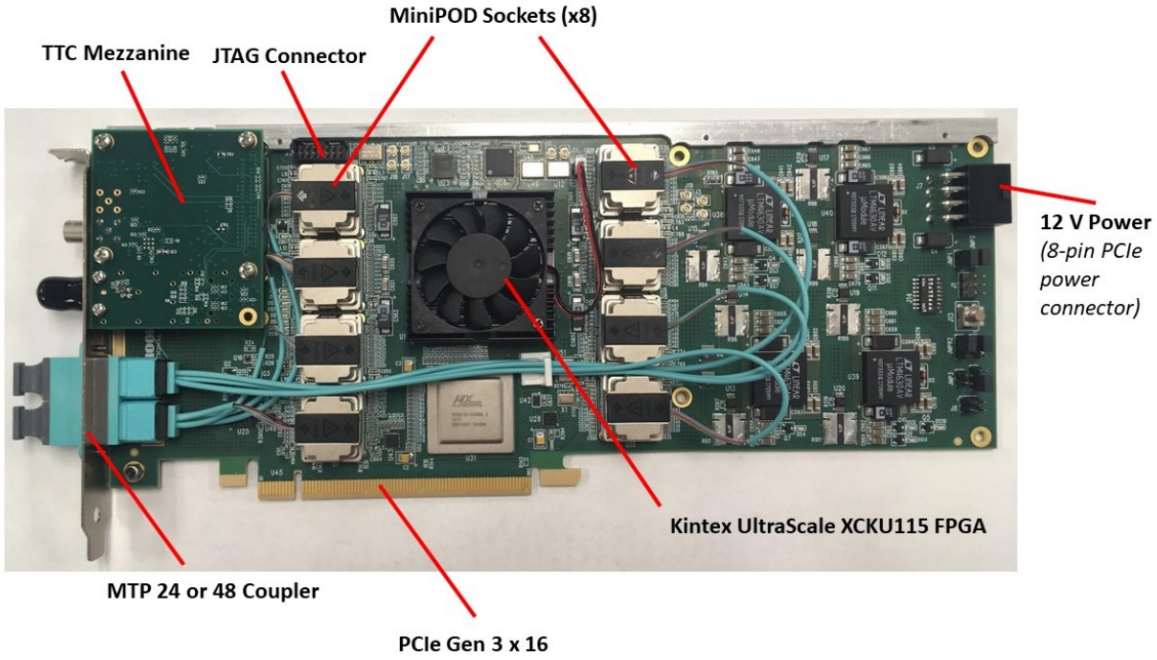
- Master - WR TMC
- Endpoint - TTC-PON TMC

https://indico.cern.ch/event/1019078/contributions/4444397/attachments/2312299/3935290/twepp_sidorenko.pdf

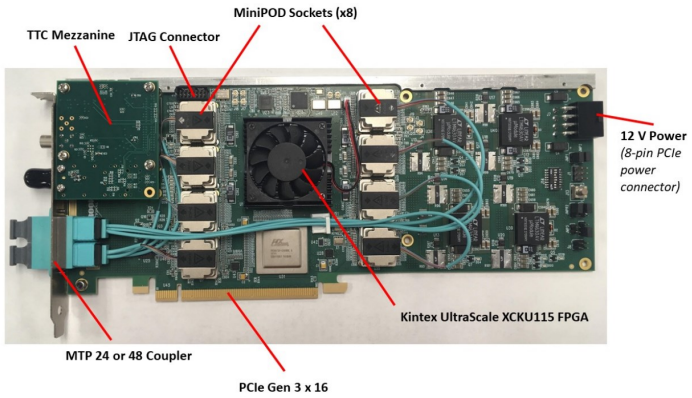
ZCU102 Evaluation Kit



BNL-712 board

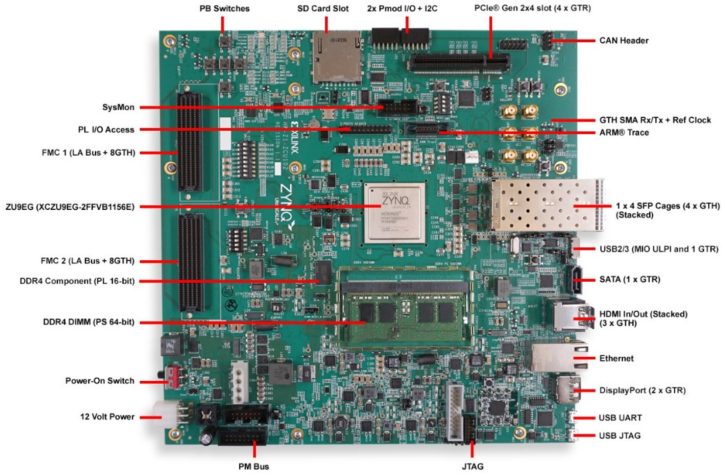


BNL-712 board



- ❑ Interactive operation from Python console
- ❑ AGWB-base Wishbone infrastructure
- ❑ Firmware develop base on fusesoc tool

ZCU102 Evaluation Kit



- ❑ PICe + Wishbone register access
- ❑ GTH Ultrascale transcivers

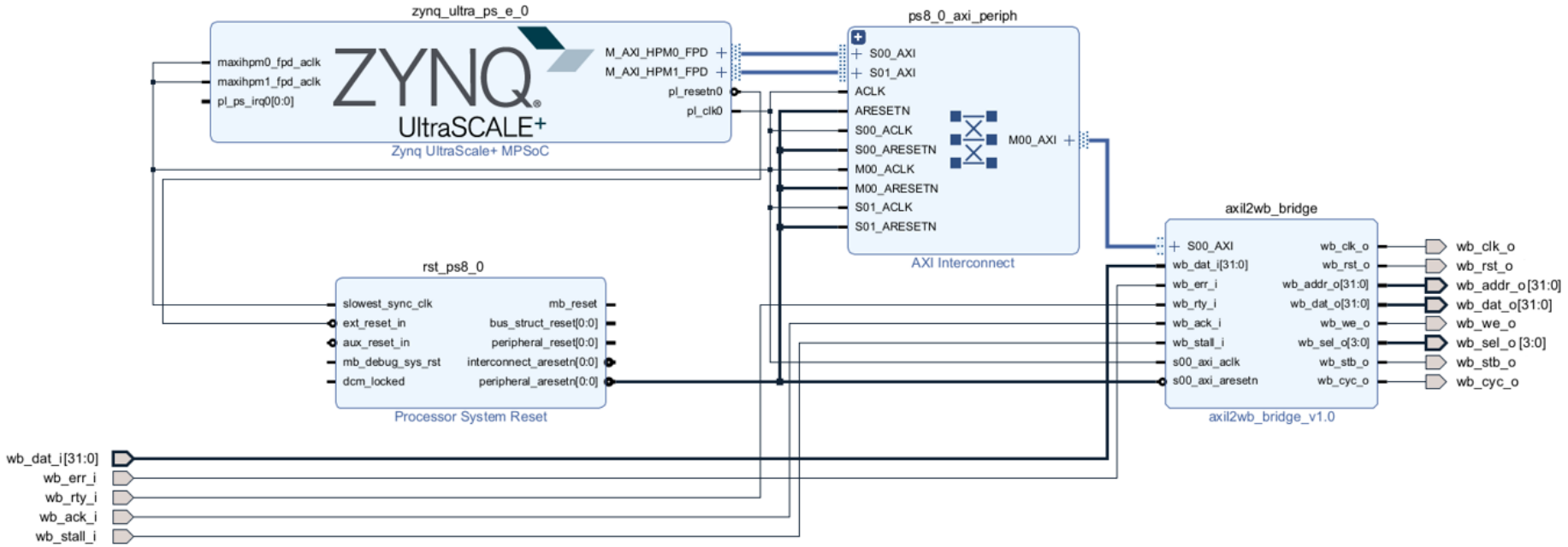
- ❑ Zynq + Wishbone register access
- ❑ GTH Ultrascale+ transcivers

CBM TFC-master repository :

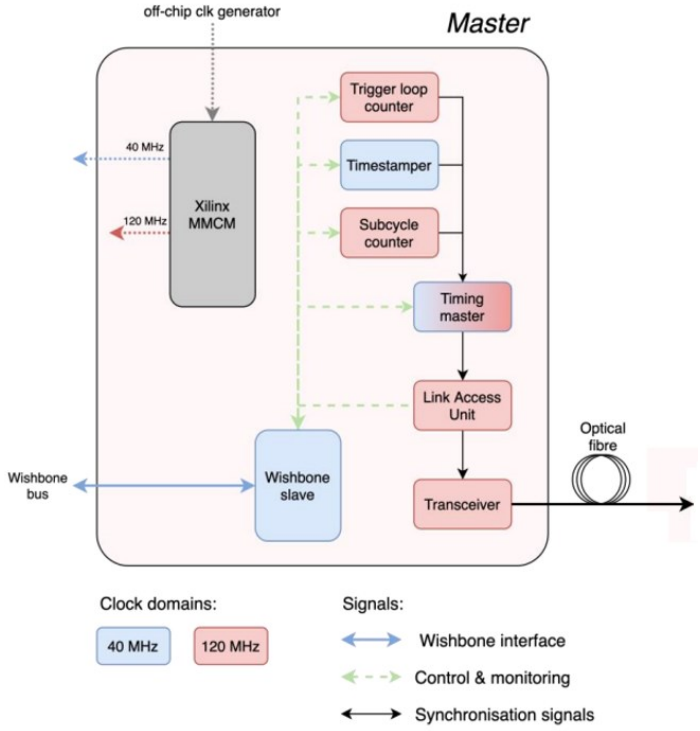
https://git.cbm.gsi.de/daq/fpga-firmware/tfc/cri-tfc/-/tree/tfc_devel/projects/tfc2_master

2. Implement the basic control interface, based on the IPBus protocol.

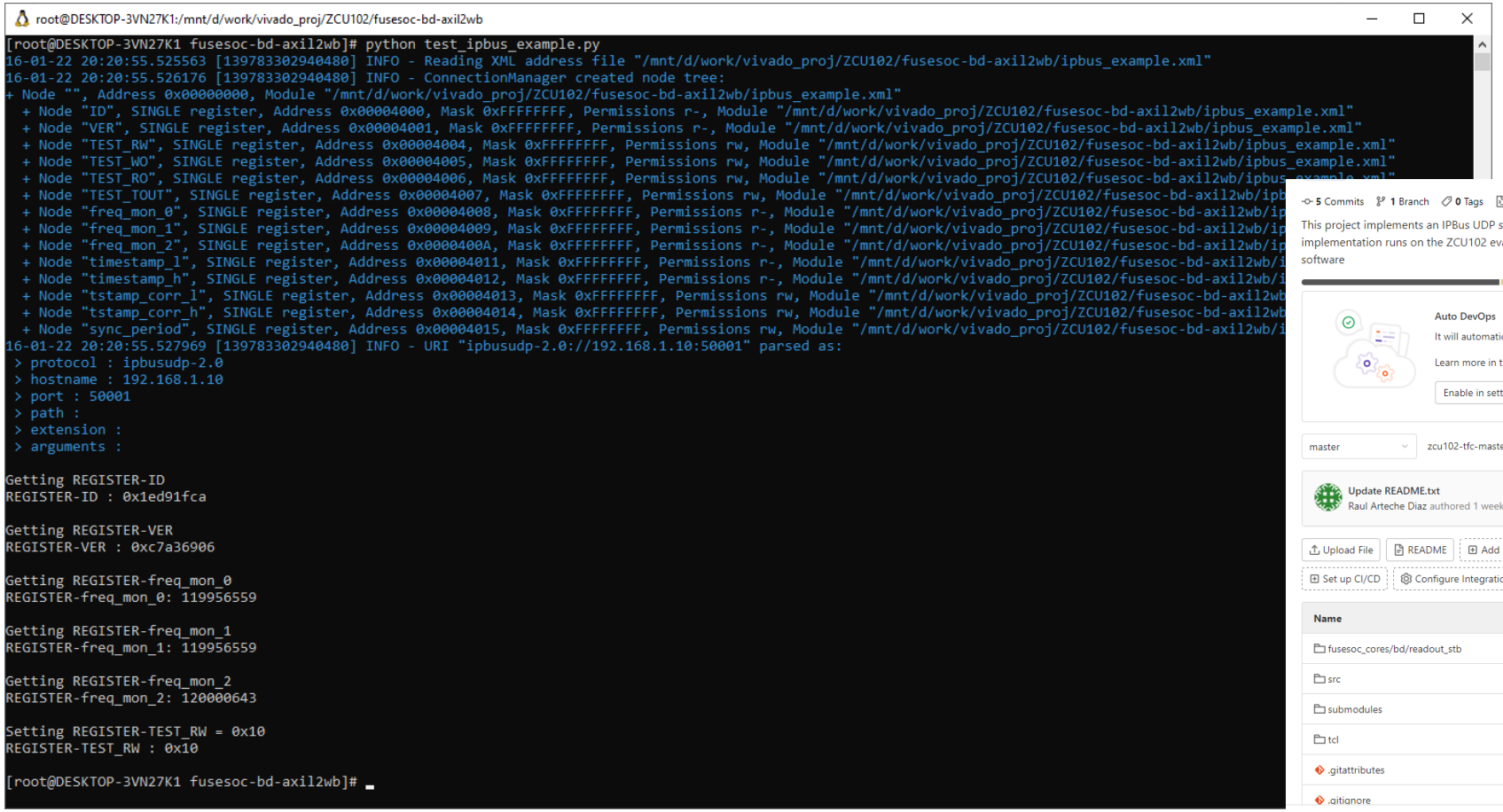
Zynq + AXIL to Wishbone bridge.



Architecture of Master TFC core.



The FreeRTOS LwIP UDP IPBus Server application creates a UDP server to provide connections to IPBus client running on host machine. Once the remote client connects with this server, the UDP server will start decoding data from client according to the IPbus 2.0 protocol.



https://git.jinr.ru/v.sidorenko/zcu102-tfc-master

3. Implement a solution to synchronize the system to the Clock and Timing Network.

SEVEN Solutions
When every nanosecond counts

WHITE RABBIT LEN

WR-LEN

It is the competitive WR alternative capable of supporting **daisy chain** configurations. It allows a cost effective solution to distribute **PPS/10MHz** signals or **IRIG-B** protocol to your equipment.

The WR-LEN is also available in its OEM version in order to integrate accurate timing synchronization into your product.

Optional: 2xμ-DB9 connector for PPSs & 10MHz fan-out or configurable output triggers.

www.sevensols.com

info@sevensols.com
support@sevensols.com

SEVEN Solutions
(+34) 958 285 024
C/ Periodista Rafael Gómez Montero, 2
Oficina 13 - Edf. CETIC
18014 Granada, SPAIN.

Technical Specifications / WR-LEN

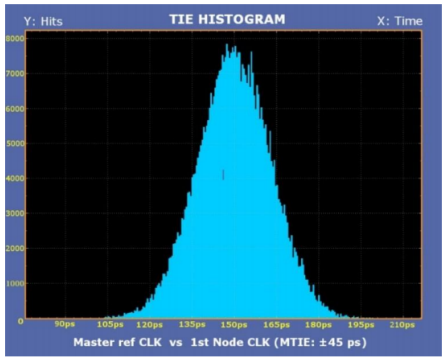
Management ports	
10/100/1000 ETH	Ethernet copper to fiber links data retransmission, node management
USB-UART	ToD, management
Software	
CLI	Command line interface for configuration and status information
Timing protocols/interfaces	
PTPv2 /White-Rabbit	Dual optical fiber Ethernet 1G interfaces
IRIG-B / PPS I/O	Digital LVTTL (3.3V). Selectable operation
Frequency I/O	10 MHz programmable input/output
Certifications	
Product	RoHS, FCC, CE, SE
Others	ISO-9001, ISO-14001
Physical Specification	
Dimension	54 x 105 x 135 mm
Color	Black (Metallic)
Power supply	
Voltage, current and power	5V DC, 1.5A - 7.5W max
Environmental Conditions	
Temperature	-10ºC ~ +50ºC
Humidity	0% ~ 90% RH
Under request extras	
2 x μDB9 connectors + converters to SMA	PPSs & 10MHz fanout or Configurable output triggers

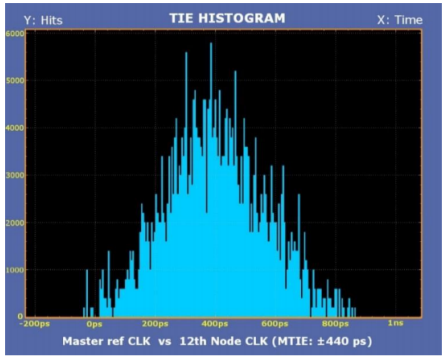
HIGHLIGHTS

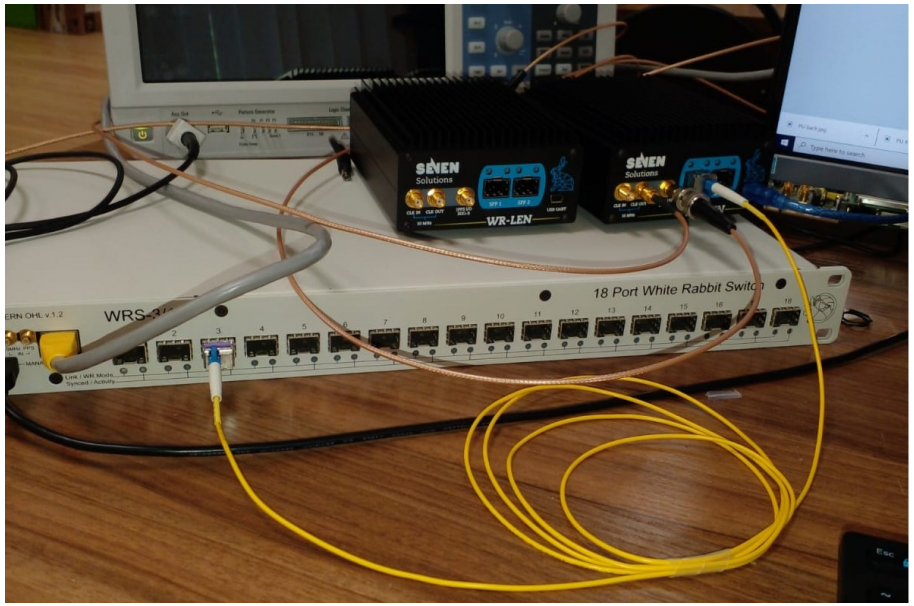
- ✓ Sub-nanosecond time accuracy
- ✓ Compact size
- ✓ Distance range: over 80 km using fiber
- ✓ Dynamic calibration
- ✓ Cost effective
- ✓ Time and frequency distribution
- ✓ Optional fan-out of PPS/10MHz

* Available in its OEM version!

Master reference clock (10MHz) vs Nodes Clock (10 MHz) in a daisy chain configuration

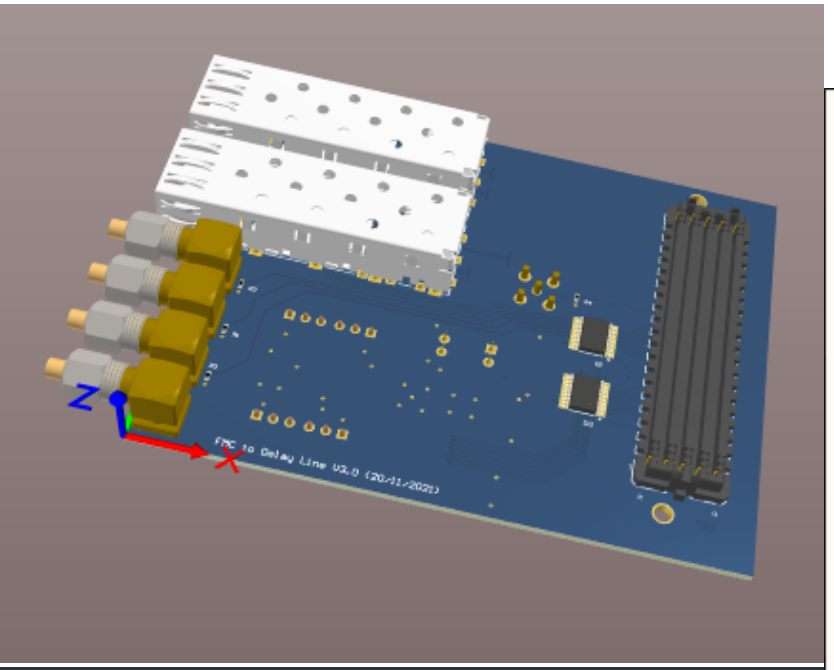


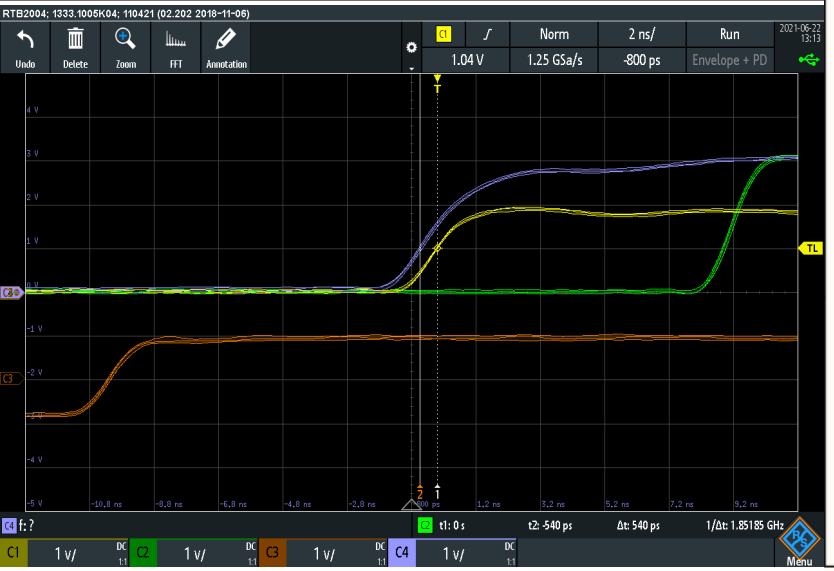



SEVEN Solutions
WR-LEN
18 Port White Rabbit Switch

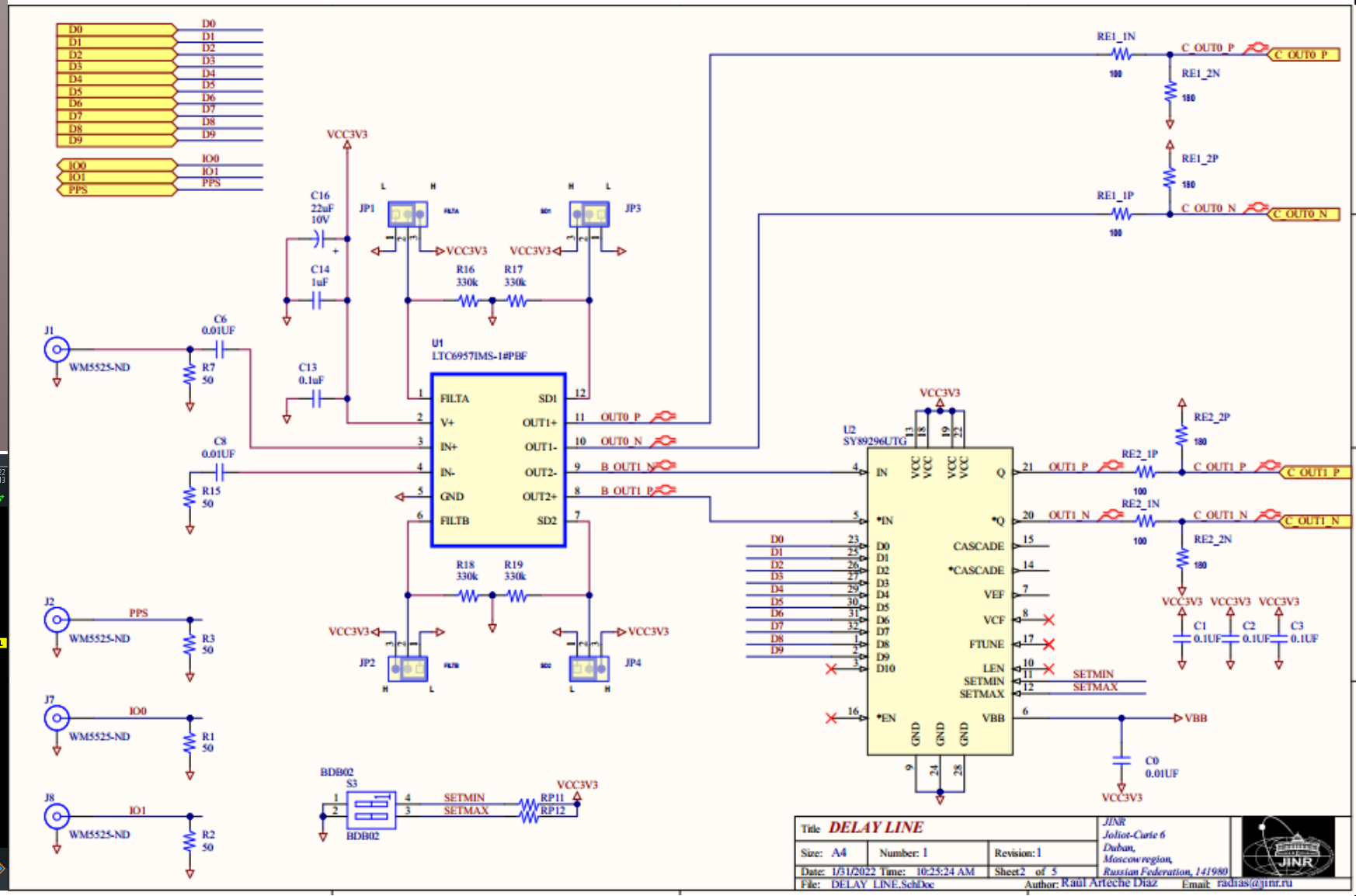

RTB2004; 1333.1005K04; 110421 (02.202 2018-11-06)
Undo
Delete
Zoom
FFT
Annotation
Norm
20 ns/
Run
1.04 V
1.25 GSa/s
-800 ps
Envelope + PD
C1 WRS-PPS
C2 WRS-10MHZ
C3 WRL-10MHZ
C4 WRL-PPS
TL
C4 f: ?
C1 1 V/ DC
C2 1 V/ DC
C3 1 V/ DC
C4 1 V/ DC
Menu


RTB2004; 1333.1005K04; 110421 (02.202 2018-11-06)
Undo
Delete
Zoom
FFT
Annotation
C1
Norm
2 ns/
Run
1.04 V
1.25 GSa/s
-800 ps
Envelope + PD
2021-06-22
13:13
TL
C4
C3
C4 f: ?
C2 t1: 0 s
t2: -540 ps
Δt: 540 ps
1/Δt: 1.85185 GHz
C1 1 V/ DC
C2 1 V/ DC
C3 1 V/ DC
C4 1 V/ DC
Menu

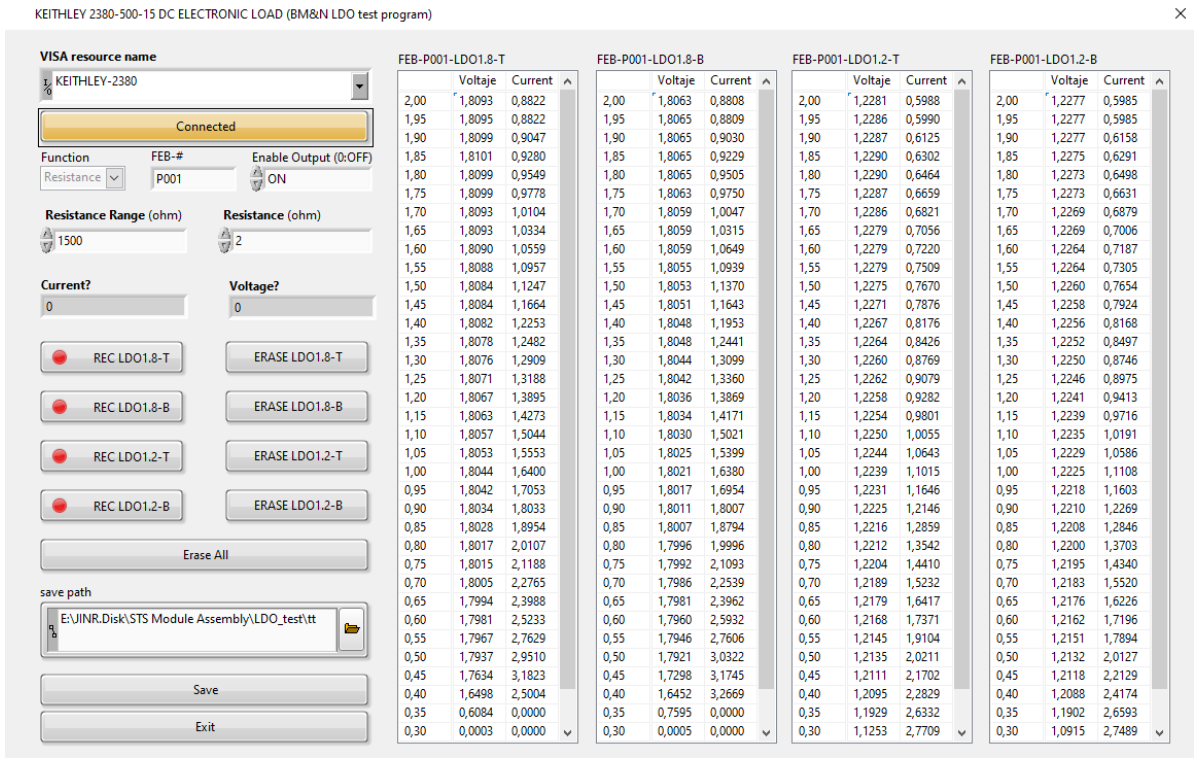


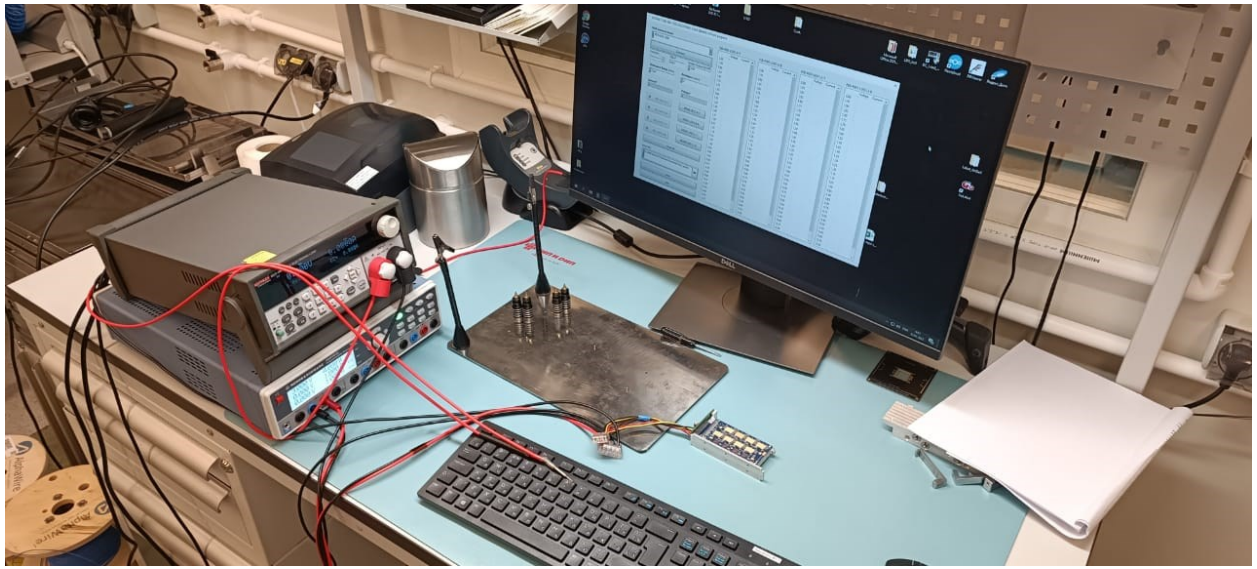


wr_clk delay range 3.2ns to 14.8ns in 10ps increments



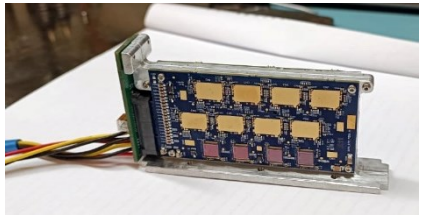
4. Assembly and testing procedure LDO v2.1 at JINR lab.



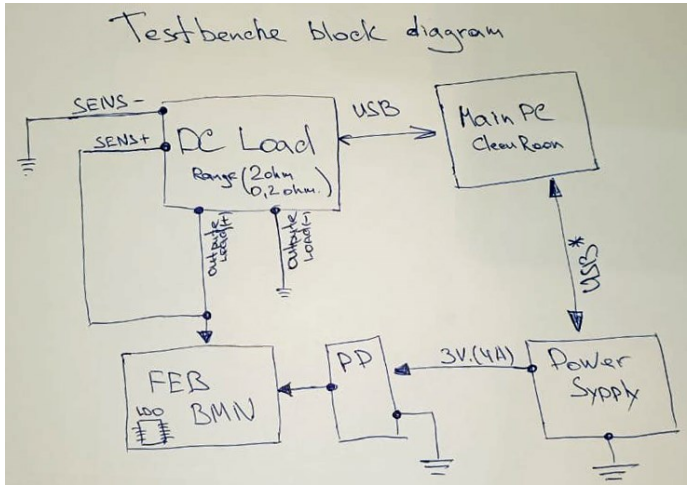


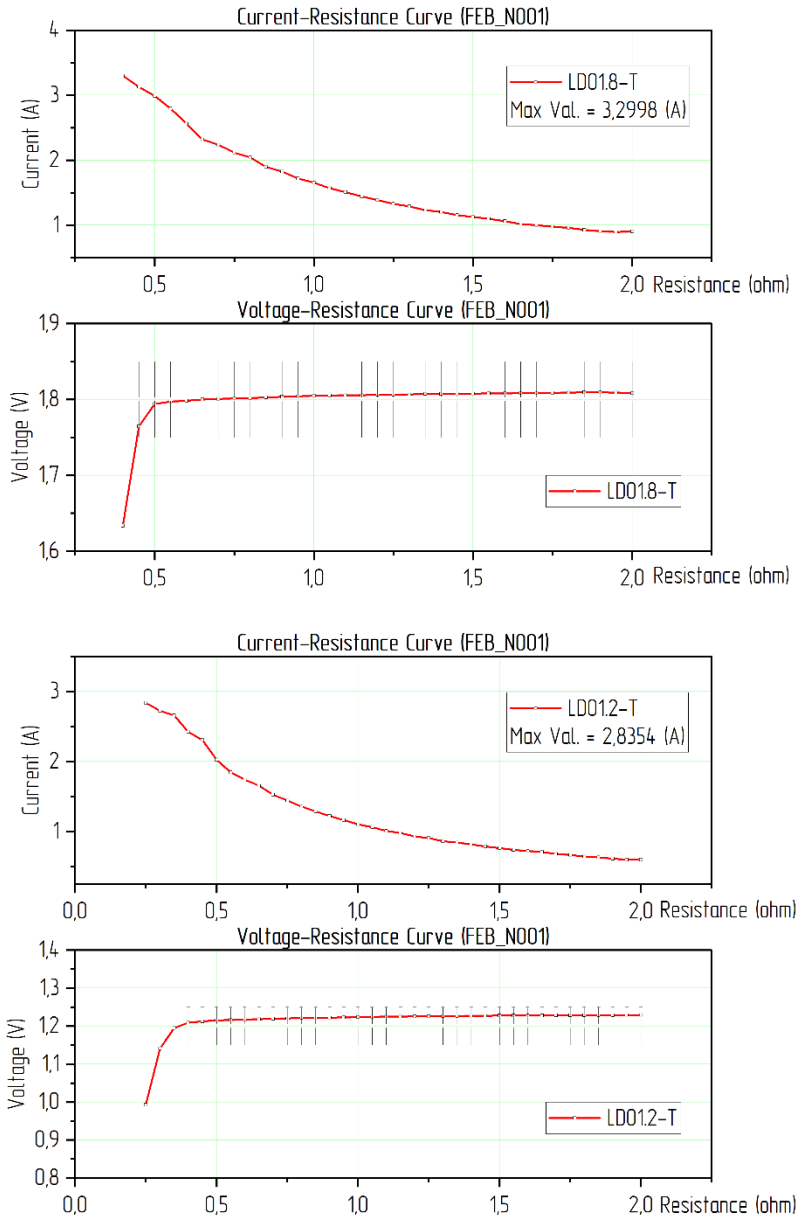
Power supply Rohde & Schwarz Model HMP2020

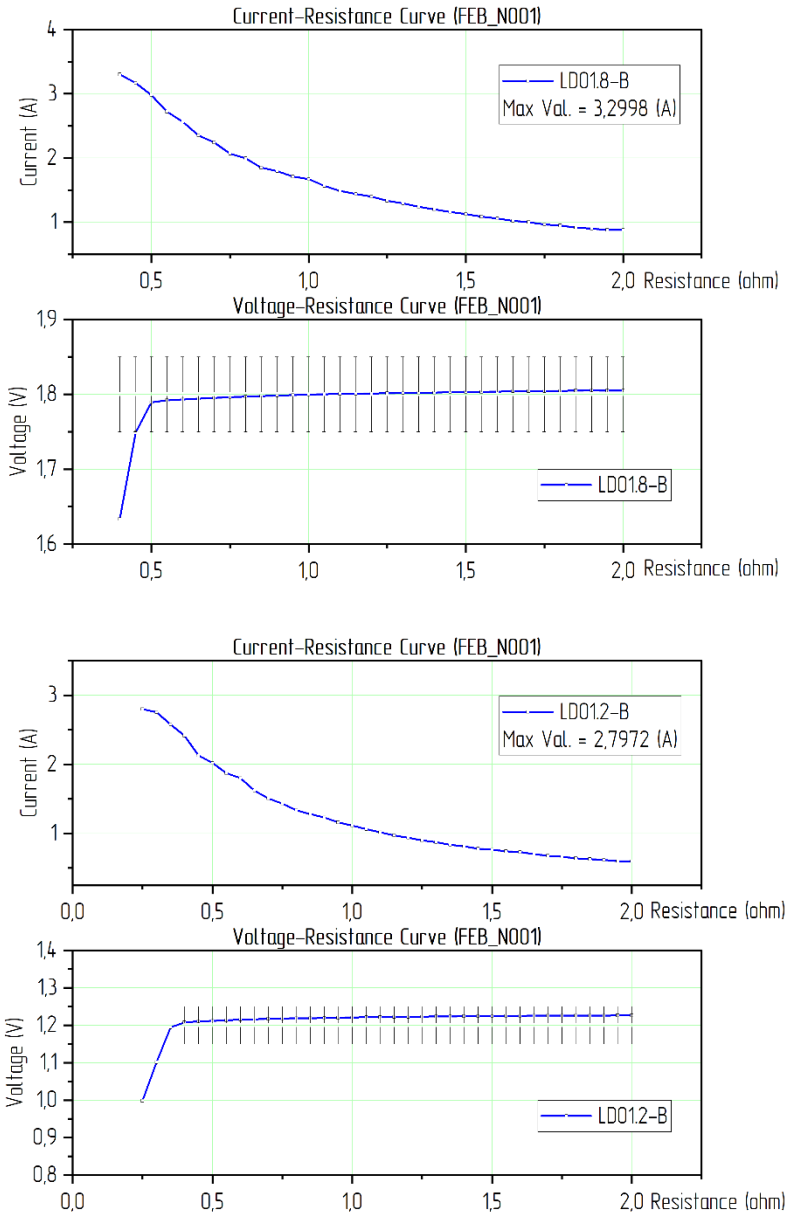
FEB BM@N



Keithley programmable DC electronic load Model 2380-500




Current–Resistance Curve (FEB_N001)
LDO1.8–T
Max Val. = 3,2998 (A)
Current (A)
Resistance (ohm)
Voltage–Resistance Curve (FEB_N001)
LDO1.8–T
Voltage (V)
Resistance (ohm)
Current–Resistance Curve (FEB_N001)
LDO1.2–T
Max Val. = 2,8354 (A)
Current (A)
Resistance (ohm)
Voltage–Resistance Curve (FEB_N001)
LDO1.2–T
Voltage (V)
Resistance (ohm)


Current–Resistance Curve (FEB_N001)
LDO1.8–B
Max Val. = 3,2998 (A)
Current (A)
Resistance (ohm)
Voltage–Resistance Curve (FEB_N001)
LDO1.8–B
Voltage (V)
Resistance (ohm)
Current–Resistance Curve (FEB_N001)
LDO1.2–B
Max Val. = 2,7972 (A)
Current (A)
Resistance (ohm)
Voltage–Resistance Curve (FEB_N001)
LDO1.2–B
Voltage (V)
Resistance (ohm)

- ZCU102 was selected as TFC hardware platform.
- A basic control interface, based on the IPBus protocol was developed.
- A solution base on WR-LEN is going to be used to synchronize the system to the Clock and Timing Network.

- The testing procedure LDO v2.1 at JINR lab was decreased from 30 minute to 1 minute with the help of the new testbench

Backup Slides

- Read transaction (Type ID = 0x0)
- write transaction (Type ID = 0x1)
- Non-incrementing read transaction (Type ID = 0x2)
- Non-incrementing write transaction (Type ID = 0x3)

https://ipbus.web.cern.ch/doc/user/html/_downloads/d251e03ea4badd71f62cffb24f110cfa/ipbus_protocol_v2_0.pdf