Status of the STS project

D. Dementev for STS & MPD-ITS teams

Current situation & possible outcomes

Collaboration with CBM-STS project was frozen with the following consequences for the BM@N STS :

- ❑ Ban on any professional communication and cancelling of all contracts with Germany. *No access to the critical components: readout ASICs and micro-cables*;
- ❑ Loose of the main funding source of the project: *GSI-JINR Roadmap Agreement*.

Outcomes

Current situation & possible outcomes

Possible strategies :

1. Search for the legal base for the derogation of the existing restrictions on the import of critical components from GSI.

2. Keeping on with **DSSD**-based technology. Redesign and production of the critical components (ASICs & micro-cables) in Russia.

3. **MAPS** – switching to the new sensor technology, foreseen for the MPD ITS detector.

Keeping on with DSSD technology (Proposal №2)

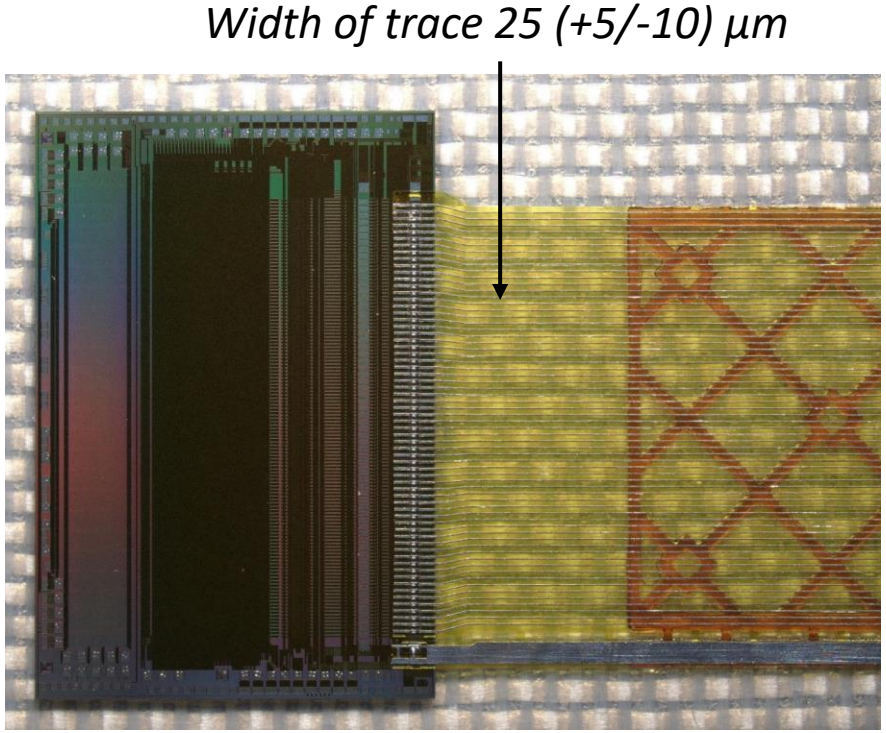
1. **Micro-cables** for the transmission of the analogue signal from the strips to the inputs of the readout ASIC

Proposal from SINP MSU:

Micro-cables could be developed and manufactured by "Horizont" company at Ekaterinburg.

Bonding parameters strongly depend upon the **width of traces and cross section**! Excessive variations make it necessary to adapt bonding parameters which is very time-consuming.

*=> Need for **precise masks and material** of a good quality!*



STSXYTER ASIC with micro-cable produced at LTU (Kharkov)

Keeping on with DSSD technology (Proposal №2)

2. Readout ASICs *Proposals from SINP MSU:*

a. Reverse engineering of the STSXYTER ASIC

Could be done with the help of "IDM-PLUS“ company. Project has to be redesigned afterwards to adapt it to the Fab’s technology

Pros: back-end readout chain remains unchanged

Cons: high power consumption (as for STSXYTER)

b. Use of the IC initially developed by MEPhI for the CBM GEM detectors as a groundwork for the new ASIC

Chip requires some minimal reworking, in particular changing of the front-end part. The project has to be adapted to the Fab’s technology.

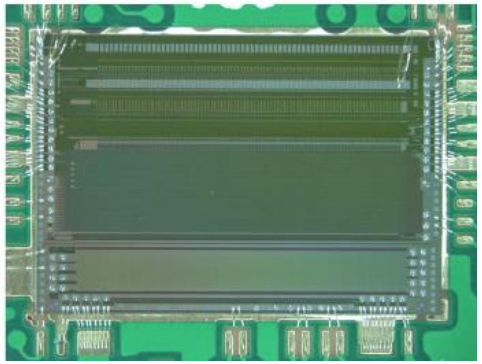
Pros: Existing ASIC design as a basis

Cons: Possible need for a redesign of the back-end electronics

c. Development of a new simplified ASIC from the scratch

Pros: Optimized for the experiment-specific requirements

Cons: Development from the scratch may require more than 3 years



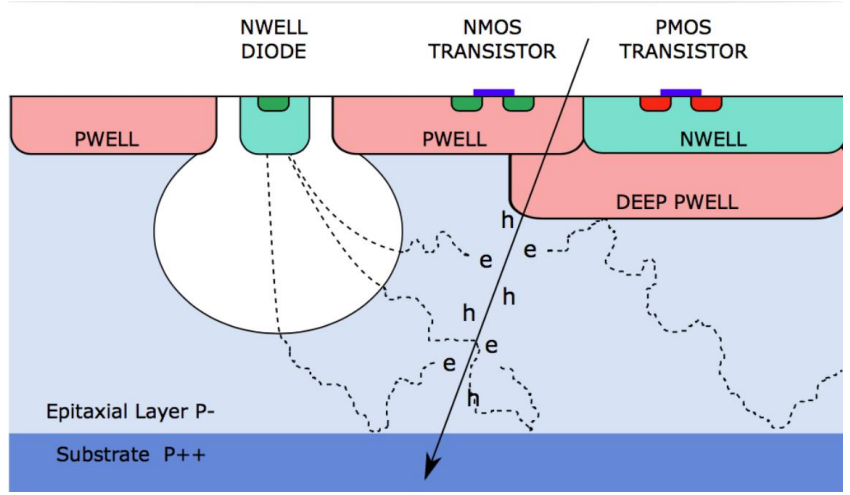
STSXYTER ASIC

Details in the talk of E. Atkin

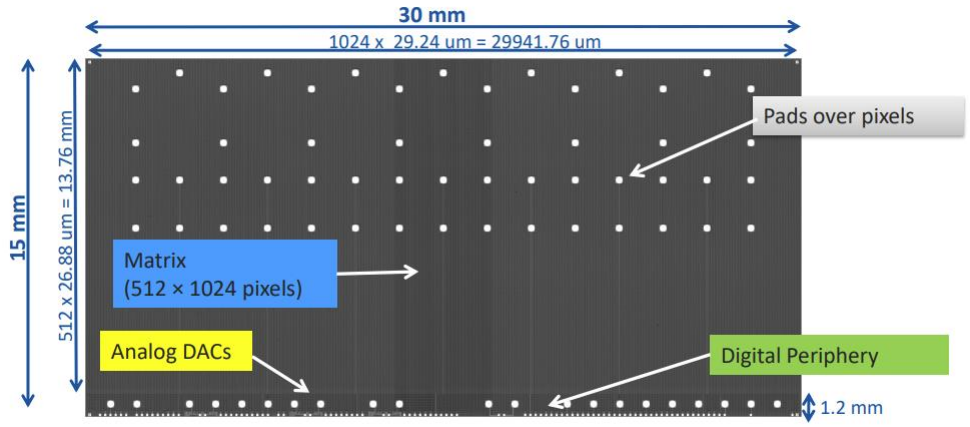
Usage of ALTAI MAPS for STS (Proposal №3)

ALTAI chip was designed at CERN especially for experiments at NICA and inherits the technology of ALPIDE Monolithic Active Pixel Sensor.

- ❑ High-resistivity (> 1kΩ cm) p-type epitaxial layer (20µm - 40µm thick) on p-type substrate.
- ❑ Small n-well diode (2-3 µm diameter), ~100 times smaller than pixel => low capacitance.
- ❑ Deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area.



© ALICE collaboration



MPD ITS

- ❑ Size: 15mm x 30mm
- ❑ Pixel pitch: 28µm x 28µm
- ❑ Event time resolution: < 2µs
- ❑ Power consumption: 39mW/cm²
- ❑ Dead area 1.1mm x 30mm

Status of ALTAI chips

- Preproduction batch 11 Wafers produced and tested

- Production of 19000 ALTAI chip contracted to CERN and already paid.

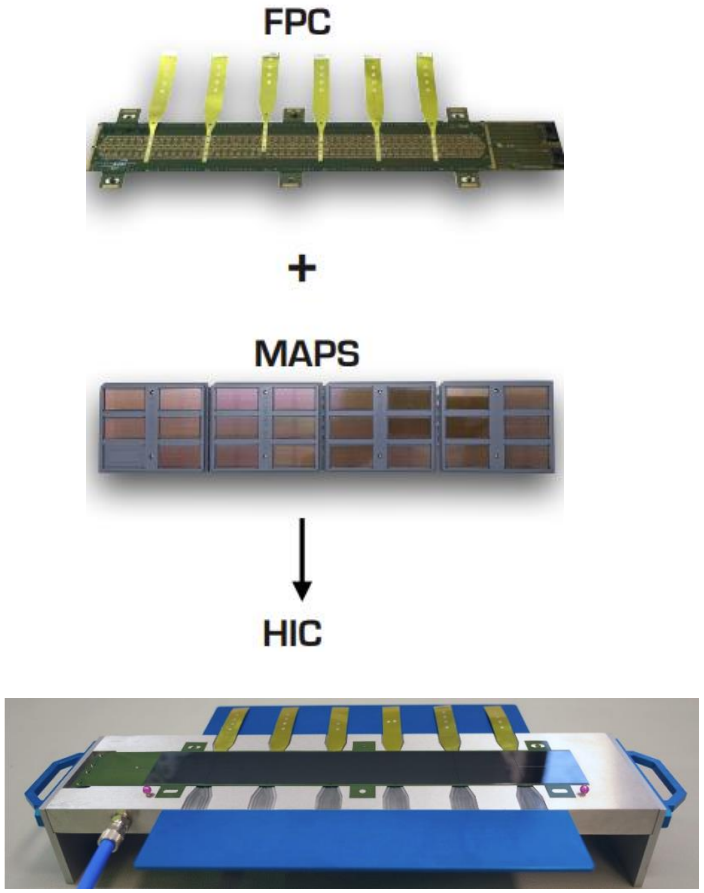
~ 2M USD

Current restriction: Council Regulation (EU) 2022/328 of 25 February 2022

CERN legal and logistics office is working on a possibility of an application for the derogation of the export restriction for the ALTAI chips.

C. Ceballos and Yu. Murin

Assembling of MAPs-based detector modules

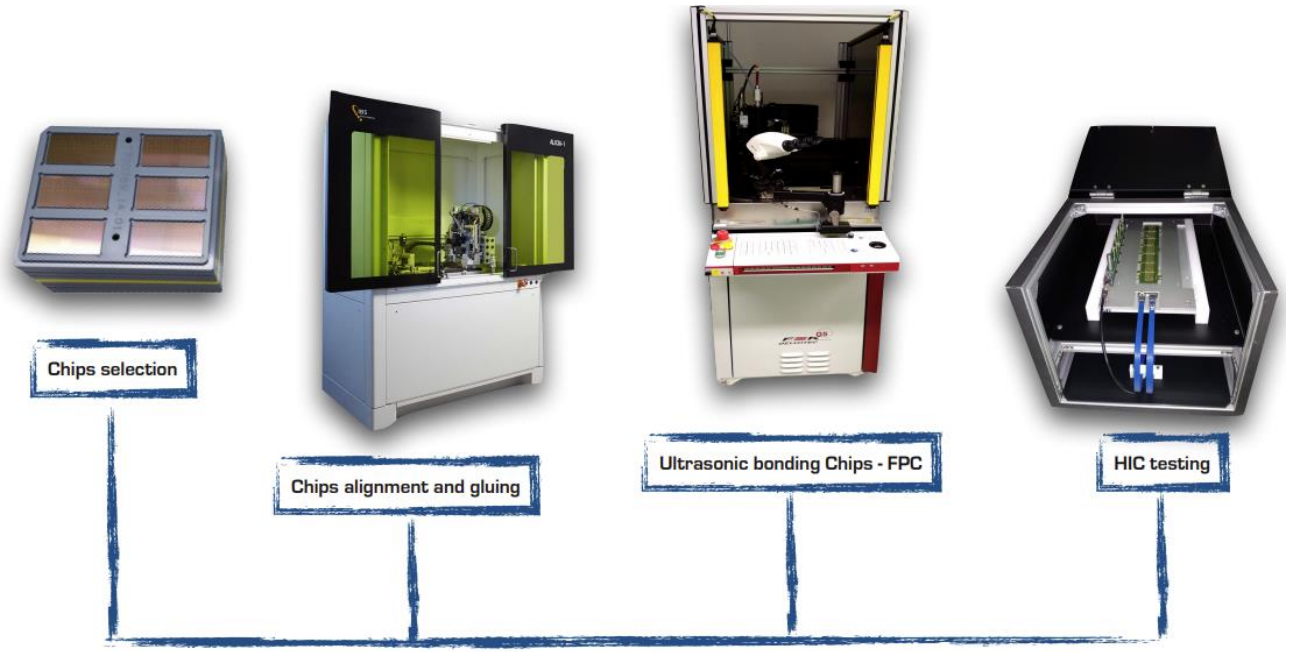


Full technological transfer from ALICE Collaboration

Complete Knowhow
Detector assembly and testing hardware/software
Assembly fixtures

Full detector assembly line from chips to detector layers is being setup **at JINR**

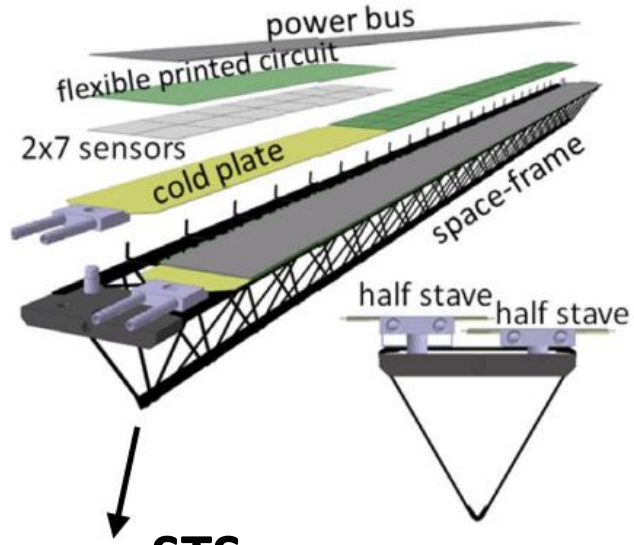
HICs assembly line was already tested



C. Ceballos, A. Sheremetiev & team

Usage of ALTAI MAPS for STS

Exploded view of the *super-module* of MPD ITS detector

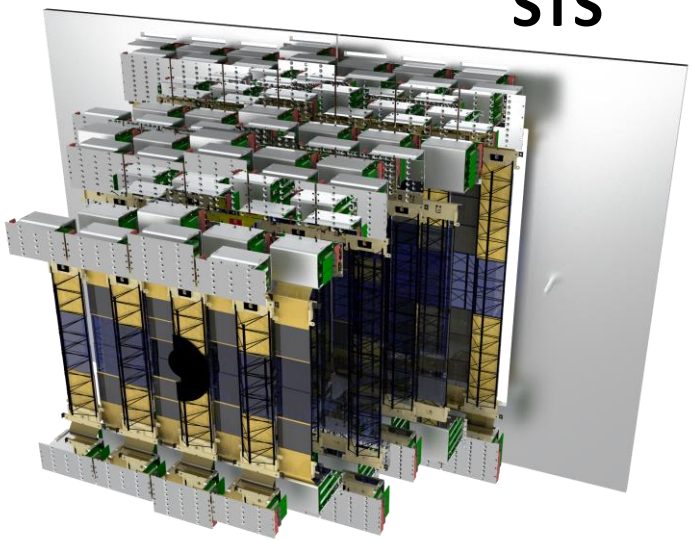


MAPS-based super-module (*stave*) has a width of 60 mm –

The same as DSSD-based super-module (*ladder*) of STS

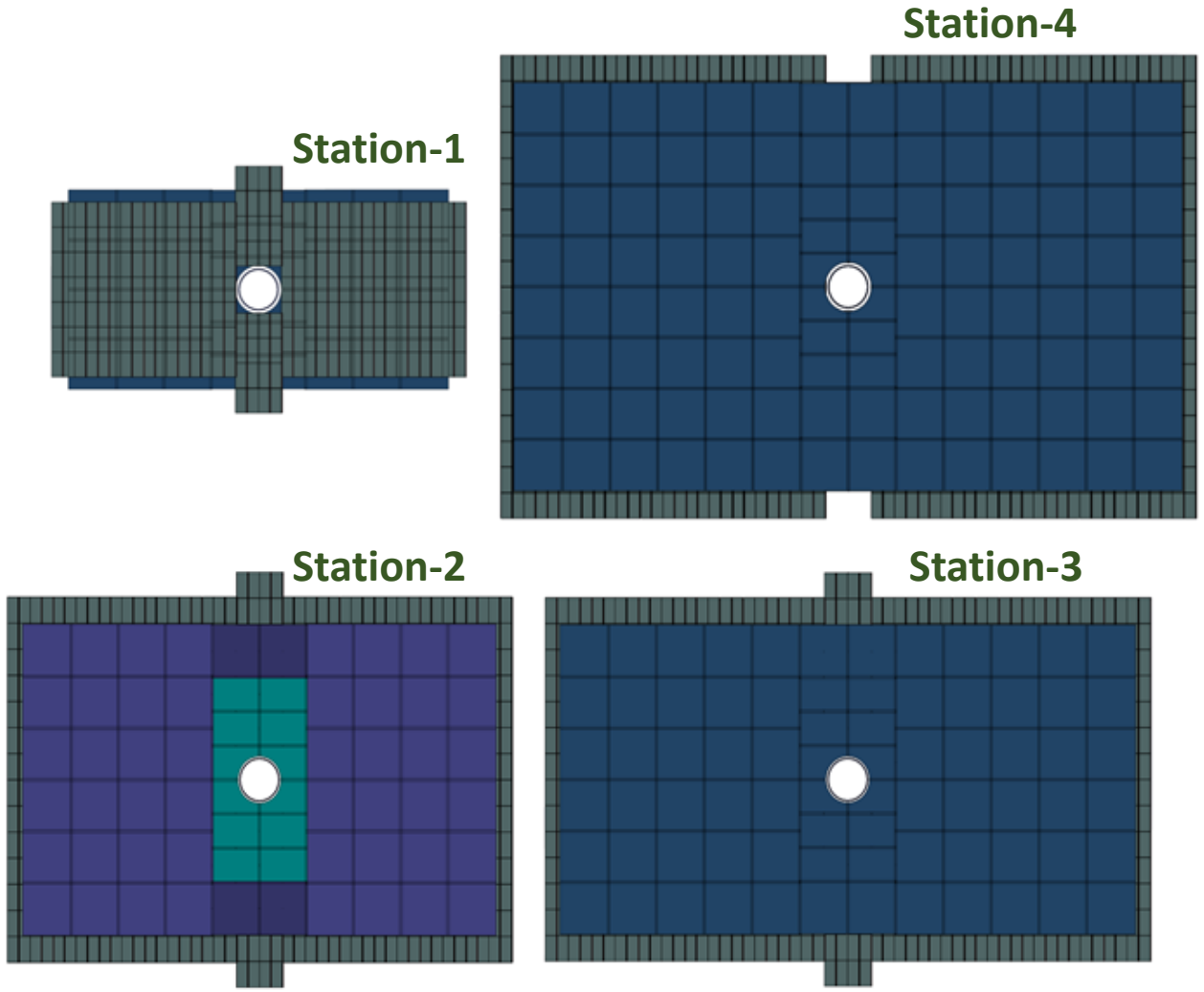
=> Possibility to use CF-frames, that were already produced for STS;

STS



Topology of STS stations based on MAPS

- 2.7 k ALTAI chips
- Power dissipation 0.5 kW!

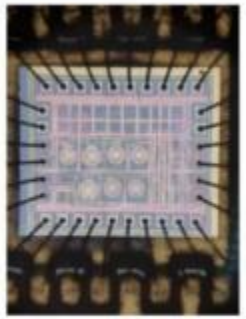


Comparison of the DSSD-based topology (blue) with a MAPS-based topology (grey)

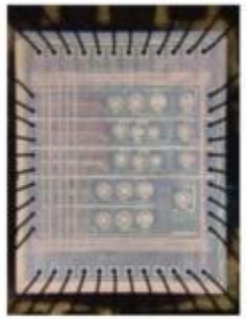
V. Elsha

Readout electronics for MAPS

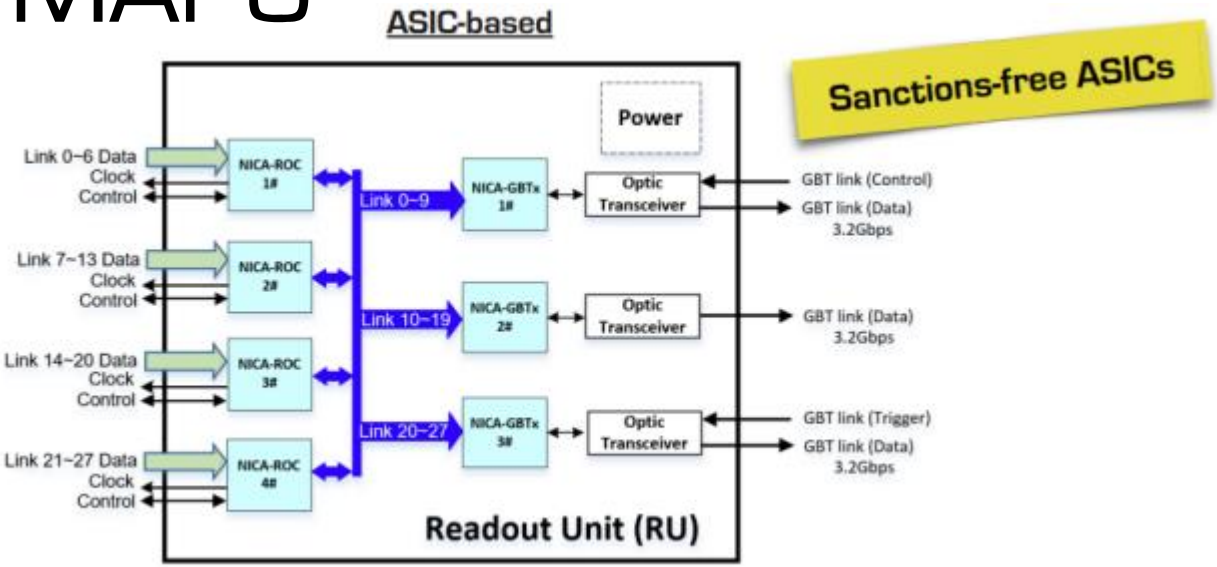
PLL+Deser Chip
Part of NICA_GBT core



LDLA Chip
For 1Tx+1Rx
optical module



LDAr Chip
For multi-Tx/Rx
optical module



UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA

ASICs for the data concentration and signal transmission between on-detector electronics and back-end interfaces via optical lines is being developed at USTC (China):

NICA_ROC: Concentrates the output data of front-end ALPIDE chips and transfer the packaged data to the following NICA_GBTx ASIC. It also receives control commands, clocks, and trigger signals from the backend and distributes them to ALPIDE chips.
NICA_GBTx: A high-speed bidirectional data interface ASIC for optical links.
NICA_LD (Laser Driver) and **NICA_TIA** (Transimpedance Amplifier): Are two analog ASICs that would be integrated together with the laser and PD (Pin Diode) in the customized optical transceiver module.

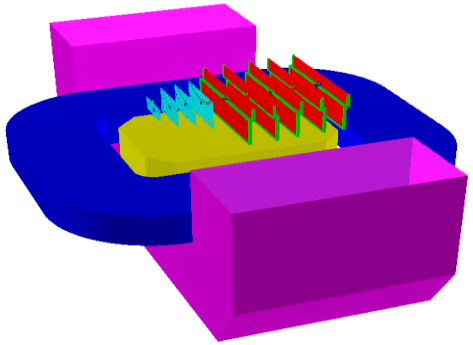
Full family of ASICs will be available in 2023.

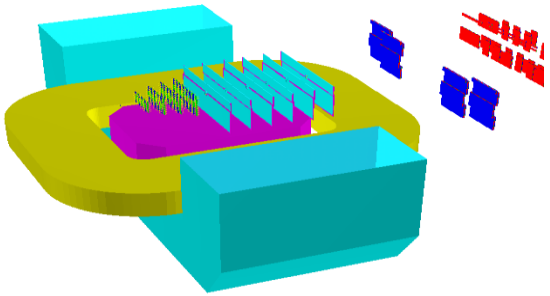
Tracking performance simulation

Detectors: Si (4 stations) + GEMs (5 (6) stations)

Generator: PHQMD, 0.5k Au+Au at T_0 = 4.0A GeV, 0-5 fm

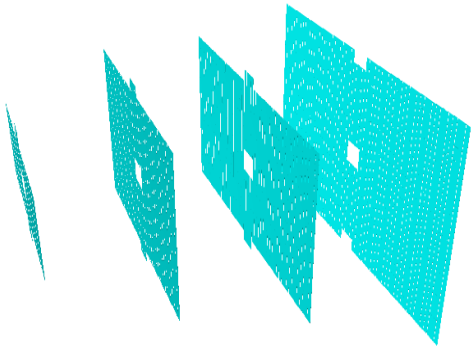
Magnetic field: B = 0.8 T



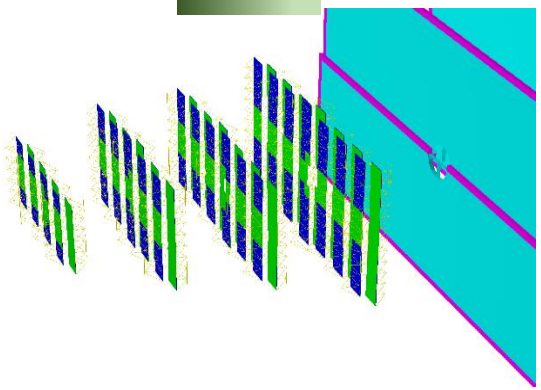


V. Kondratyev, A.Zinchenko, D.Zinchenko

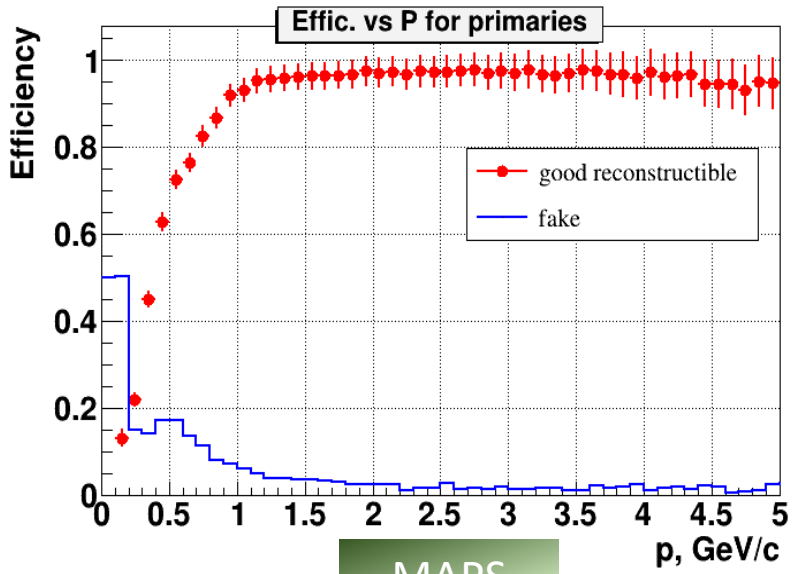
MAPS



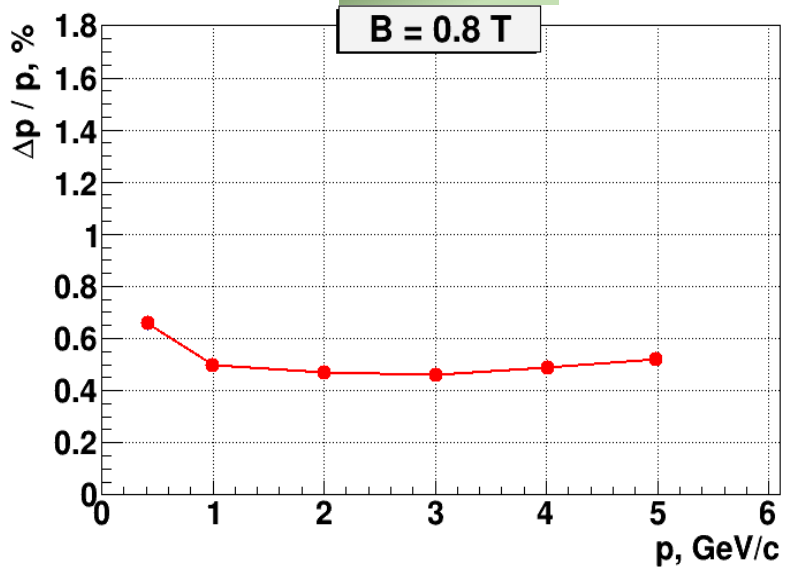
DSSD

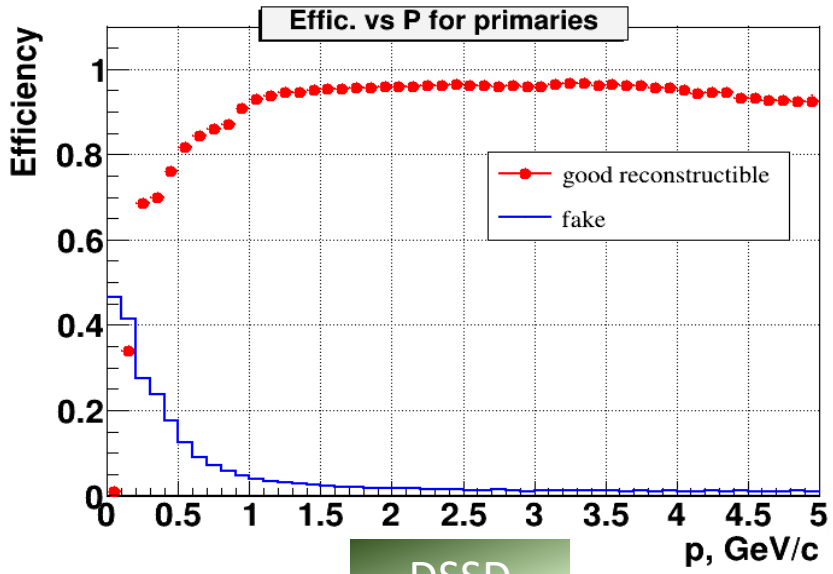


Tracking performance simulation

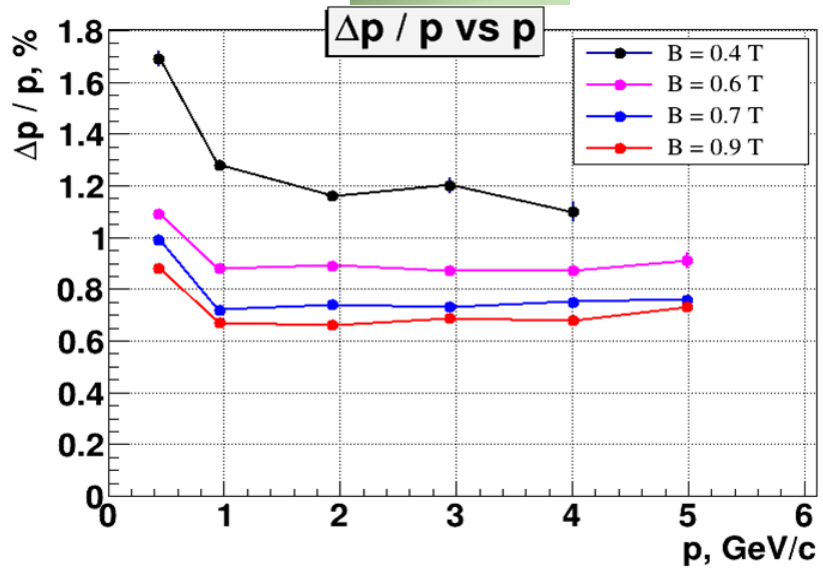


MAPS





DSSD



PRELIMINARY

A.Zinchenko and D.Zinchenko

Summary on DSSD

Pros	• DSSD sensors already in the dry-storage cabinets; • Full technological line for the detector assembly is ready at JINR; • Access to unlimited number of readout ASICS in the case of successful redesign and production of chips in Russia
Cons	• Uncertainty for the identification of Fab; • Need of a new ASIC design and possible redesign of the back-end electronics
Resources	MSU: 1M USD and 2-4 years for the redesign and production of new ASIC

Summary on MAPS

Pros	• Production of ALTAI chips already contracted to CERN and payed; first 11 wafers of tested chips already produced; • Full assembly line from chips to detector layers available at JINR • Synergy with MPD and future experiments at EicC (China)
Cons	• Pending on the official decision on export license on ALTAI chips from CERN;
Resources	2-3 years with 150k USD per year

Conclusion

STS project needs to be revised due to the freezing of collaboration with CBM-STS.

- Two proposals from SINP MSU and JINR groups are work in progress and open for the discussion.
- Two approaches are not competing with each other, but are only two available options. Both strategies could be realized only with a joint effort of JINR and SINP MSU groups.

Thanks for your attention!

Backup slides –>

Main problems:

- Lack of a readout electronics (ASIC)
- Lack of ultralight cables
- Lack of silicon sensors with a cutout for the beam pipe.

Sensors could be fully developed, manufactured and tested by SINP MSU. The fabrication itself could be done at the Zelenograd Science and Technology Center (ZSTC).

Cables could be developed and manufactured by "Horizont“ company at Ekaterinburg.

The most serious problem is ASIC.

Joint efforts of JINR, MEPhI, SINP MSU and IDM-PLUS are necessary to solve the problem by the middle of 2025.

Option A

The development, if possible, an exact copy of the STS-XYTER. This requires 2 - 3 ASICs (they are available at JINR), for copying and analysis of the topology and circuit design (the so-called "reverse design"), the equipment for this in "IDM-PLUS“ company is available. At the same time we propose to make small simplifications in the structure of ICs in the future, namely, to remove some of the gain adjustments, which should have been in STS-XYTER and provide the ability to work not only with silicon detectors, but also with GEM detectors. In the future, we should redesign the project to 180 nm STM technology (this is the technology that is available today in JSC "MIKRON").

The positive of this solution - all further existing electronics remain unchanged.

Negative - remains, as for the STS-XYTER high power consumption and low bit rate (5 bits) ADC in each channel.

Option B

We proposed to use as an available groundwork IC, developed by MEPhI under the leadership of V.V. Shumikhin/E.V. Atkin for gas (GEM) detectors of CBM experiment. The IC was prototyped (50 samples have been manufactured) using UMC 180 nm technology (the same technology used for the STS-XYTER). All design (schematic and topological) information is available here. This chip requires some minimal reworking, in particular, changing of the frontend part. From the point of view of rework of the front-end part for BM@N the SINP MSU and MEPhI have sufficient experience. Then, as in the first case, adaptation to the technological route of the manufacturer (JSC "MIKRON") is required.

Details in the next talk.

Positive - practically ready own design, minimal rework.

Negative - probably need to redesign the data acquisition electronics.

Option C

ASIC development from scratch, such as an analogue of VA-1 (VA-2), but tailored to the requirements of the BM@N experiment with the required specific parameters.

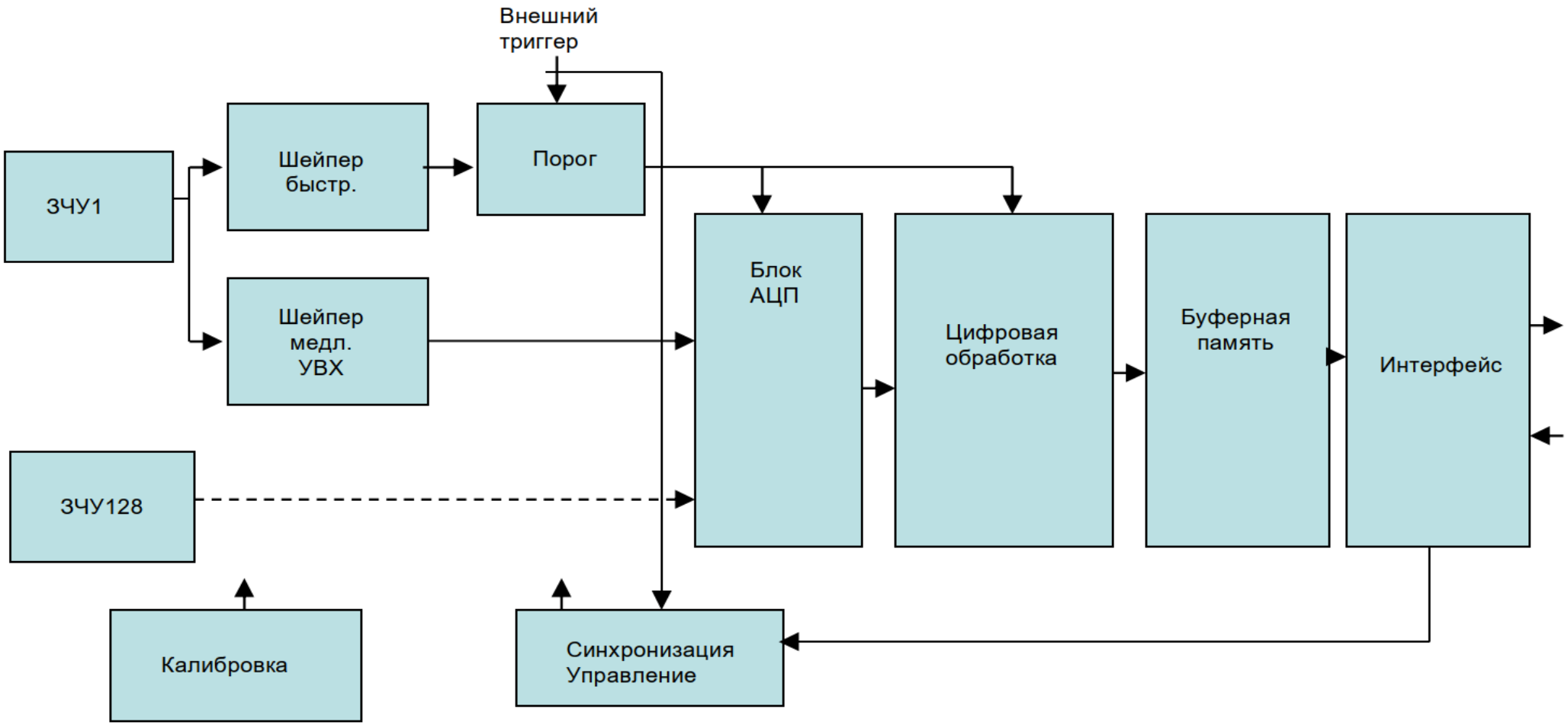
The pluses of this development are obvious - a specialized (optimized) chip for the experiment.

The disadvantages are also obvious: the lack of universality, the need to form the technical requirements, more development time, probably a higher labour content and as a consequence a higher cost, the risk that in 3 years the final version of the ASIC will not be ready.

Basic technical requirements for option B and C (this is for the first discussion ONLY!!!)

1. Number of input channels 128
2. Loading of channels/event does not exceed 16 - 20 channels
3. Minimum input signal (1 MIP) 3.6 fC
4. Signal-to-noise ratio in the slow channel at a capacity of 100 pF > 20
5. Signal-to-noise ratio in the fast channel > 10
6. Conversion time in the slow channel ~ 300 nsec
7. Conversion time in fast channel ~ 50-80 nsec.
8. Input signal polarity - ”+ “ and “-”
9. Dynamic range ~ 30 MIP (100 - 120 fC)
10. Maximum load of one channel < 100 kHz
11. Nonlinearity < 5%.
12. ADC bit rate for clock frequency 25 MHz - 8 -10 bit
13. Output clock frequency - 10 MHz
14. Power consumption not more than - 600 mW (5 mW per channel)
15. External trigger frequency up to - 100 kHz

First idea for option C



Status of ALTAI chips

- Preproduction batch 11 Wafers produced and waiting to be tested in Korea.
- Production of 19000 ALTAI chip contracted to CERN and already paid.

→ ~ 2M USD

Current restriction:

Council Regulation (EU) 2022/328 of 25 February 2022

Article 2a - paragraph 1:

It shall be prohibited to sell, supply, transfer or export, directly or indirectly, goods and technology which might contribute to Russia's military and technological enhancement, or the development of the defence and security sector, as listed in Annex VII, whether or not originating in the Union, to any natural or legal person, entity or body in Russia or for use in Russia.

C. Ceballos and Yu. Murin

Status of ALTAI chips

The provision foresees Derogations (Art 2a - paragraphs 4 and 5) in certain defined situations

Possible grounds on which apply for a derogation of the export restrictions for the ALTAI chips from CERN to JINR

(Art 2a - paragraph 4)

(c) intended for the operation, maintenance, fuel retreatment and safety of civil nuclear capabilities, as well as civil nuclear cooperation, in particular in the field of research and development;

(f) intended for the exclusive use of entities owned, or solely or jointly controlled by a legal person, entity or body which is incorporated or constituted under the law of a Member State or of a partner country;

Note:

The Committee of Plenipotentiaries of the Governments of the Institute Member States is the supreme body of JINR. Each member of the Institute has one representative in the Committee of Plenipotentiaries and some of the JINR Member States are also EU Member States (e.g. Bulgaria, Slovakia, Romania)

C. Ceballos and Yu. Murin