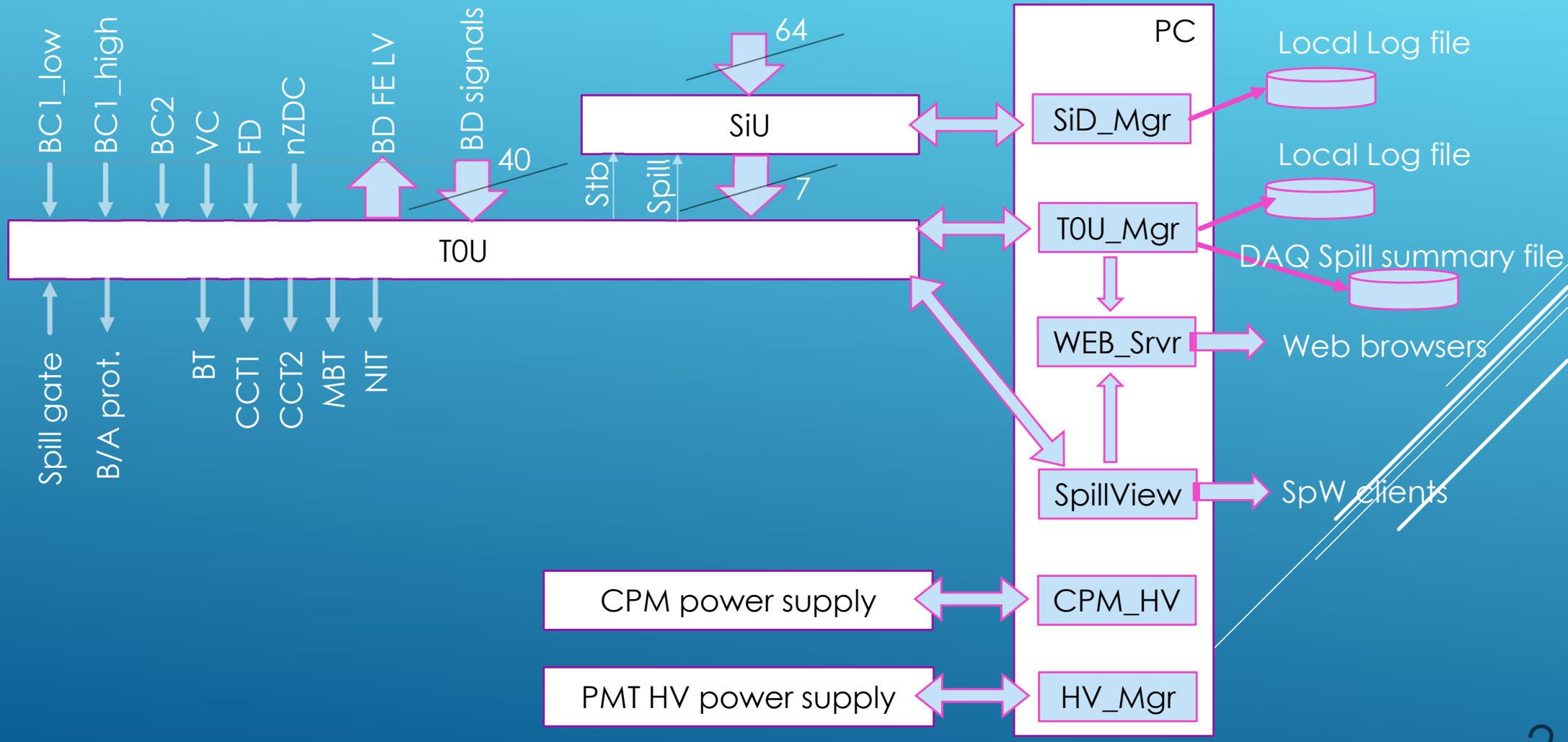
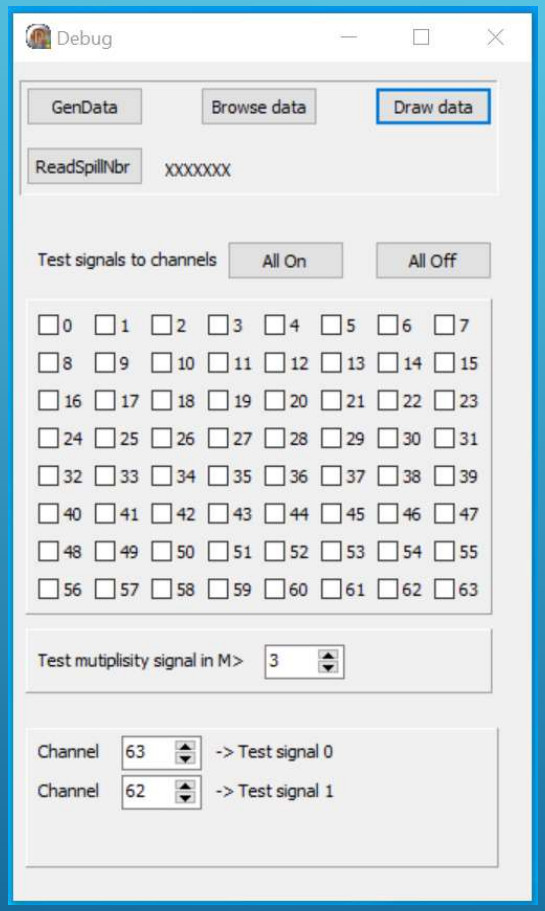
THE TRIGGER SYSTEM ELECTRONICS

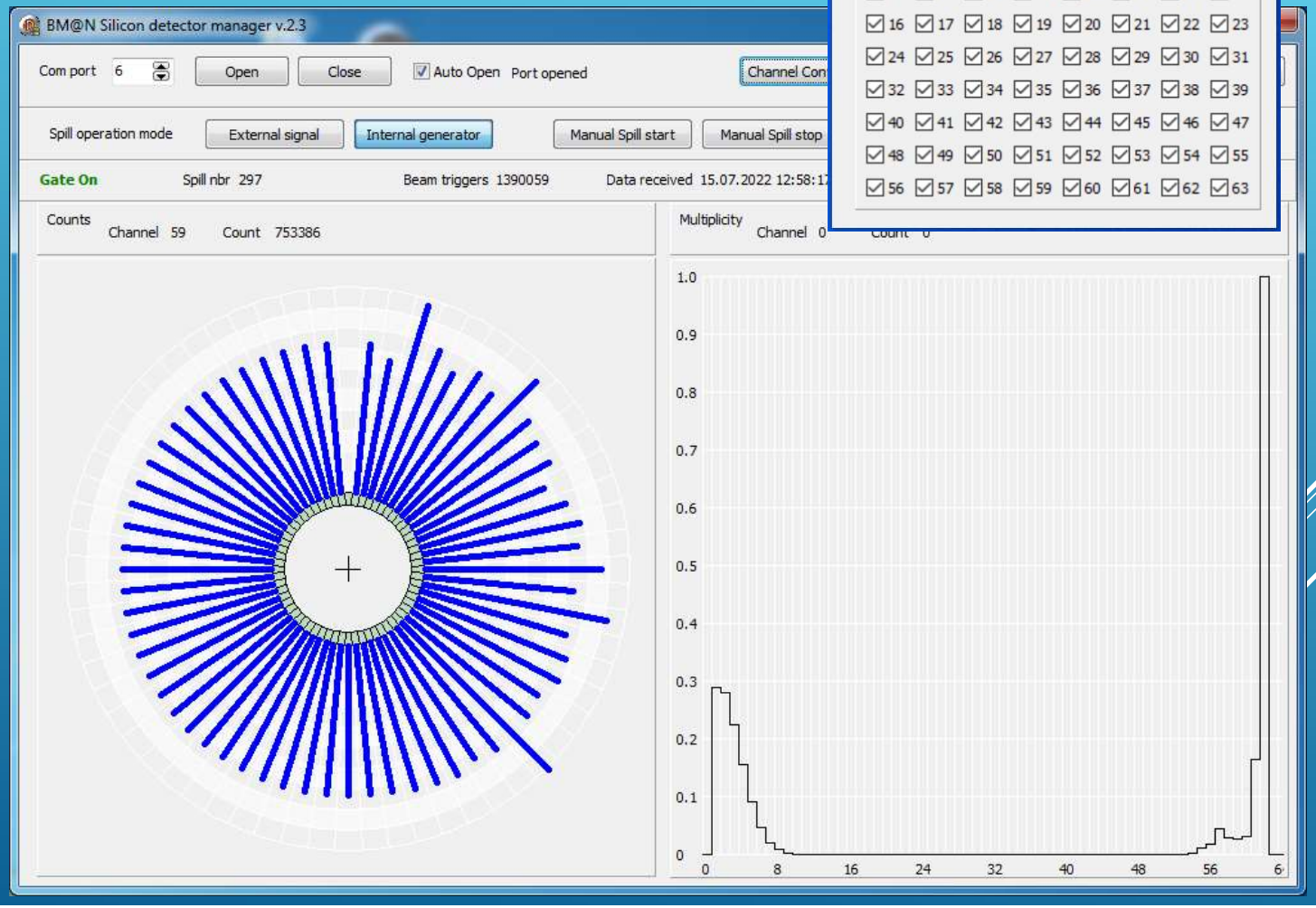
Trigger group

TRIGGER ELECTRONIC



SID MGR


Debug
GenData
Browse data
Draw data
ReadSpillNbr
xxxxxxx
Test signals to channels
All On
All Off
Test mutiplisity signal in M>
3
Channel
63
-> Test signal 0
Channel
62
-> Test signal 1

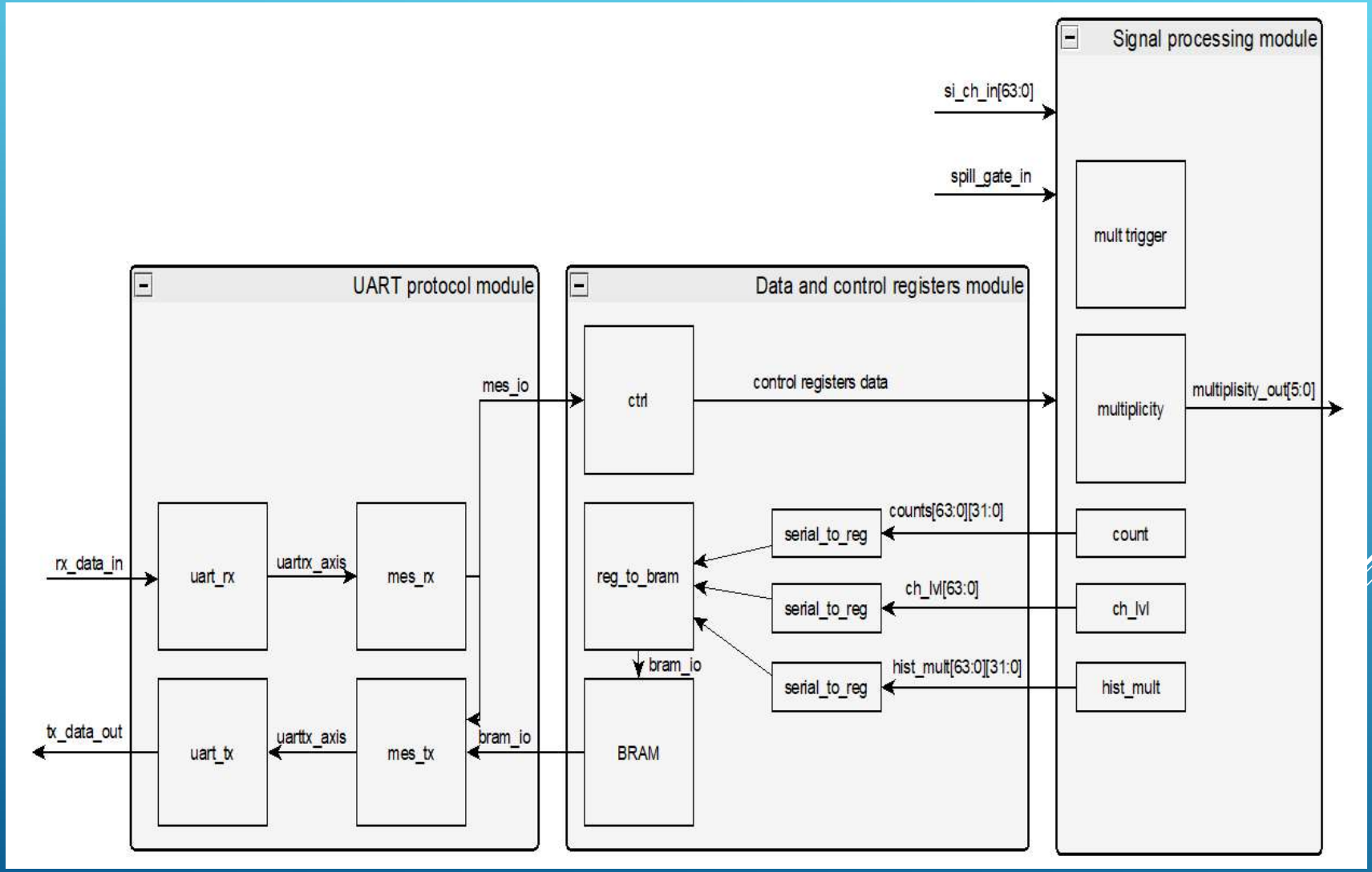

BM@N Silicon detector manager v.2.3
Com port
6
Open
Close
Auto Open
Port opened
Spill operation mode
External signal
Internal generator
Manual Spill start
Manual Spill stop
Gate On
Spill nbr 297
Beam triggers 1390059
Counts
Channel 59
Count 753386
Multiplicity
Channel 0
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
8
16
24
32
40
48
56

Channel configuration
All enabled
All disabled
Disabled channels

SIU FPGA

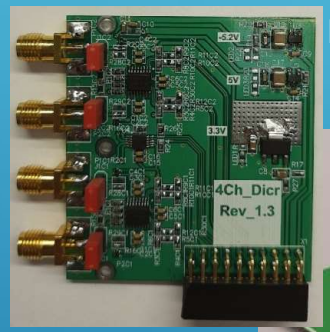
- FPGA 5CGXBC5C6F27C7 (30000 ALMs), used 32% of FPGA ALMs
- Used Quartus Prime 19.1, programming language - System Verilog
- Internal FPGA clock frequency – 50 MHz
- Communication to PC – USB virtual com-port, 115200 baud
- Compilation time – ~4 min
- Project uses synchronous design. For asynchronous signals used 200 MHz digitizing frequency
- Project built using self-containing units with defined interfaces
- Project was checked with Timing Analyzer
- SiU tested with the test signal generator developed for BM@N SiD and BD testing

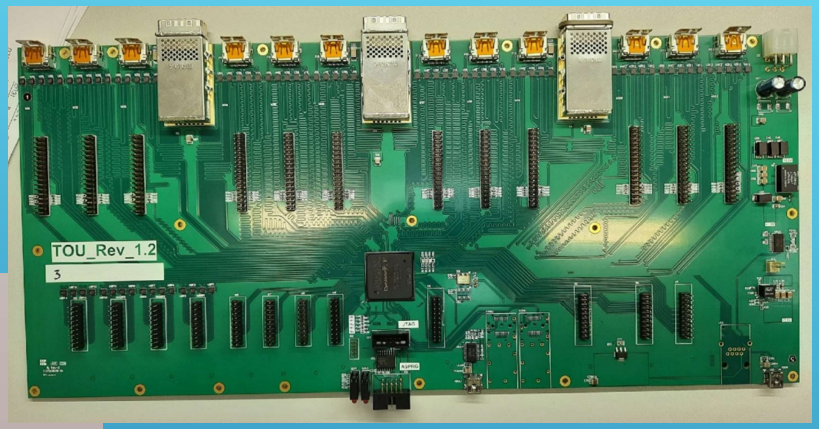
SIU FPGA II

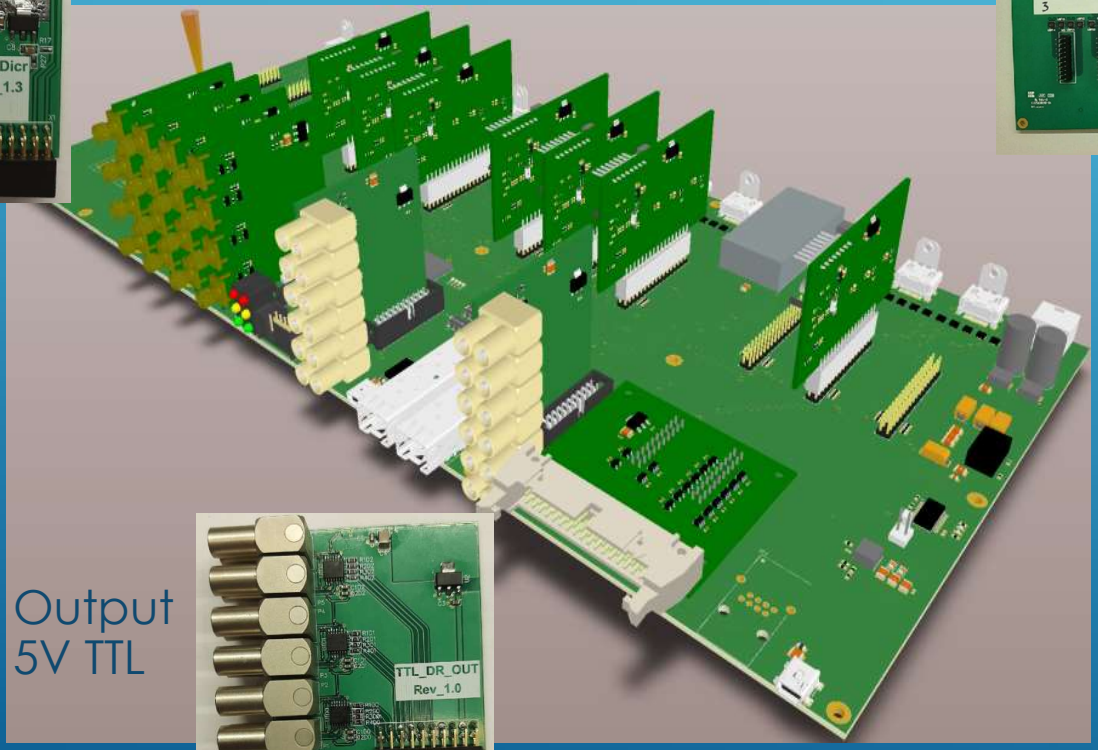

Signal processing module
si_ch_in[63:0]
spill_gate_in
mult trigger
multiplicity
multiplisity_out[5:0]
count
ch_lvl
hist_mult
counts[63:0][31:0]
ch_lvl[63:0]
hist_mult[63:0][31:0]
UART protocol module
Data and control registers module
mes_io
ctrl
control registers data
rx_data_in
uart_rx
uartrx_axis
mes_rx
reg_to_bram
serial_to_reg
serial_to_reg
serial_to_reg
bram_io
tx_data_out
uart_tx
uarttx_axis
mes_tx
bram_io
BRAM

TOU

- 4-ch. Input discriminators
- -2 to 2V input
- Threshold 5mV step
- 1.5 GHz equivalent input rise time bandwidth







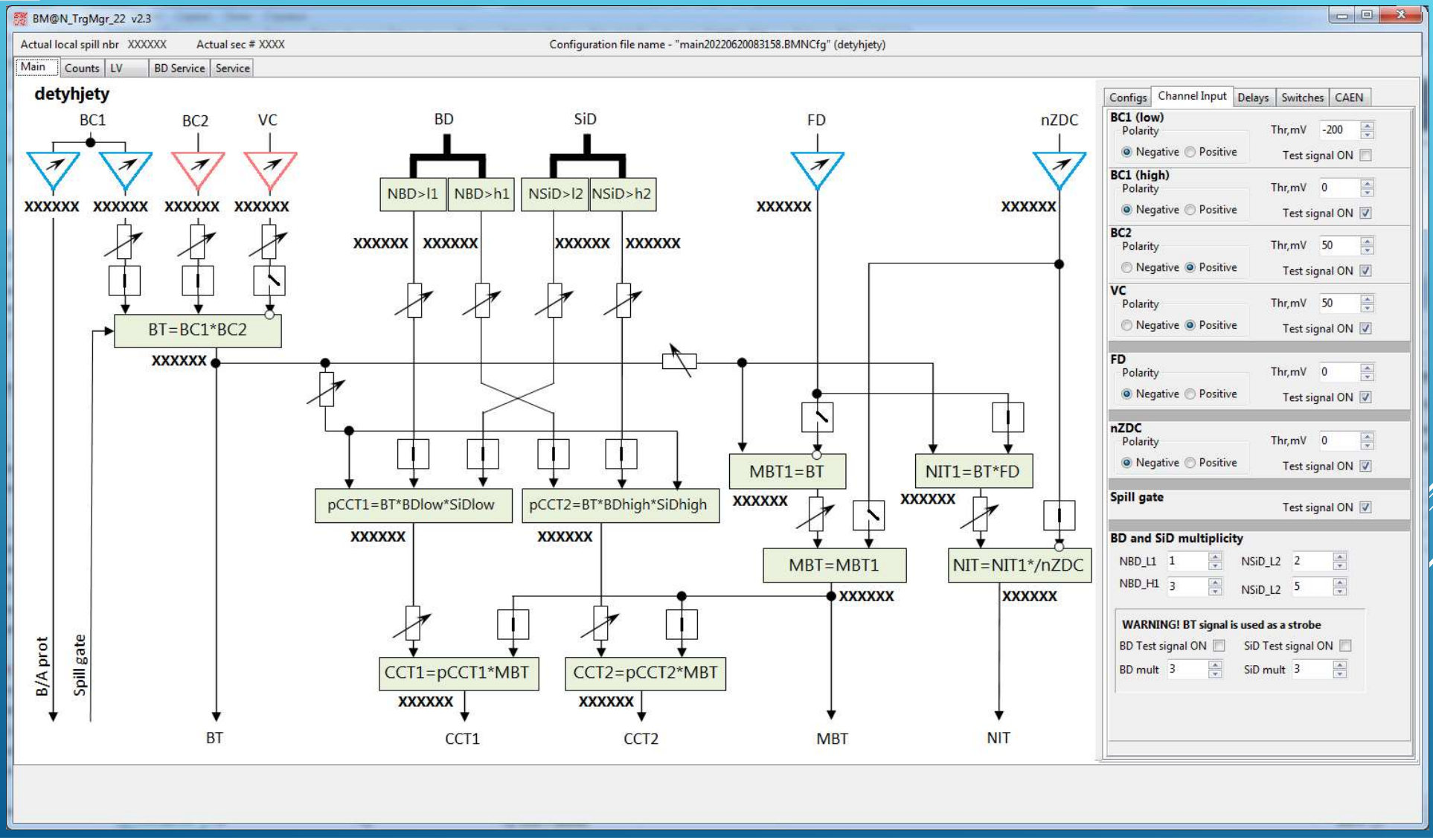
- Output 5V TTL

- **New boards ready and tested**

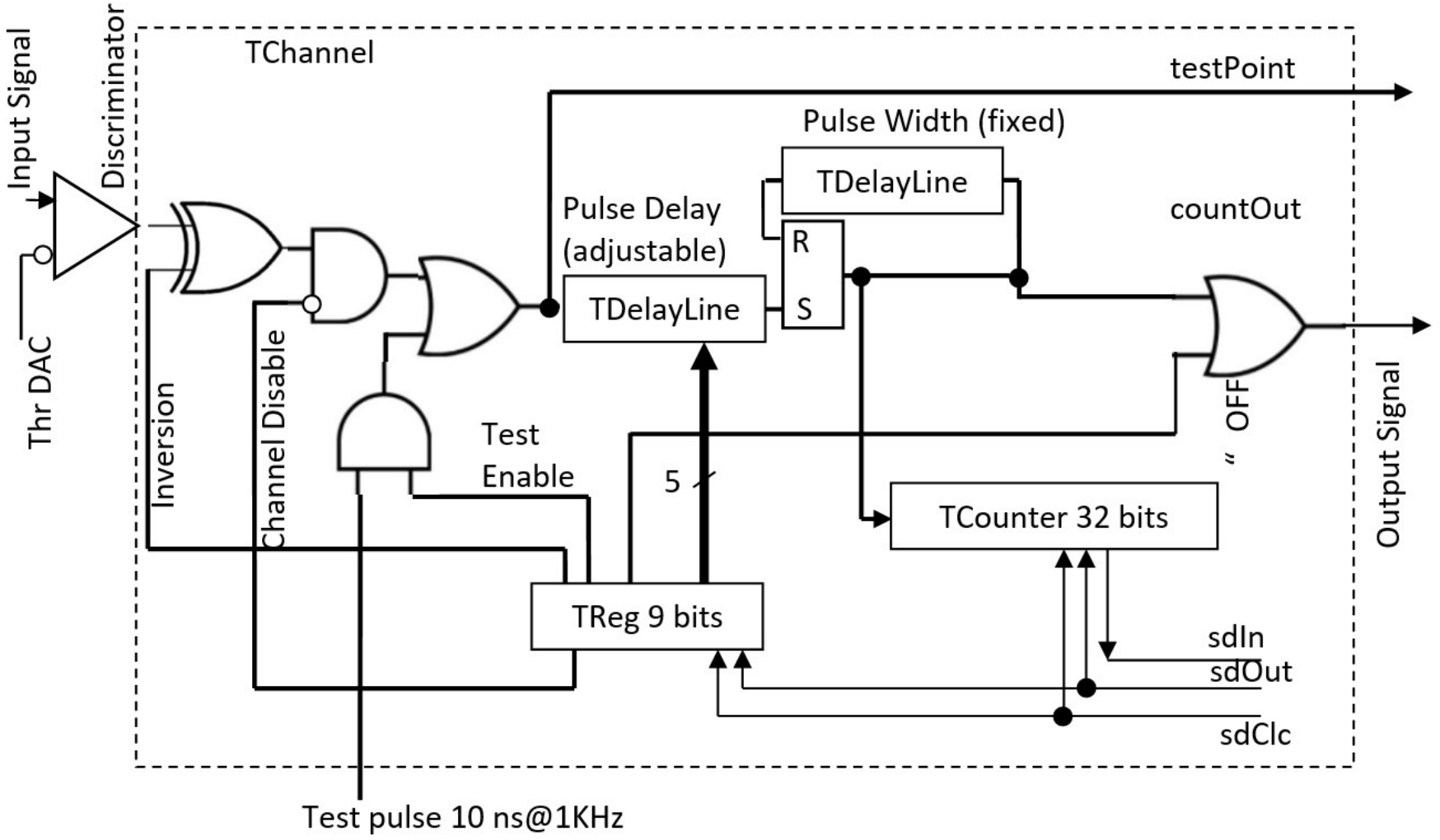
T0U FPGA

- Two external Communication lines to PC – USB virtual com-port, 115200 baud
  - Trigger control and monitoring, both I/O. **Spill data readout ~2 secs**.
  - Real-time counts reading for spill view server. 8 channel readout with 100 Hz, used by ~50%
- Internal communication – a hybrid of I2C and SPI, written from scratch
  - Signals
    - 10 MHz clock
    - Address flag
    - MOSI
    - MISO
- 26% FPGA ALMs used
- 7% connection lines used
- Compilation time ~7.5 min (old project ~ 12 hours)

T0U MGR


BM@N_TrgMgr_22 v2.3
Actual local spill nbr XXXXXX
Actual sec # XXXX
Configuration file name - "main20220620083158.BMNCfg" (detyhjety)
Main
Counts
LV
BD Service
Service
detyhjety
BC1
BC2
VC
BD
SiD
FD
nZDC
NBD>I1
NBD>h1
NSiD>I2
NSiD>h2
BT=BC1*BC2
pCCT1=BT*BDlow*SiDlow
pCCT2=BT*BDhigh*SiDhigh
MBT1=BT
NIT1=BT*FD
MBT=MBT1
NIT=NIT1*/nZDC
CCT1=pCCT1*MBT
CCT2=pCCT2*MBT
B/A prot
Spill gate
BT
CCT1
CCT2
MBT
NIT
Configs
Channel Input
Delays
Switches
CAEN
BC1 (low)
BC1 (high)
BC2
VC
FD
nZDC
Polarity
Negative
Positive
Thr,mV
Test signal ON
Spill gate
BD and SiD multiplicity
NBD_L1
NBD_H1
NSiD_L2
NSiD_L2
WARNING! BT signal is used as a strobe
BD Test signal ON
SiD Test signal ON
BD mult
SiD mult

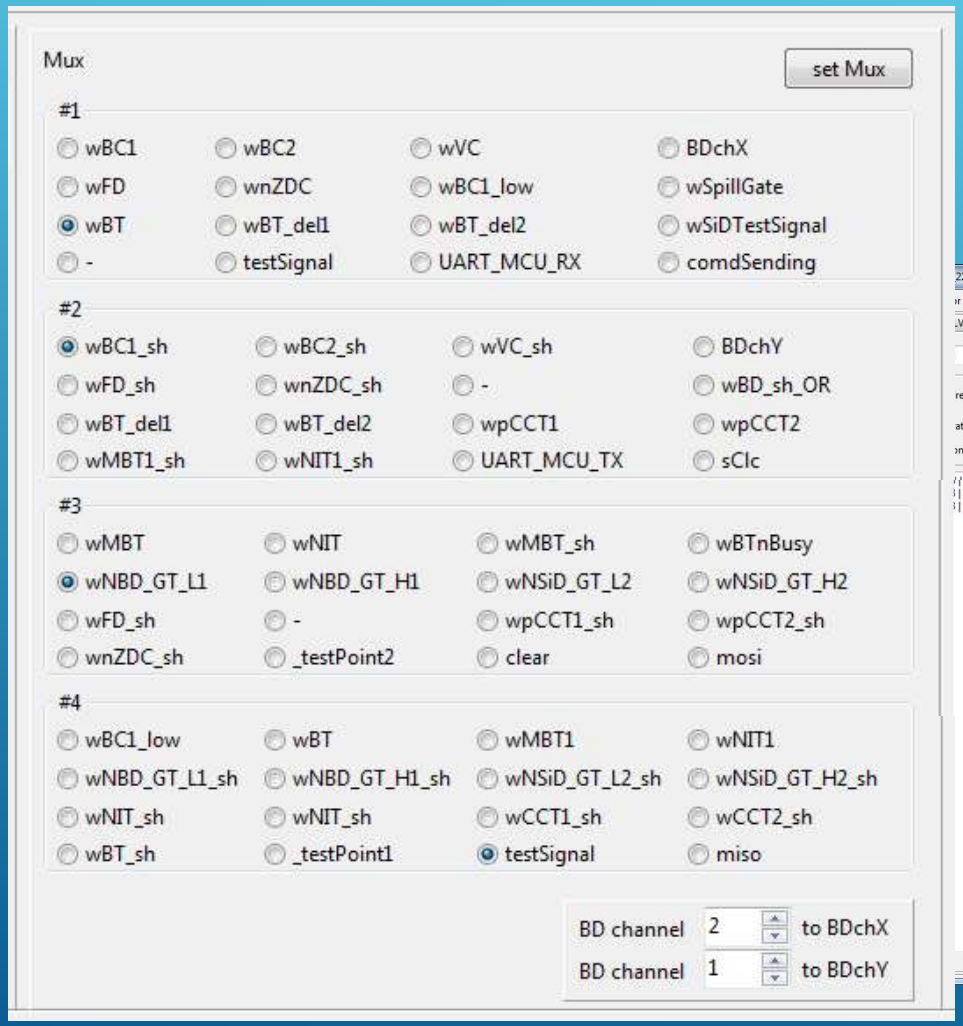
T0U CHANNEL I

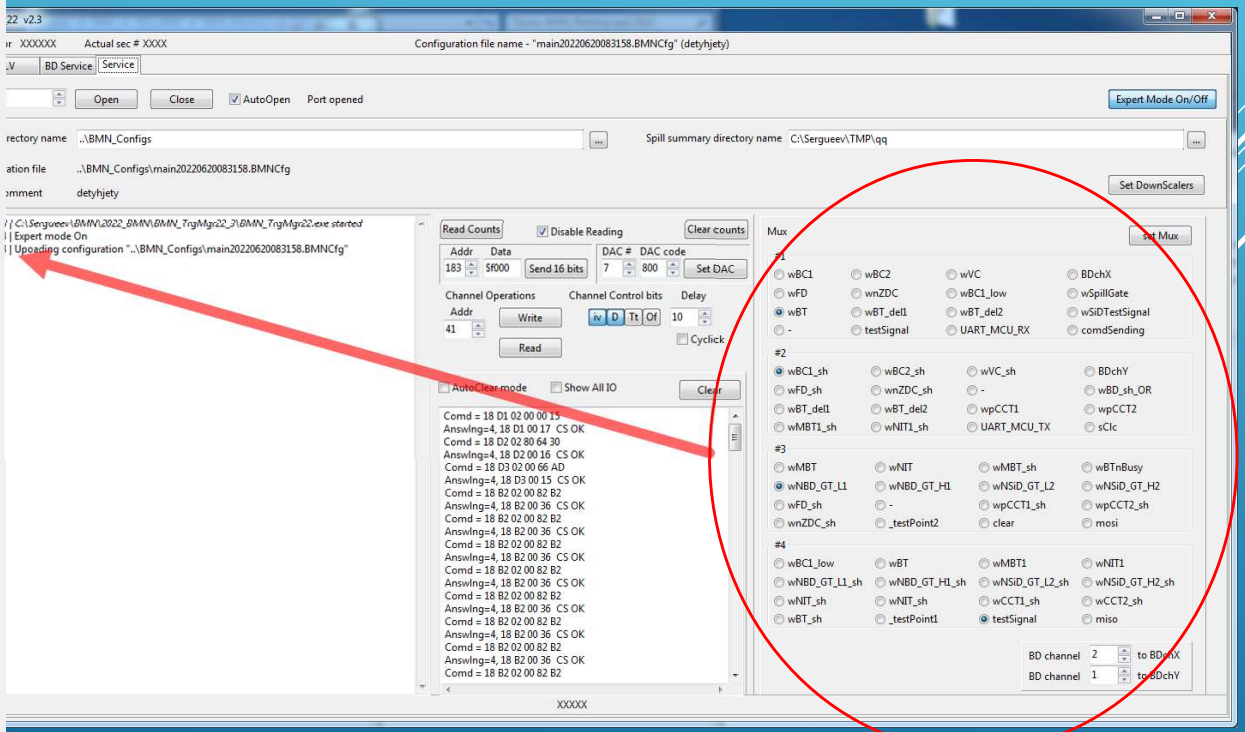


T0U CHANNEL II

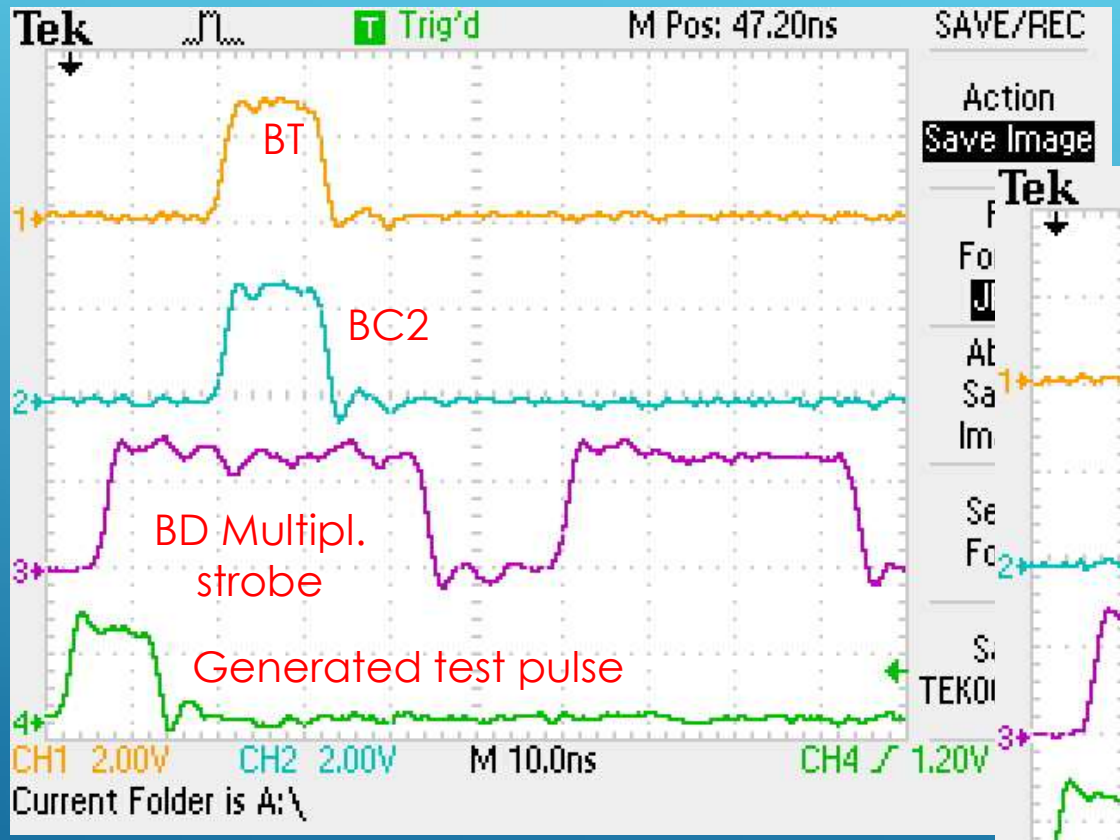
- Delay lines are asynchronous for ordinary channels with short delay and synchronous for channels with long delay
- Asynchronous delay is built using FPGA element propagation delay. Very resource consuming. Not longer than 45 ns. Step ~1.5 ns.
- Synchronous delay uses FPGA 100 MHz internal clock counting therefore introduces jitter +/- 5 ns
- Synchronous delays used in circuits with delay longer than 50 ns

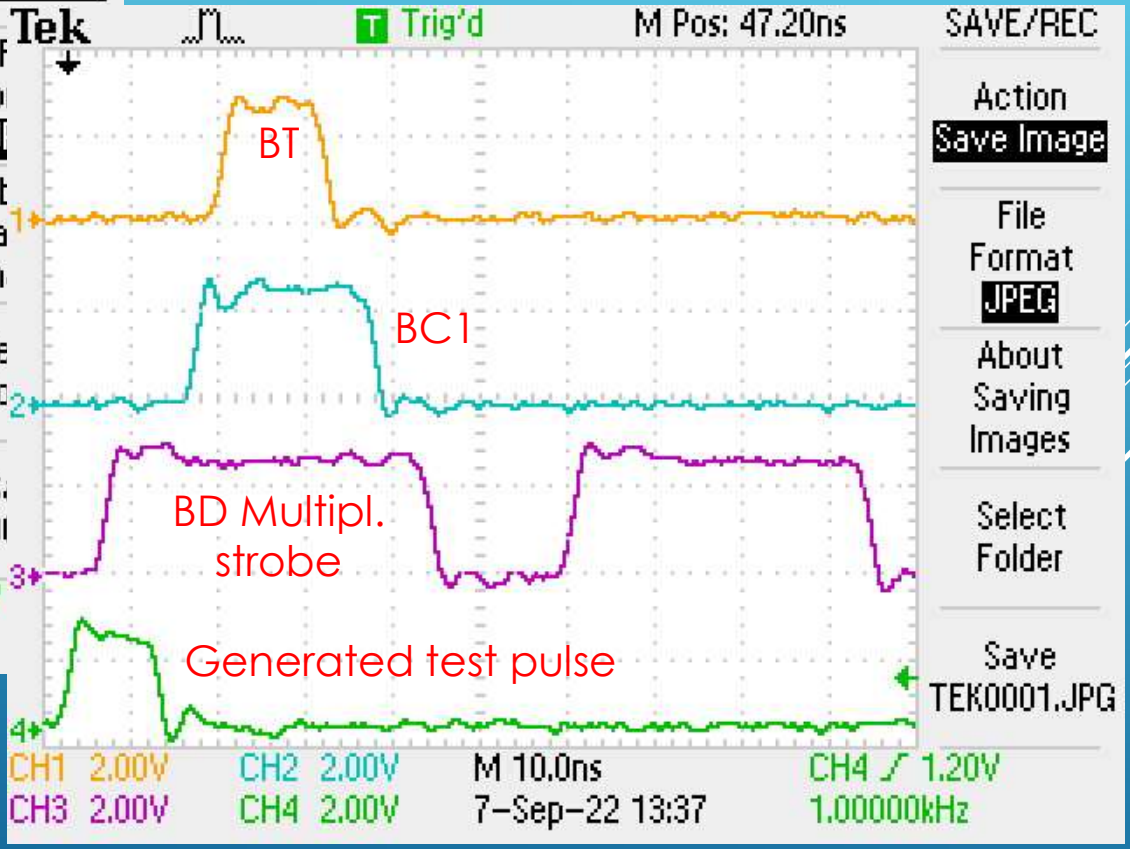
T0U ADJUSTMENT I



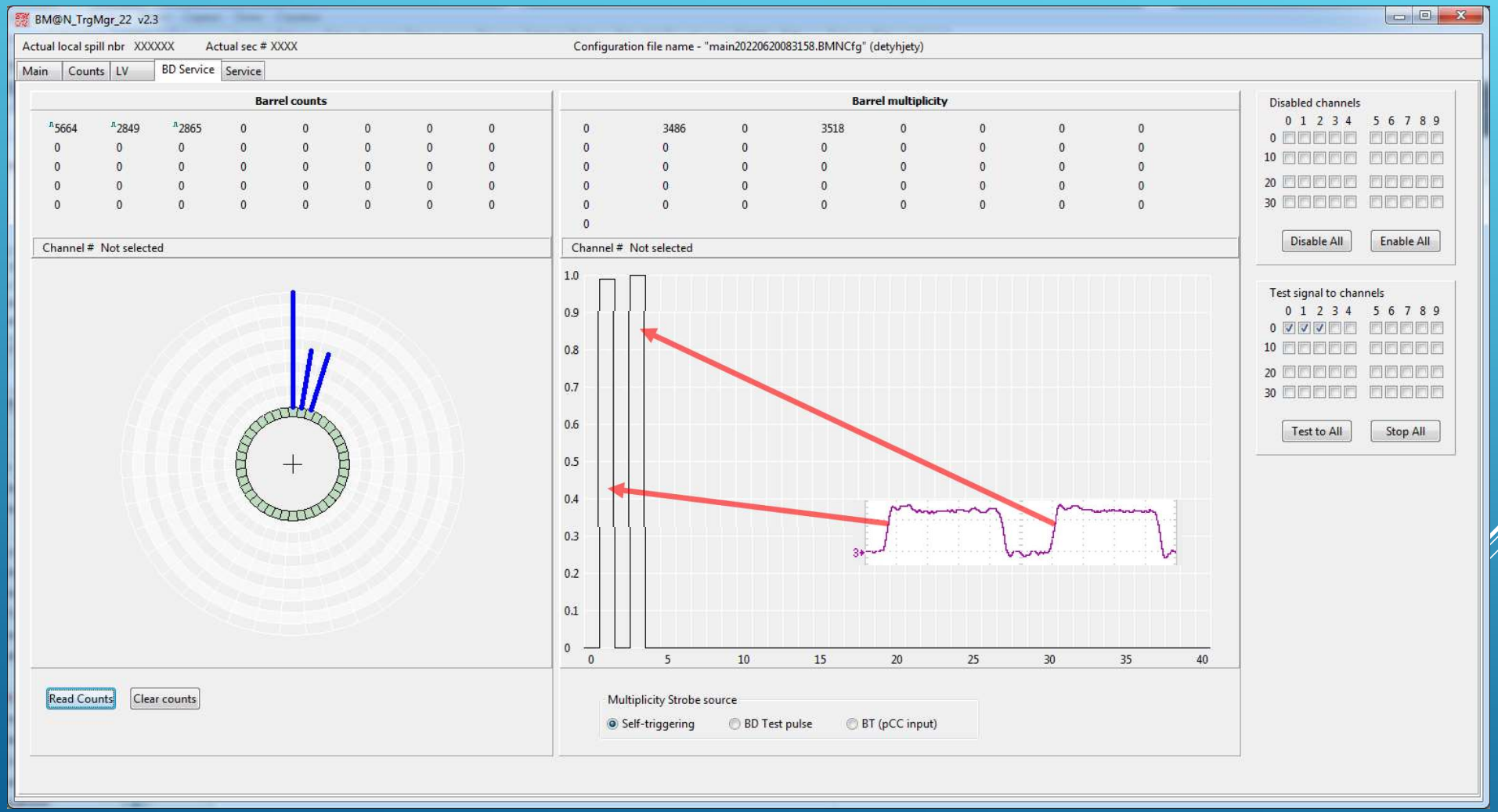


T0U ADJUSTMENT II





BD CONTROL


BM@N_TrgMgr_22 v2.3
Actual local spill nbr XXXXXX
Actual sec # XXXX
Configuration file name - "main20220620083158.BMNCfg" (detyhjety)
Main
Counts
LV
BD Service
Service
Barrel counts
Barrel multiplicity
Channel # Not selected
Channel # Not selected
Disabled channels
Disable All
Enable All
Test signal to channels
Test to All
Stop All
Read Counts
Clear counts
Multiplicity Strobe source
Self-triggering
BD Test pulse
BT (pCC input)

ACTUAL STATE

- **SiD module** ready, passed for testing to the Silicon group
- **SiD_Mgr** ready , passed for testing to the Silicon group
- **T0U** almost ready, needs to be tested with the input boards. Might be some cosmetics modifications will be needed
- **T0U_Mgr** almost ready. Some modifications will be needed
- **Web Server** under development. The SRC experiment server as a template used
- **Spill_View** under development. The SRC experiment server as a template used

- **The trigger system should be ready by the 2022 mid-October**

BM@N

Thank you