Variant of the FEE chip for STS

on behalf of NRNU MEPhI ASIC Lab
E. Atkin

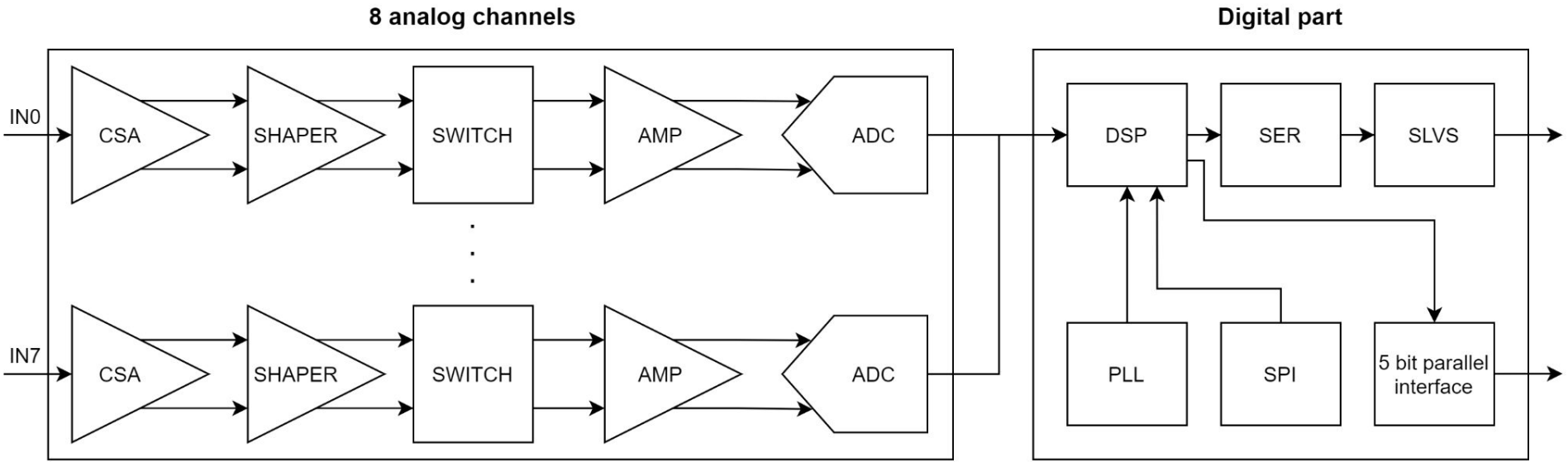
9th Collaboration Meeting of the BM@N Experiment, 14/09/22

Plan

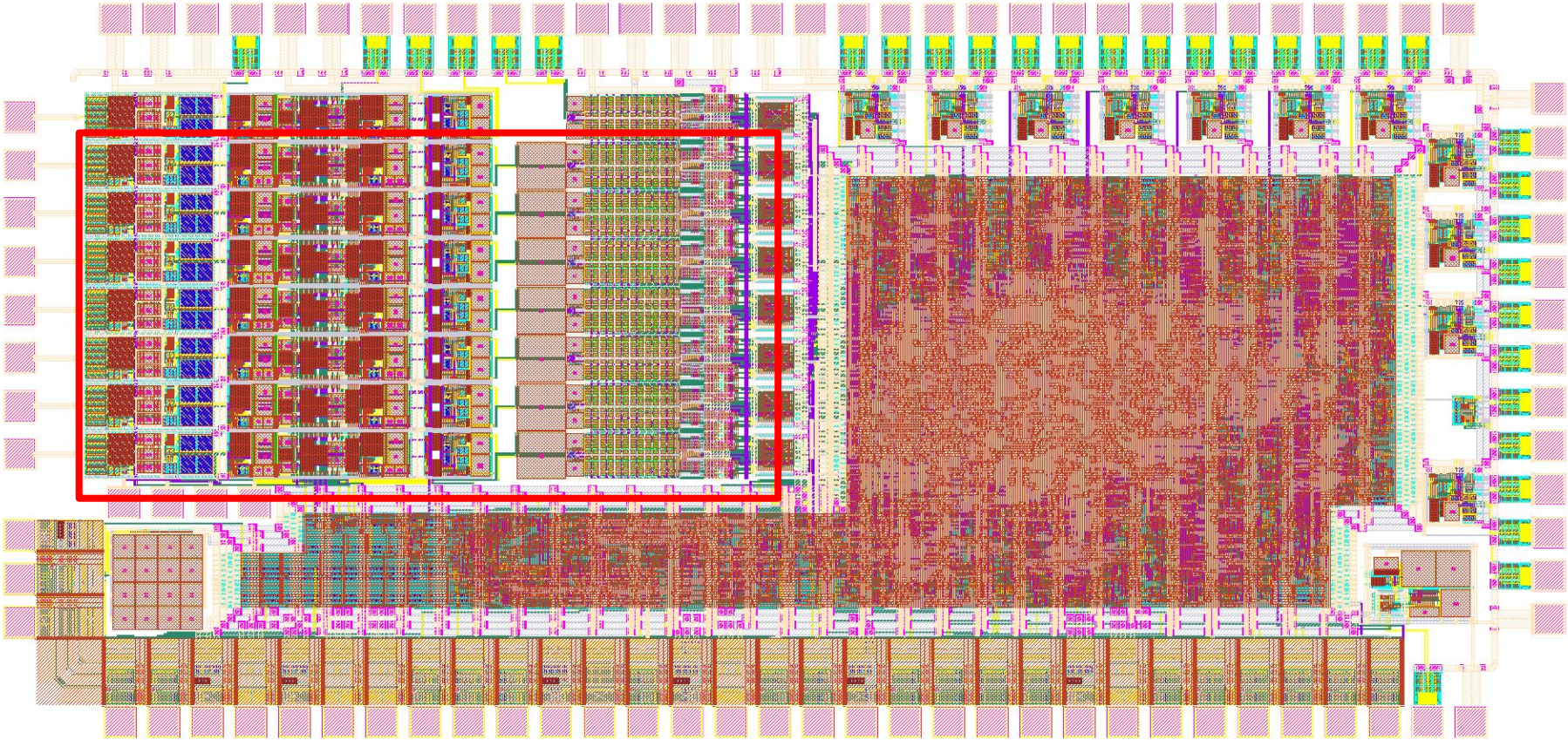
1) RSF ASIC for GEMs as a prerequisite for STS: layout, parameters, features, test boards, some results
2) RSF ASIC vs preliminary STS specifications vs STS-XYTER parameters
3) To do list
4) Technology and example projects
5) Summary

RSF ASIC for GEM detectors (Structure)

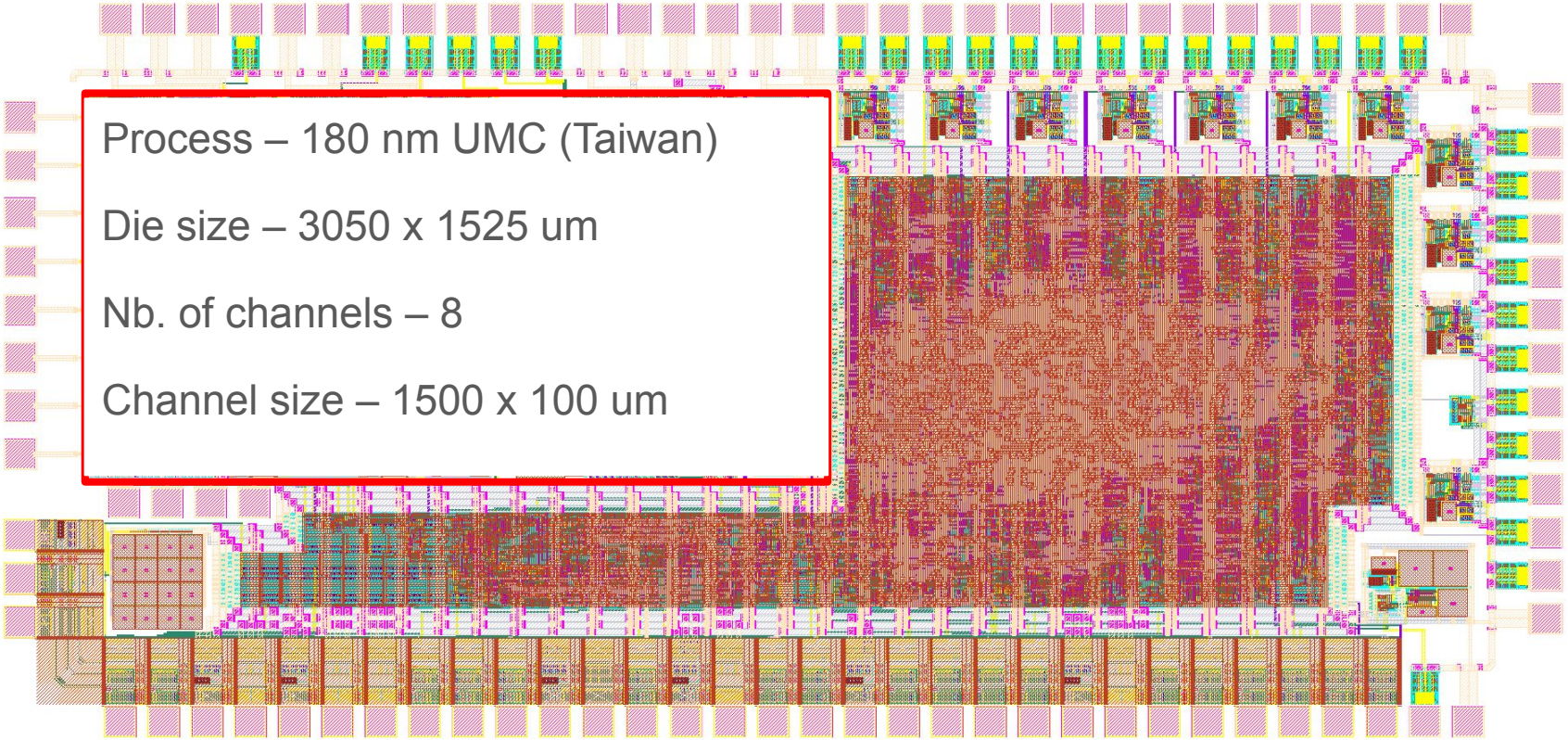
was designed under RSF Grant № 18-79-10259 (2019-21)



RSF ASIC Layout



Technology & Size



Process – 180 nm UMC (Taiwan)

Die size – 3050 x 1525 um

Nb. of channels – 8

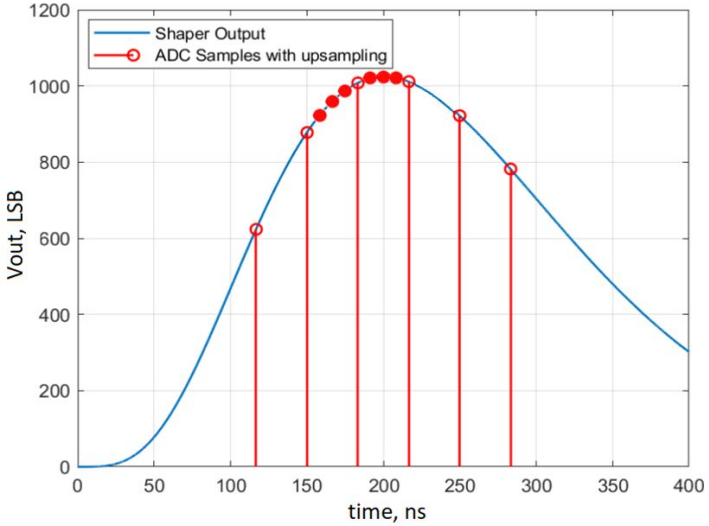
Channel size – 1500 x 100 um

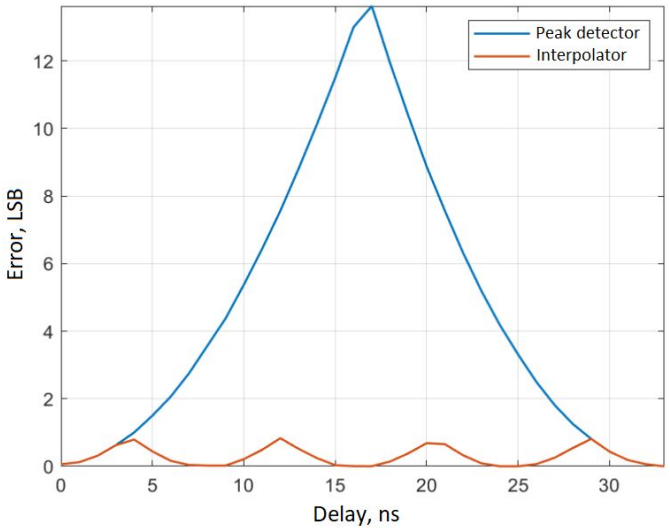
Main aim specifications for RSF ASIC

1) 8 input channels
2) Input signal amplitudes from 1 fC to 100 fC
3) Both negative and positive polarities
4) ENC 900 e at 50 pF detectors capacitance and shaping time 280 ns
5) The maximum channel rate – 1 MHz
6) 10 bit ADC at 25 MHz sampling rate
7) Total power consumption 170 mW
8) Asynchronous output with SLVS transmitter
9) DSP options – interpolation and deconvolution

DSP options

RSF ASIC DSP includes:
1) interpolation system for increase resolution of peak determine (amplitude and timestamp)
2) deconvolution system for overlay compensation





1) Implementation of Interpolation in Read-out ASIC for GEM Detectors // Russian Microelectronics, Value 50, Issue 5, pp. 353 - 356, 2021
2) Charge Sensitive Amplifier with Pseudo-differential Output // Russian Microelectronics, Value 50, Issue 3, pp. 206 - 210, 2021
3) Implementation of the interpolator for signal peak detection in read-out ASIC // JOURNAL OF INSTRUMENTATION, Value 15, Issue 116, 2020, C01017
4) An Interpolator for Signal Peak Detection in Front-end Electronics // INSTRUMENTS AND EXPERIMENTAL TECHNIQUES, Value 63, Issue 1, pp. 41 - 451, 2020

DSP options

Main publications:

1) Implementation of Interpolation in Read-out ASIC for GEM Detectors // Russian Microelectronics, Value 50, Issue 5, pp. 353 - 356, 2021

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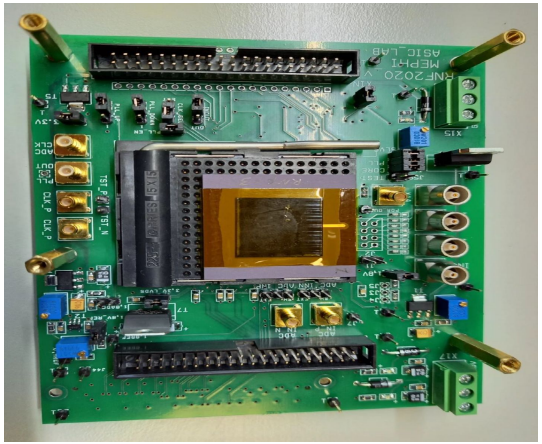
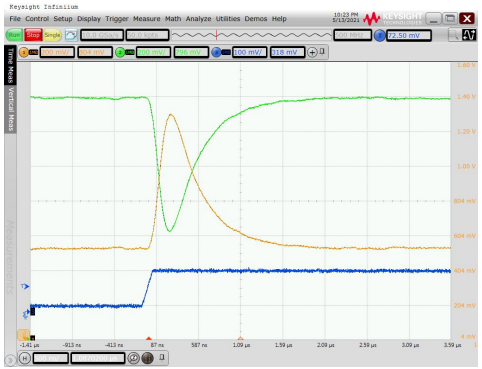
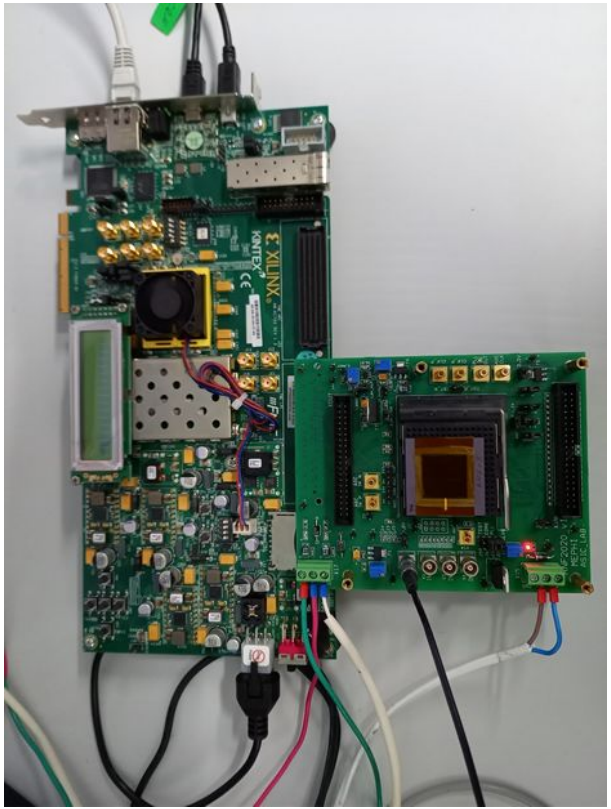
Test & Control boards

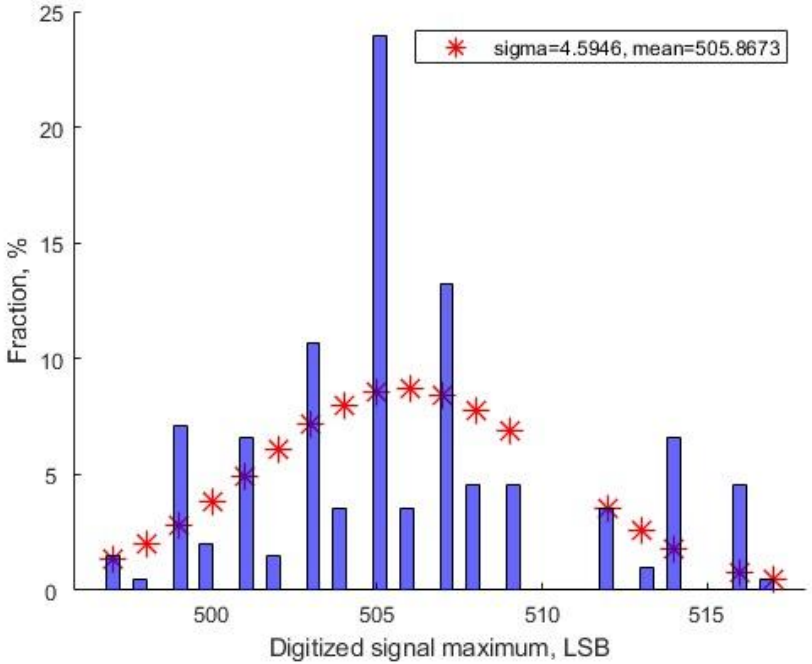
- Chip-in-socket test board
- FPGA board KC705 (Kintex 7) functionality: control, data acquisition, data transmission to PC via Ethernet





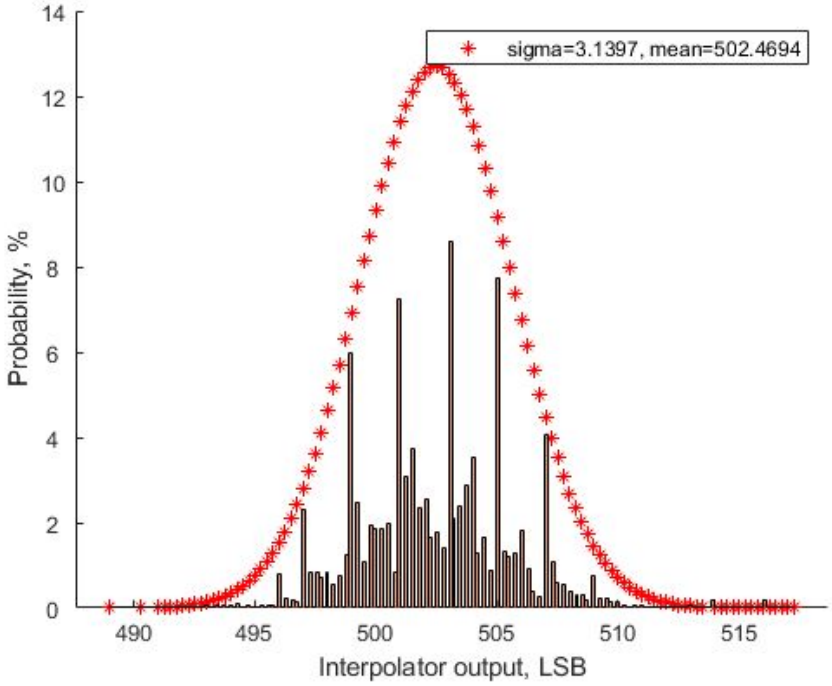


Experimental results



ADC output at 55 fC input signal (200 sampled signals)

σ = 4.6 LSB => 0.5 fC ENC



Interpolator output at 55 fC input signal (200 sampled signals)

σ = 3.14 LSB => 0.34 fC ENC

Prototype RSF ASIC vs. STS specifications

	RSF ASIC	STS specifications
Number of channels	8	128
Input signal range	1-100 fC	3.6 fC (1 mip) to 108 fC (30 mips)
Polarity	bipolar	bipolar
ENC	0.12 fC at 100 pF and 280 ns shaper 0.34 fC at 1 pF and 280 ns shaper (lab tested)	0.18 fC at 100 pF and 300 ns shaper
Maximum channel signal rate	1 MHz	500 kHz
ADC	10 bit at 25 MHz 6 bit (lab tested)	10 bit 25 MHz
Power consumption	170 mW or 5 mW/channel + 85 mW DSP + 45 mW fast interfaces	600 mW or 4.6 mW/channel (!?)
Architecture	asynchronous	triggered up to 50 MHz

ASIC vs. STS specifications

	RSF ASIC	STS specifications
Number of channels	8	128
Input signal range	1-100 fC	3.6 fC (1 mip) to 108 fC (30 mip)
Polarity	bipolar	bipolar
ENC	0.12 fC at 100 pF and 280 ns shaper 0.34 fC at 1 pF and 280 ns shaper (lab tested)	0.18 fC at 100 pF and 300 ns shaper
Maximum channel signal rate	1 MHz	500 kHz
ADC	10 bit at 25 MHz 6 bit (!) (lab tested)	10 bit 25 MHz
Power consumption	170 mW or 5 mW/channel + 85 mW DSP + 45 mW fast interfaces	600 mW or 4.6 mW/channel
Architecture	asynchronous	triggered up to 50 MHz

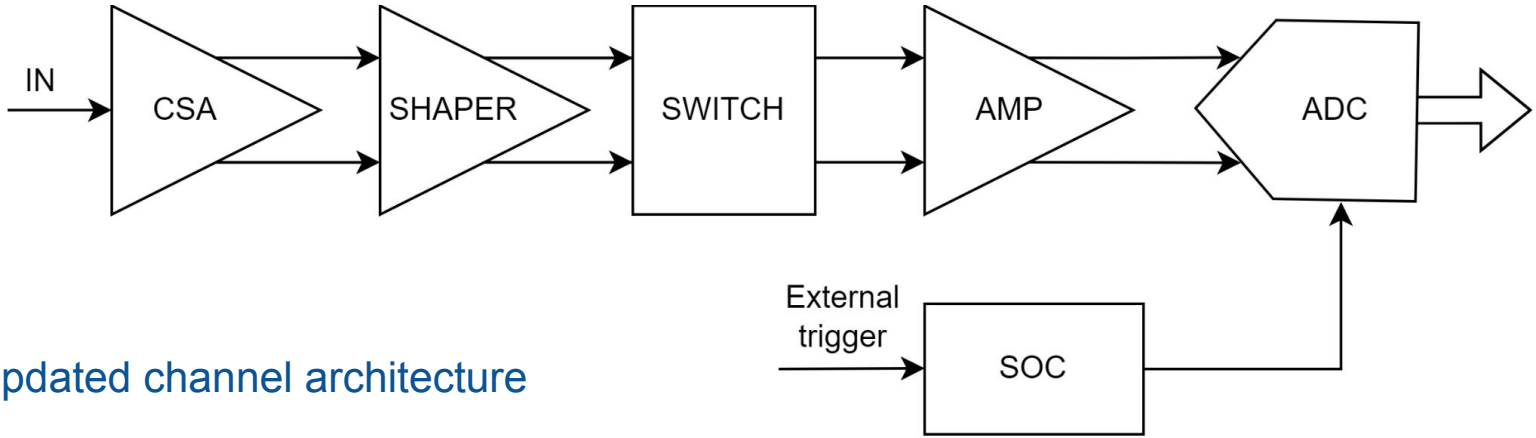
RSF ASIC vs. STS vs. XYTER*

Nb. of channels	8	128	128
Signal range	1-100 fC	3.6 fC (1 mip) to 108 fC (30 mip)	up to 15 fC (MUCH option – 1-100 fC)
Polarity	bipolar	bipolar	bipolar
ENC	0.12 fC at 100 pF and 280 ns shaper; 0.34 fC at 1 pF and 280 ns shaper (lab tested)	0.18 fC at 100 pF and 300 ns shaper	0.18 fC (50 pF) and 280 ns shaper
Hit rate	1 MHz	500 kHz	250 kHz (MUCH opt. 2 MHz)
ADC	10 bit at 25 MHz 6 bit (!) (lab tested)	10 bit 25 MHz	5 bit
Power consumption	170 mW or 5 mW/channel + 85 mW DSP + 45 mW fast interfaces	600 mW or 4.6 mW/channel	10 mW/channel (incl. logic)
Architecture	asynchronous	triggered up to 50 MHz	asynchronous

* K. Kasinski, STS-XYTER, a 128 channel readout ASIC for silicon strips, 2018 FEE, Jouvence, Canada

Main to do list

1) increase number of channels to 128
2) remove DSP, not needed
3) optimise of ADC design (to 10 bit)
4) shift to triggered (synchronous) architecture
5) design an area-efficient layout with 50 um channel pitch



Updated channel architecture

How to process: possible shift to Mikron (Zelenograd)

1) Signed are two NDAs (both with Mikron factory and RII ME)
2) Two available deployed PDKs for CMOS technological nodes of 180 and 90 nm
3) Two current projects (first projects at Mikron since 2022):
    - *NINO ASIC remake for SPD (180 nm)*
    - *Concentrator ASIC for MPD (90 nm)*
4) For STS a design of minimum 2 prototype versions and their tapeout are foreseen. Each fabrication cycle can last up to 1 year
5) The first prototype version can be manufactured at the end of 2023 (in case of fast start). Output → 100+ chips
6) Before engineering run (small volume production) it may last up to 3 years in total

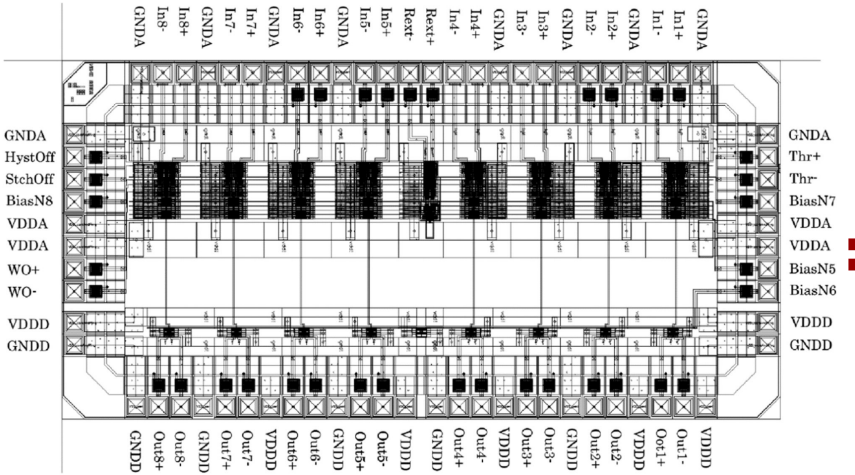
Example project - NINO ASIC remake for SPD

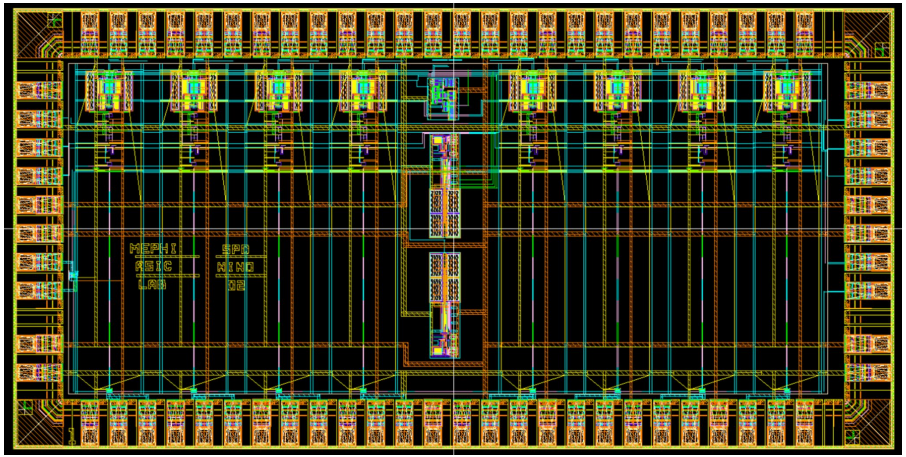
Parameter	NINO	NINO MEPHI
Dynamic range	30-2000 fC	30-2000 fC
Jitter	< 10 ps	< 15 ps
Noise (Cdet=0)	< 2500 e	< 2000 e
Peaking time	1 ns	0.4 ns
Rdiff	50-100 Ohm	35-110 Ohm
Qth	10-500 fC	10-430 fC
Stretching time	0-100 ns	0.5-100 ns

Design phase: ~2.5 months
(submitted on Aug 25, 2022)

Mikron PDK 180 nm

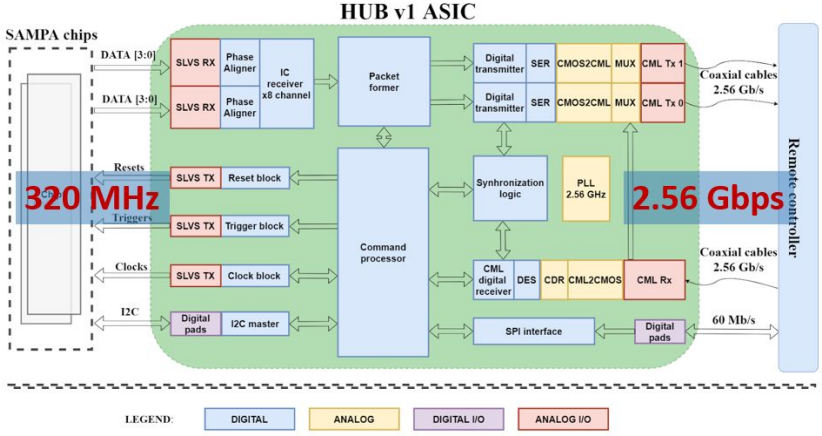
✓ Fully compatible interfaces



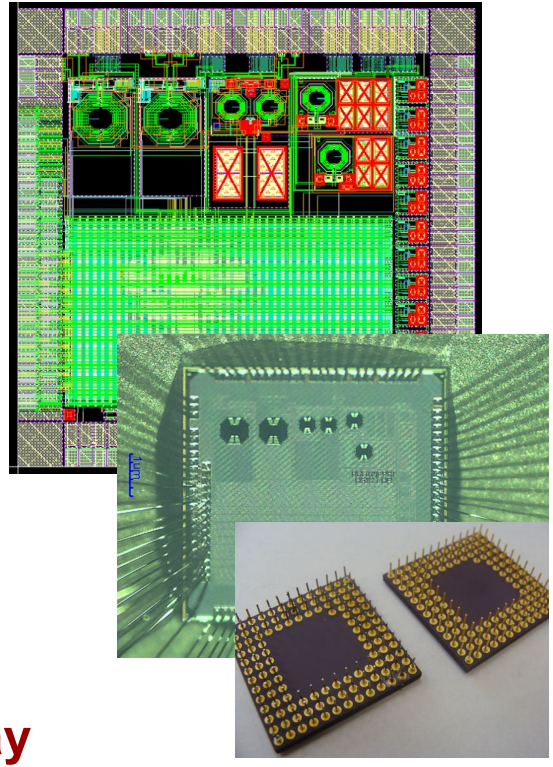


Example project - Concentrator ASIC for MPD

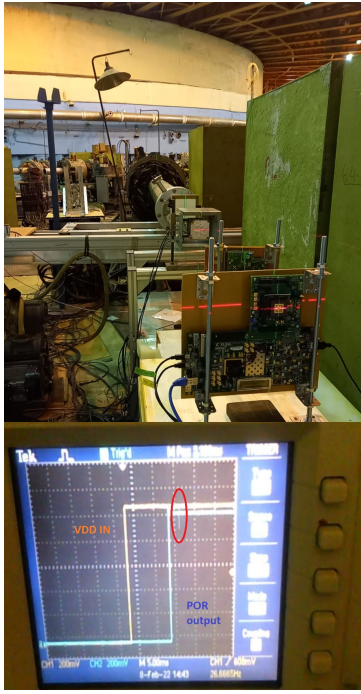
Parameter	Value
Control IO	CML 2.65 Gbps x3
Data IO	SLVS 320 Mbps x8
TID tolerance	100 MHz
Slow control	CMOS SPI, I2C
Power	500 mW
Node	TSMC 65 nm



Design phase: 6-7 months
(Oct 1 - Apr 1, 2020-21)



Heavy ion testing,
Gatchina, feb. 2022



Shift to Mikron PDK 90 nm is underway

Summary

1) RSF ASIC is a good prerequisite for STS FEE chip
2) Design of the 128 channel 10-bit triggered version should be done to fit necessary STS specs
3) Shift the new ASIC design from UMC 180 nm process to Mikron 180 nm one should be made
4) The first prototype ASIC version can be manufactured at the end of 2023