



Current status of the readout system for the MPD-ITS.

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VIII-th Collaboration Meeting of the MPD Experiment at the NICA Facility - 2021.10.13









This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 871072



> Overview.

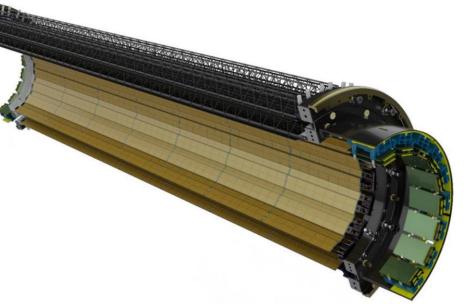
- Readout Unit Status.
- > ASIC development Status.
- Power Unit Status.
- > MAPS chip test bench.
- Prototype of Data cable, test result.
- > Conclusions.

Overview.



□ ITS OB in MPD of NICA

- Two Outer Barrel 2 layers pixels detectors
- Radial position (mm):145,195
- Length in Z: 1477 mm
- Layer 4: 18 STAVEs/Layer 5: 24 STAVEs
- ➢ 8232 MAPS 3,7 m²



Dia

Diameter of ITS case 495 mm

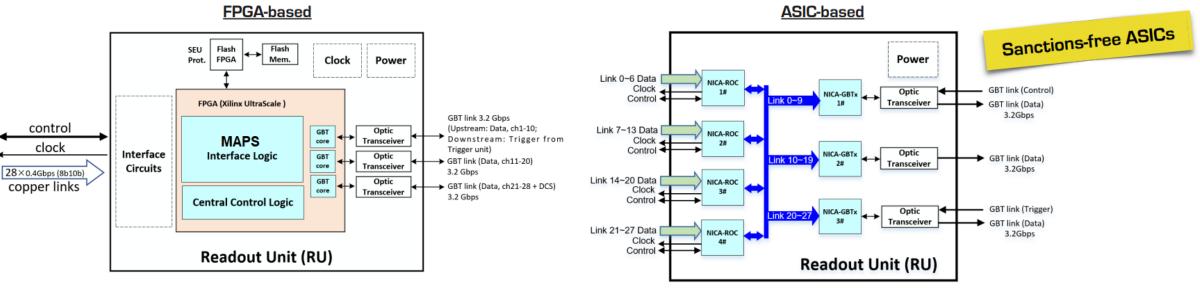
Tasks:

- □ ITS OB in MPD of NICA
- Readout Unit (RU) system Scale:
 - ✤ 42 RU modules
 - Each RU control/read out 196 MAPS chips
- Power Unit (PU) System Scale:
 - ♦ 42 PB \rightarrow 84PU
- Challenges:
 - High reliability in radioactive environments
 - High speed data transmission and real-time pre-processing (10⁸ pixels/RU)

- ◊ 1) Prototype Design of FPGA-based RU & PU (R&D by the end of Year 2022)
- 2) Engineering Version Design of FPGA-based RU (R&D by the end of Year 2023)
- 3) Engineering version Design of PU (R&D by the end of Year 2023)
- ◊ 4) Demo of ASIC-based (NICA-ROC, NICA-GBT) RU (R&D by the end of Year 2023)

RU design solutions.

MPD-ITS NICA



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- NICA_ROC: Concentrates the output data of front-end MAPS chips and transfer the packaged data to the following NICA_GBTx ASIC. It also receives control commands, clocks, and trigger signals from the backend and distributes them to MAPS chips.
- NICA_GBTx: A high-speed bidirectional data interface ASIC for optical links.
 - It receives multichannel data from the front-end (NICA_ROC), performs scrambling, encoding, frame building and serializing as the main function for the up-link direction.
 - It receives high-speed serial data from the back-end, performs CDR (Clock and Data Recovery), deserializing, decoding and distributing to the front-end as the main function for the down-link direction.
- NICA_LD (Laser Driver) and NICA_TIA (Transimpedance Amplifier): Are two analog ASICs that would be integrated together with the laser and PD (Pin Diode) in the customized optical transceiver module.
 - NICA_LD receives the high-speed up-link serial data from NICA_GBTx and amplifies the signal to driver the laser.
 - NICA_TIA receives the down-link serial signal from the pin diode, and amplifies the signal to NICA_GBTx, so that the data can be furthered processed in NICA_GBTx. These four ASICs will be introduced in the following sections.

FPGA-base RU prototype.



Recent Work

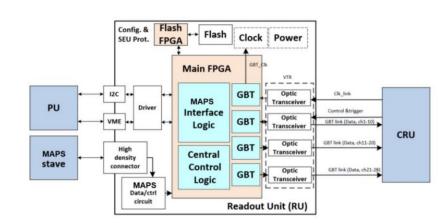
FPGA-based RU prototype V0

- · Finished the schematic design
- Finished PCB layout & fabrication
- · Soldered 2 boards for testing
- Initially tested the prototype 0 power supply
- · Tested the main FPGA and it works well

· Work plan

- · Prepare to build test platform
- · Verify the firmware

V0 Hardware Design



- Designed the FPGA based RU prototype 0 (9U size)
- · Soldered 2 RU boards for testing

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V0 Hardware Design

- RU uses high-density connectors to transfer data and control signals with MAPS staves
- Power supply from VME backplane, which is also used as one potential path for communication between RU and PU
- I²C interface is reserved on the front panel as an alternative path to communicate with PU
- Protection from SEU based on logic scrubbing, with a flash based FPGA
- Three SPF connectors with GBT fiber optic links for communication with CRU, and another SPF connector is used for clock. The others are reserved
- The main FPGA has been tested and is now working properly





Firmware Design

Firmware top-level architecture

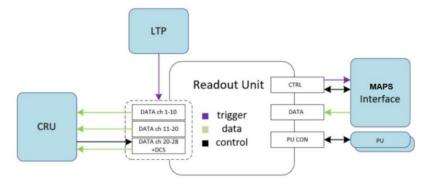
Deliver triggers to stave sensors

Receive triggers from CTP & decode

Receive "control" information from CRU

Control, configure and monitors stave sensors

Receive data from stave, decode & compress



• Finished

- Finished but need to be tested
- Need to be done
- No clue

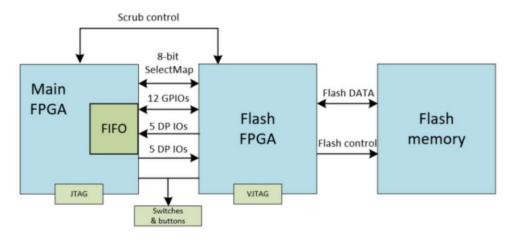
• Deliver monitoring information to CRU

- Deliver CRU frames data packets to CRU
- Monitor and control Power Board
- Handle radiation upsets I programmable logic (& sensors)

Firmware Design of the Flash FPGA

Flash FPGA firmware purpose:

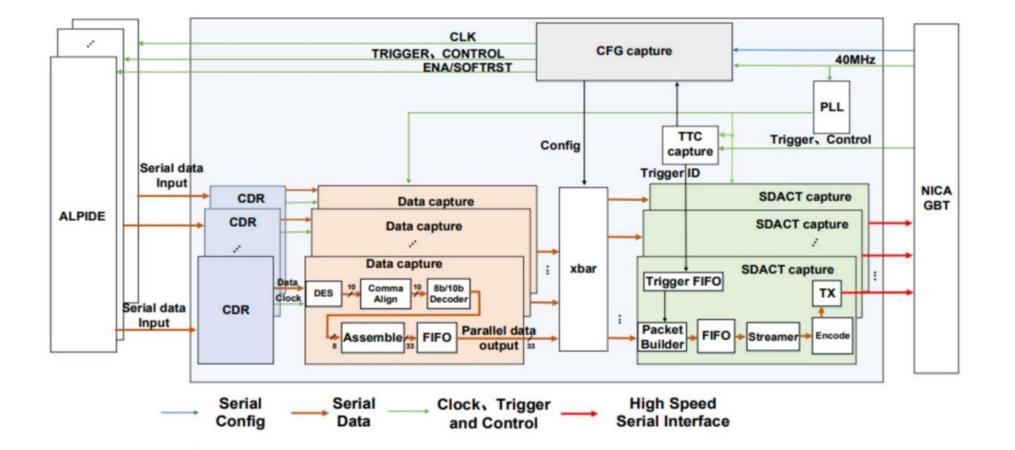
- · Re-program main FPGA from SelectMap
- Read and store the main FPGA firmware in flash memory
- Communicate with main FPGA for SEU protection



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RU firmware process:



• NICA_ROC: Concentrates the output data of front-end MAPS chips and transfer the packaged data to the following NICA_GBTx ASIC. It also receives control commands, clocks, and trigger signals from the backend and distributes them to MAPS chips.

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MPD - ITS



Recent work

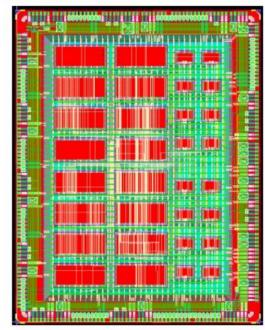
> NICA ROC ASIC design

- Finished the Back End design
- Placement and routing
- Post layout simulation
- Signoff and Tape out
- > NICA ROC ASIC test board design
 - Finished the test plan design
 - Finished device selection

Work Plan

- > To finish test board schematic design
- > To finish test board PCB layout design

Layout



- Areas: 5.7mm×4.5mm
- Pins: 247
- Package: QFP256

43 (43)

0 (0)

max fanout

max length

Violating Paths: 0 0 0 0 0 All Paths: 10032 7384 246 2992 Hold mode all reg2reg reg2cgate defau WNS (ns): 0.002 0.143 0.678 0.002	WNS	(ns):	0.03/	0.03/	0.005	0.1/0
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	max_tran	1 6	9 (0)	0.000	9	(37)

-26

θ

Placement and Routing report

57 (57)

0 (0)

Setup time

Hold time

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NICA_GBT, NICA_LD/RX ASICs and Customized Optical Module.

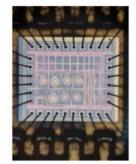


NICA_GBT, NICA_LD/Rx ASICs

Three chips of the first tape-out(December, 2020) in a standard 55 nm CMOS technology have been tested and successfully verified.



PLL+Deser Chip Part of NICA GBT core



LDLA Chip For 1Tx+1Rx optical module

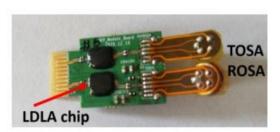


LDAr Chip For multi-Tx/Rx optical module

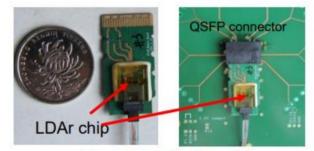
> The next tape-out is scheduled to be around the end of 2021. It will include the first complete NICA GBT analog core (eTx/eRx, PLL, CDR, Des/Ser, PhaseAligner, etc..), and the second version of LDLA/LDAr chips.

Customized Optical Module

Two types of customized optical modules are under development.



1Tx1Rx optical module



4Tx array optical module

- The further development of the optical modules (to replace CERN VTTx/VTRx) modules) is ongoing together with the iteration of the LDLA/LDAr chips.
- After the second tape out of LDLA/LDAr in the end of this year, the customized optical modules are also planned to be updated and integrated with the new LDLA/LDAr.

https://indico.cern.ch/event/820476/contributions/4372791/

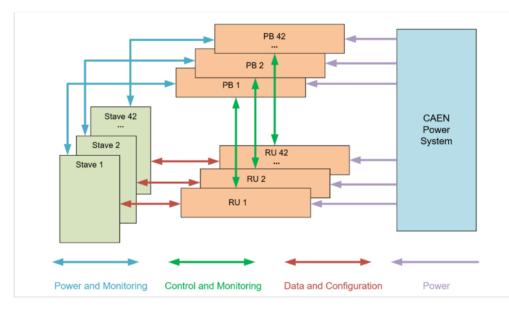
A 14 Gbps optical transceiver LDLA14 fabricated in a 55 nm CMOS process has been designed and tested for NICA MPD project. Wideopen 14 Gbps eyes have been captured in both Tx and Rx directions, BER less than 10–12 has been achieved in the optical loop test.

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Structure of the power system of MPD-ITS



- The PU supplies 1.8 V positive power, as well as negative power used as bias for the staves.
- In addition to supplying power to the staves, the PU is also controlled by RU through the serial interface to implement the following functions:
 - Separate enabling of power channels and bias channels.
 - Adjusting the power supply voltage separately.
 - Adjusting the bias voltage in one PU.
 - Over current protection with adjustable threshold on each power channel.
 - Overheat protection on each PU.
 - Monitoring of voltage, current and temperature.

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Recent work

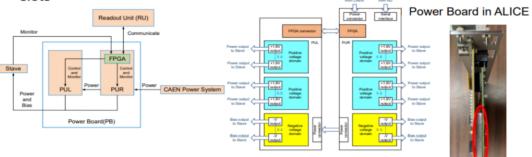
- NICA PU design
 - o Have clarified interface with CAEN power system, Power Board Breakout Board and RU
 - Have clarified communication protocols with RU
 - Have began prototype PU schematic design

Work plan

- To finish prototype PU schematic design
- To finish prototype PU PCB layout design
- To test prototype PU

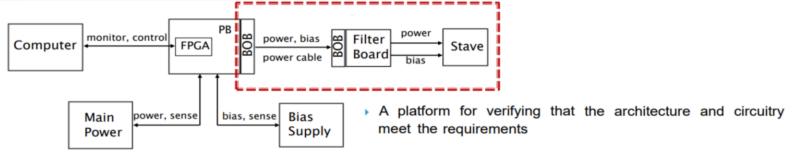
Design of PU

- The Power Board is composed by two Power Units
- Each Power Unit supplies 8 channels (16 converters, 8 for analogue and 8 for digital power rails)
- > A flash FPGA on PUR controls both PUR and PUL and responsible for communications with RU
- > The cooling plate is sandwiched between the two boards providing cooling and mechanical support, and the resulting entity fits 2 VME slots



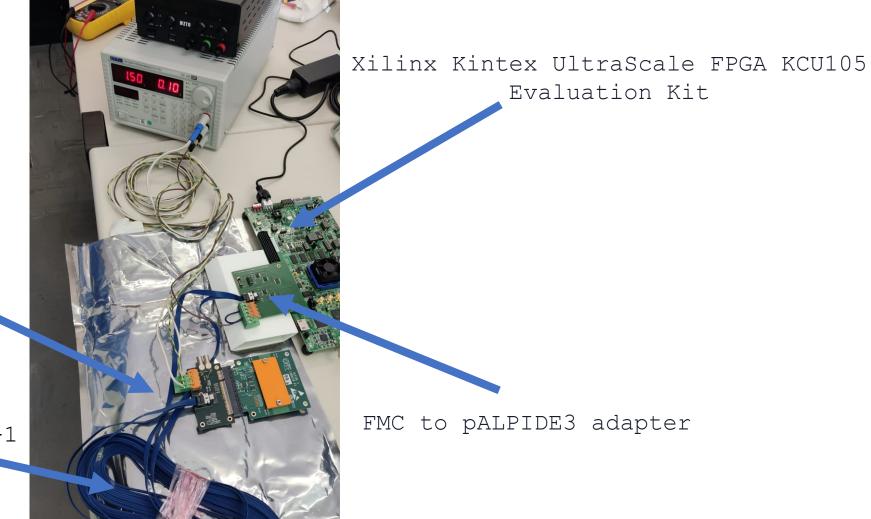


Test of prototype PU



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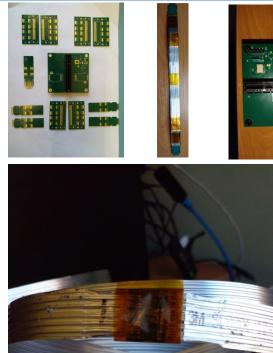


pALPIDE3 carrier v3

ECUE-12-999-T1-FF-01-1

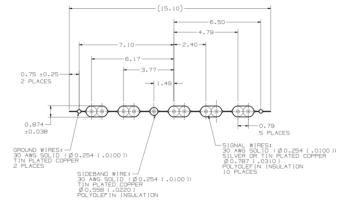
Prototype of Data cable using 3M twin axial cable , SL8800 series

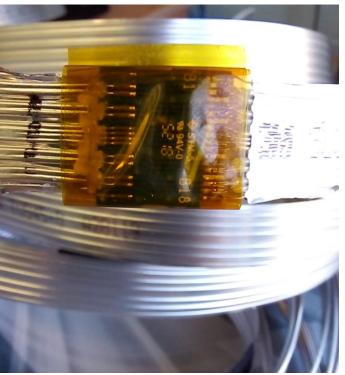






³M™ TWIN AXIAL CABLE, SL8800 SERIES





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Test result of cable (8 m) base on 3M twin axial cable , SL8800 series

2021-Oct-08 13:45:53

Vertical increment

Vertical range:

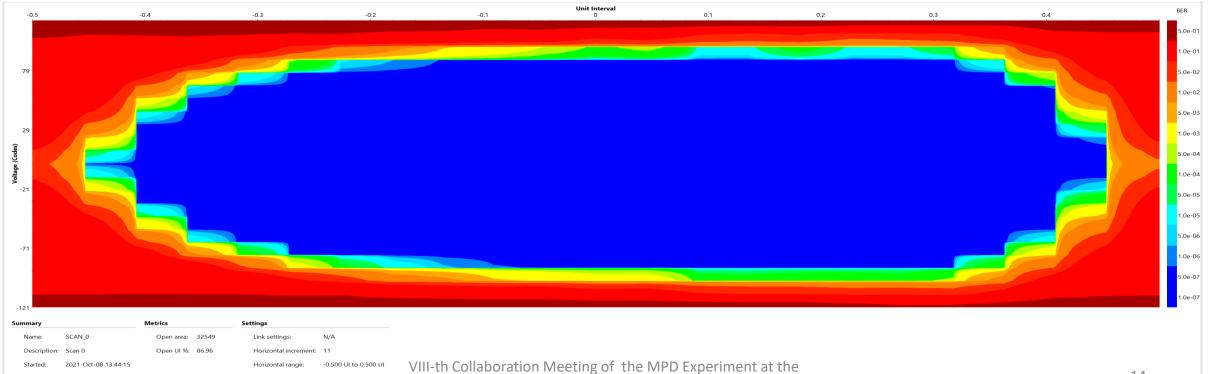
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Hardware	? _ 🗆 🖒 ×	Tcl Console	Messages Seria	I I/O Links Seria	I I/O Scans	× Intellige	nt Design Runs																							? _ 🗆 🖸
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№ MGT_X0Y7	NO LINK																													



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- > Two unit of the first prototype of a RU based on Kintex Utrascale FPGA are under test.
- The initial firmware architecture is already designed and it need to be tested, as part of the design the components needed for Radiation effect mitigation are included.
- > The specifications of PU are already defined, we have plan to finish the design and constructions of the first prototype.
- The works related to the design and development of the NICA_GBT, NICA_LD / RX ASICs are well advanced and is expected to be completed in the planned time.
- A 14 Gbps optical transceiver LDLA14 fabricated in a 55 nm CMOS process has been designed and tested for NICA MPD project. Wide-open 14 Gbps eyes have been captured in both Tx and Rx directions, BER less than 10⁻¹² has been achieved in the optical loop test.
- We were able to build in the lab a data prototype cable with vary good performance using a commercially available cable, then we need to think how to scale the construction to production version.

BACKUP

Backup (12 m 3M cable)

? _ _ _

Tcl Console Messages Serial I/O Links Serial I/O Scans × Intelligent Design Runs

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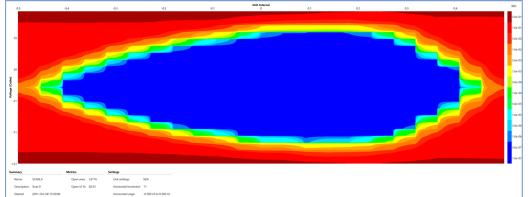
Tcl Console Messages Serial I/O Links × Serial I/O Scans Intelligent Design Runs

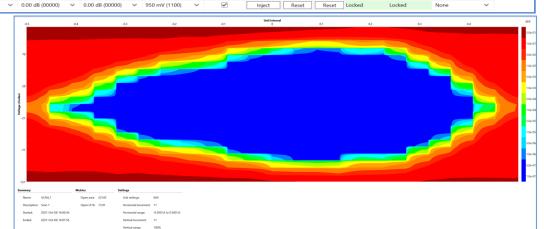
Vertical range: 1009

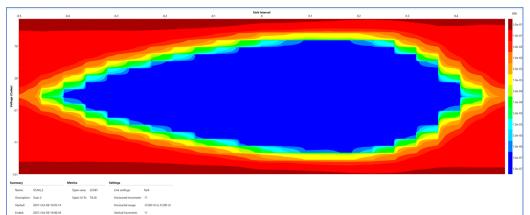
Vertical range: 100%

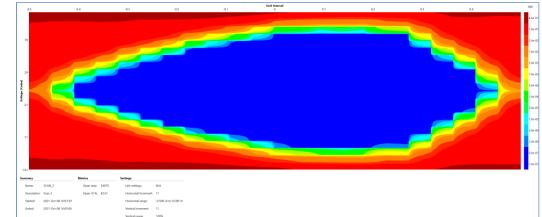
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Backup (10 m Samtec cable)



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