Current status of the readout system for the MPD-ITS.

Lei Zhao (USTC), Di Guo (CCNN) & Raúl Arteche Díaz (JINR & CEADEN) for the MPD-ITS Collaboration.

VIII-th Collaboration Meeting of the MPD Experiment at the NICA Facility - 2021.10.13

RUSSIAN FOUNDATION FOR BASIC RESEARCH
№ 18-02-40119

CREMLIN PLUS
Connecting Russian and European Measures for Large-scale Research Infrastructures

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 871072

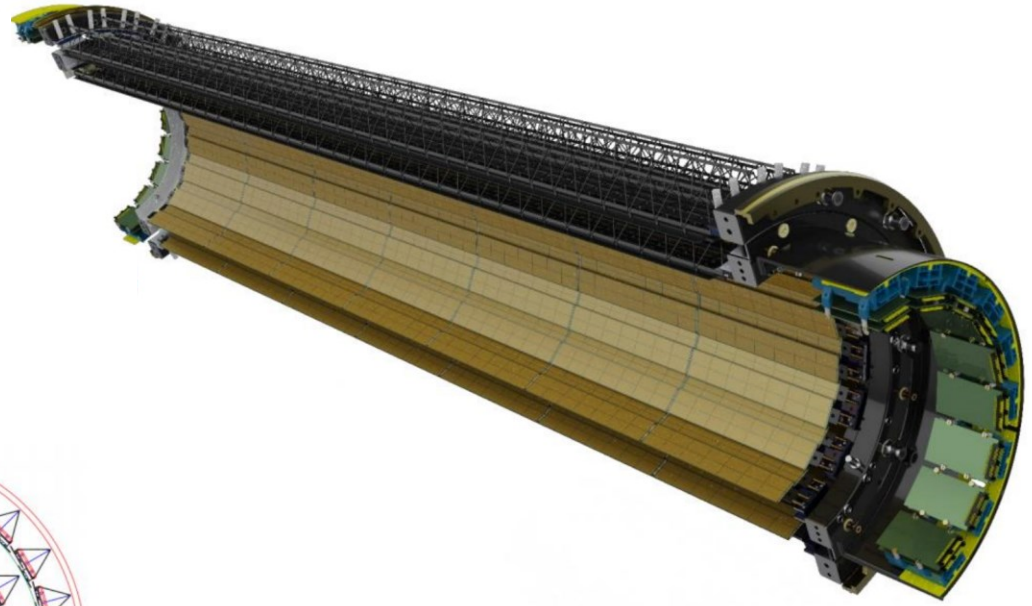
Outline

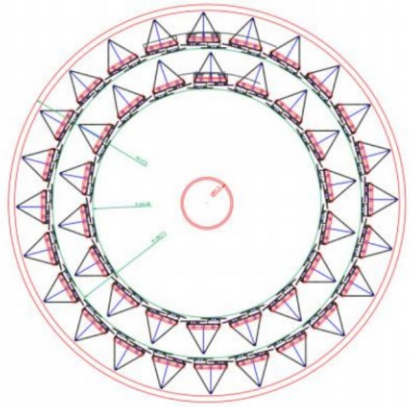
- Overview.
- Readout Unit Status.
- ASIC development Status.
- Power Unit Status.
- MAPS chip test bench.
- Prototype of Data cable, test result.
- Conclusions.

Overview.

❑ ITS OB in MPD of NICA

- Two Outer Barrel 2 layers pixels detectors
- Radial position (mm):145,195
- Length in Z: 1477 mm
- Layer 4: 18 STAVEs/Layer 5: 24 STAVEs
- 8232 MAPS 3,7 m^2





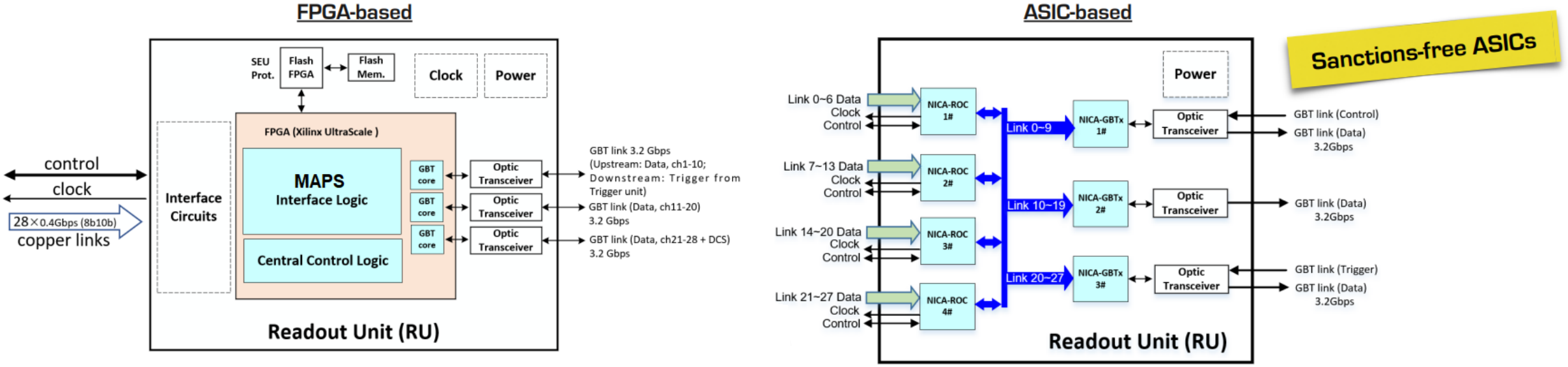
Diameter of ITS case
495 mm

❑ ITS OB in MPD of NICA

- Readout Unit (RU) system Scale:
  - 42 RU modules
  - Each RU control/read out 196 MAPS chips
- Power Unit (PU) System Scale:
  - 42 PB → 84PU
- Challenges:
  - High reliability in radioactive environments
  - High speed data transmission and real-time pre-processing (10^8 pixels/RU)

- Tasks:
  - 1) Prototype Design of FPGA-based RU & PU (R&D by the end of Year 2022)
  - 2) Engineering Version Design of FPGA-based RU (R&D by the end of Year 2023)
  - 3) Engineering version Design of PU (R&D by the end of Year 2023)
  - 4) Demo of ASIC-based (NICA-ROC, NICA-GBT) RU (R&D by the end of Year 2023)

RU design solutions .



UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA

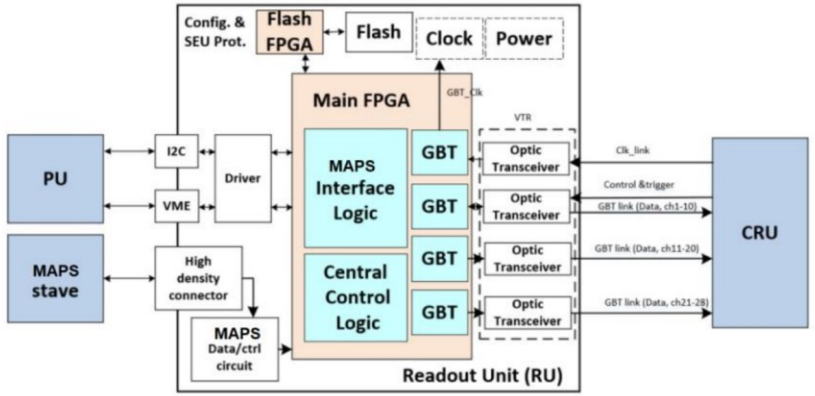
- **NICA_ROC:** Concentrates the output data of front-end MAPS chips and transfer the packaged data to the following NICA_GBTx ASIC. It also receives control commands, clocks, and trigger signals from the backend and distributes them to MAPS chips.
- **NICA_GBTx:** A high-speed bidirectional data interface ASIC for optical links.
  - It receives multichannel data from the front-end (NICA_ROC), performs scrambling, encoding, frame building and serializing as the main function for the up-link direction.
  - It receives high-speed serial data from the back-end, performs CDR (Clock and Data Recovery), deserializing, decoding and distributing to the front-end as the main function for the down-link direction.
- **NICA_LD (Laser Driver) and NICA_TIA (Transimpedance Amplifier):** Are two analog ASICs that would be integrated together with the laser and PD (Pin Diode) in the customized optical transceiver module.
  - NICA_LD receives the high-speed up-link serial data from NICA_GBTx and amplifies the signal to driver the laser.
  - NICA_TIA receives the down-link serial signal from the pin diode, and amplifies the signal to NICA_GBTx, so that the data can be furthered processed in NICA_GBTx. These four ASICs will be introduced in the following sections.

FPGA-base RU prototype.

Recent Work

- **FPGA-based RU prototype V0**
  - Finished the schematic design
  - Finished PCB layout & fabrication
  - Soldered 2 boards for testing
  - Initially tested the prototype 0 power supply
  - Tested the main FPGA and it works well
- **Work plan**
  - Prepare to build test platform
  - Verify the firmware

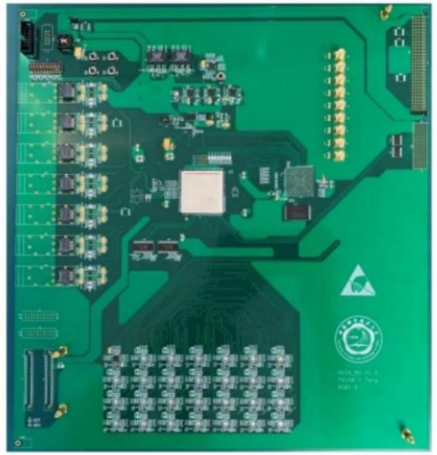
V0 Hardware Design



- Designed the FPGA based RU prototype 0 (9U size)
- Soldered 2 RU boards for testing

V0 Hardware Design

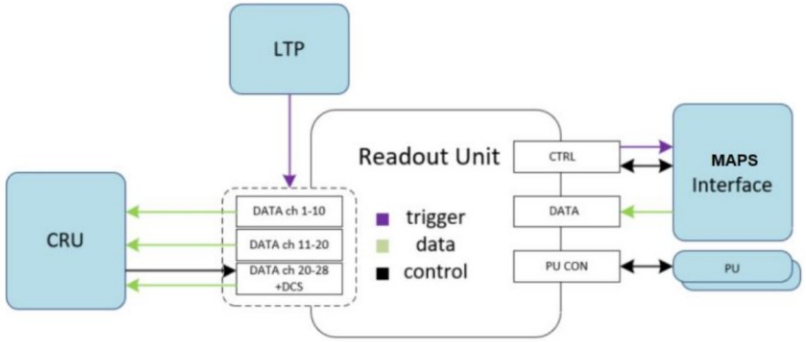
- RU uses high-density connectors to transfer data and control signals with MAPS staves
- Power supply from VME backplane, which is also used as one potential path for communication between RU and PU
- I^2C interface is reserved on the front panel as an alternative path to communicate with PU
- Protection from SEU based on logic scrubbing, with a flash based FPGA
- Three SPF connectors with GBT fiber optic links for communication with CRU, and another SPF connector is used for clock. The others are reserved
- The main FPGA has been tested and is now working properly



UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA

FPGA-base RU Firmware.

Firmware Design



- Finished
- Finished but need to be tested
- Need to be done
- No clue

RU firmware process:

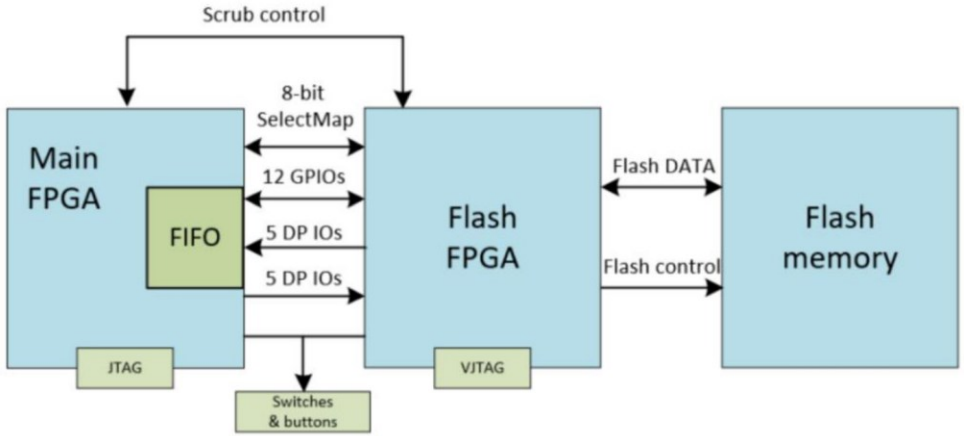
- Firmware top-level architecture
- Receive triggers from CTP & decode
- Receive “control” information from CRU
- Deliver triggers to stave sensors
- Control, configure and monitors stave sensors
- Receive data from stave, decode & compress

- Deliver monitoring information to CRU
- Deliver CRU frames data packets to CRU
- Monitor and control Power Board
- Handle radiation upsets I programmable logic (& sensors)

Firmware Design of the Flash FPGA

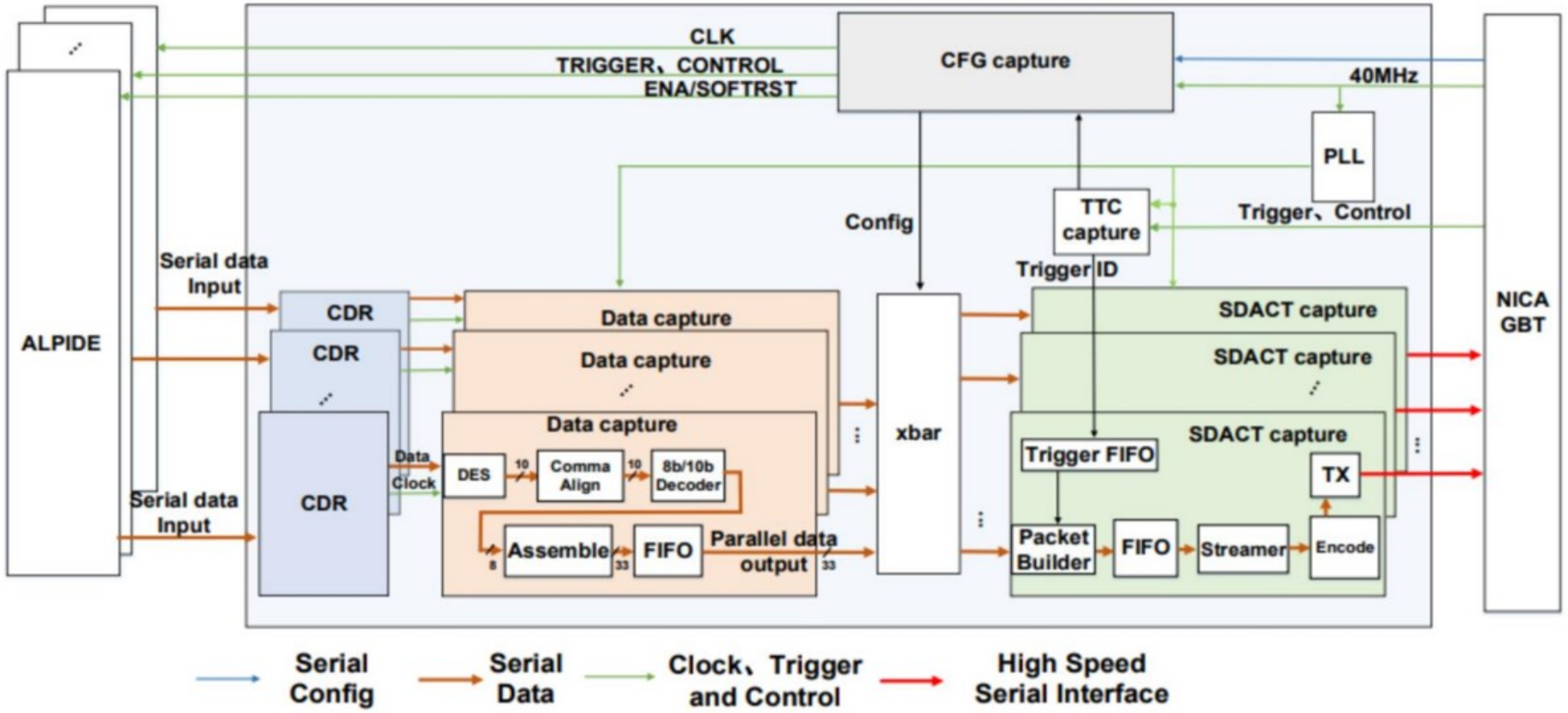
Flash FPGA firmware purpose:

- Re-program main FPGA from SelectMap
- Read and store the main FPGA firmware in flash memory
- Communicate with main FPGA for SEU protection



UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA

NICA_ROC ASIC Design



- **NICA_ROC:** Concentrates the output data of front-end MAPS chips and transfer the packaged data to the following NICA_GBTx ASIC. It also receives control commands, clocks, and trigger signals from the backend and distributes them to MAPS chips.

UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA

NICA ROC ASIC status.

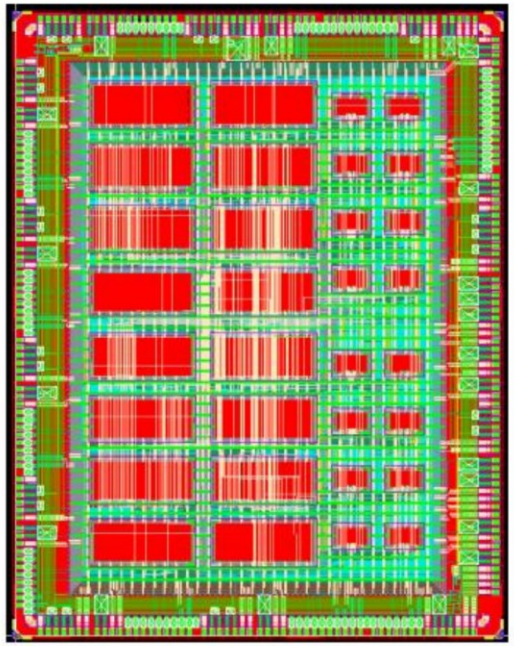
Recent work

- NICA ROC ASIC design
  - Finished the Back End design
  - Placement and routing
  - Post layout simulation
  - Signoff and Tape out
- NICA ROC ASIC test board design
  - Finished the test plan design
  - Finished device selection

Work Plan

- To finish test board schematic design
- To finish test board PCB layout design

Layout



- Areas：5.7mm×4.5mm
- Pins：247
- Package：QFP256

Placement and Routing report

Setup mode	all	reg2reg	reg2cgate	default
WNS (ns):	0.037	0.037	0.065	0.176
TNS (ns):	0.000	0.000	0.000	0.000
Violating Paths:	0	0	0	0
All Paths:	10032	7384	246	2992

Setup time

Hold mode	all	reg2reg	reg2cgate	default
WNS (ns):	0.002	0.143	0.678	0.002
TNS (ns):	0.000	0.000	0.000	0.000
Violating Paths:	0	0	0	0
All Paths:	10032	7384	246	2992

Hold time

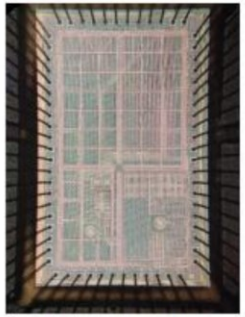
DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	9 (37)
max_fanout	43 (43)	-26	57 (57)
max_length	0 (0)	0	0 (0)

UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA

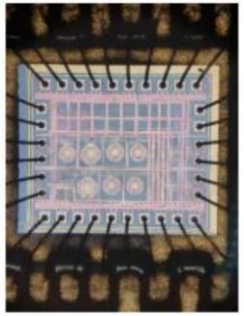
NICA_GBT, NICA_LD/RX ASICs and Customized Optical Module.

NICA_GBT, NICA_LD/Rx ASICs

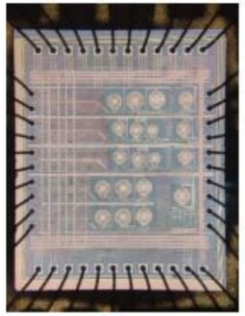
- Three chips of the first tape-out(December, 2020) in a standard 55 nm CMOS technology have been tested and successfully verified.



PLL+Deser Chip
Part of NICA_GBT core



LDLA Chip
For 1Tx+1Rx
optical module

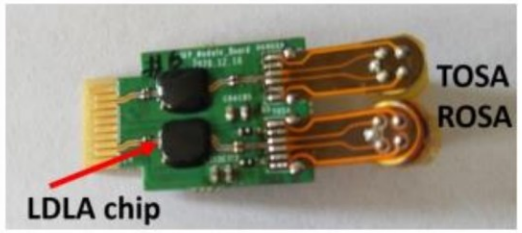


LDAr Chip
For multi-Tx/Rx
optical module

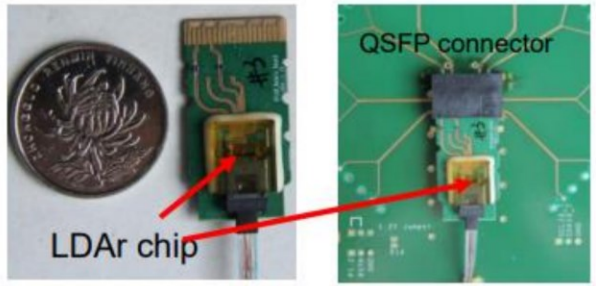
- The next tape-out is scheduled to be around the end of 2021. It will include the first complete NICA_GBT analog core (eTx/eRx, PLL, CDR, Des/Ser, PhaseAligner, etc..), and the second version of LDLA/LDAr chips.

Customized Optical Module

- Two types of customized optical modules are under development.



1Tx1Rx optical module



4Tx array optical module

- The further development of the optical modules (to replace CERN VTTx/VTRx modules) is ongoing together with the iteration of the LDLA/LDAr chips.
- After the second tape out of LDLA/LDAr in the end of this year, the customized optical modules are also planned to be updated and integrated with the new LDLA/LDAr.

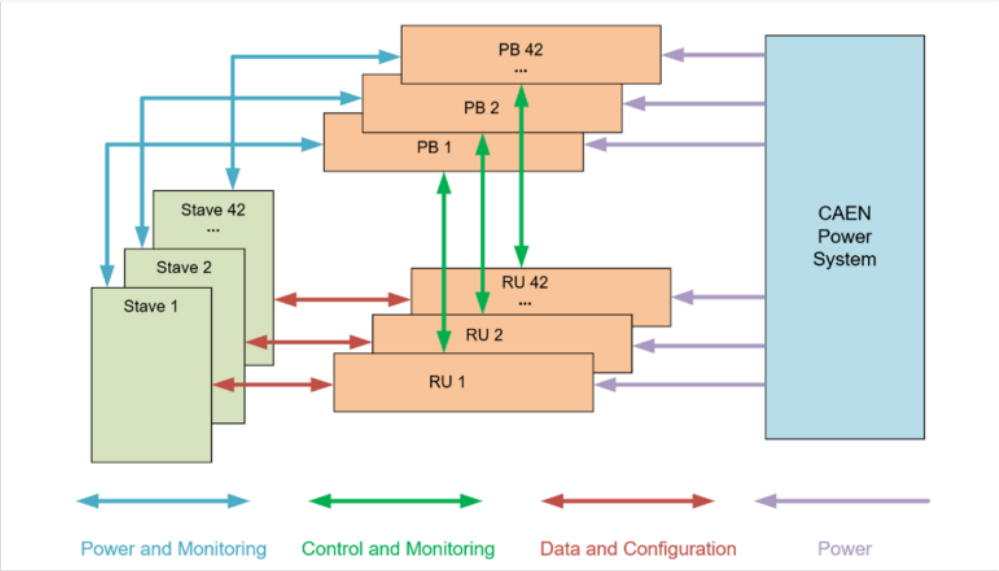
https://indico.cern.ch/event/820476/contributions/4372791/

A 14 Gbps optical transceiver LDLA14 fabricated in a 55 nm CMOS process has been designed and tested for NICA MPD project. Wide-open 14 Gbps eyes have been captured in both Tx and Rx directions, BER less than 10−12 has been achieved in the optical loop test.

UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA

Power system.

Structure of the power system of MPD-ITS



- The **PU** supplies 1.8 V positive power, as well as negative power used as bias for the staves.

- **In addition to supplying power to the staves**, the PU is also controlled by RU through the serial interface to implement the following functions:
  - Separate enabling of power channels and bias channels.
  - Adjusting the power supply voltage separately.
  - Adjusting the bias voltage in one PU.
  - Over current protection with adjustable threshold on each power channel.
  - Overheat protection on each PU.
  - Monitoring of voltage, current and temperature.

UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA

PU prototype.

Recent work

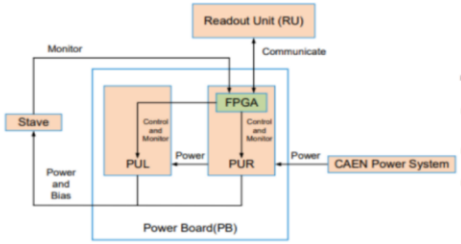
- NICA PU design
  - Have clarified interface with CAEN power system, Power Board Breakout Board and RU
  - Have clarified communication protocols with RU
  - Have began prototype PU schematic design

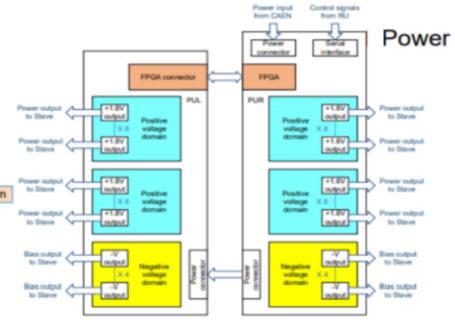
Work plan

- To finish prototype PU schematic design
- To finish prototype PU PCB layout design
- To test prototype PU

Design of PU

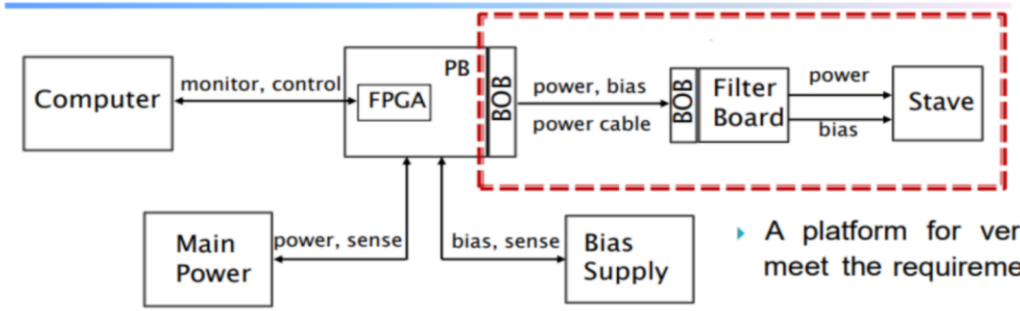
- The Power Board is composed by two Power Units
- Each Power Unit supplies 8 channels (16 converters, 8 for analogue and 8 for digital power rails)
- A flash FPGA on PUR controls both PUR and PUL and responsible for communications with RU
- The cooling plate is sandwiched between the two boards providing cooling and mechanical support, and the resulting entity fits 2 VME slots





Power Board in ALICE

Test of prototype PU



- A platform for verifying that the architecture and circuitry meet the requirements

UNIVERSITY OF SCIENCE AND TECHNOLOGY OF CHINA

MAPS chip test bench .

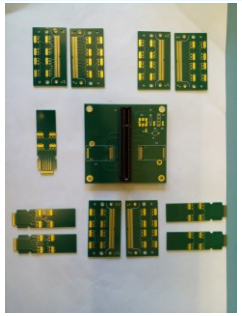
Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit

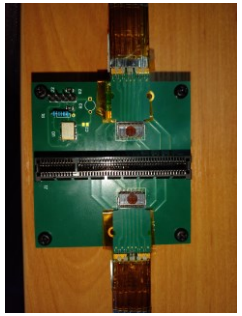
pALPIDE3 carrier v3

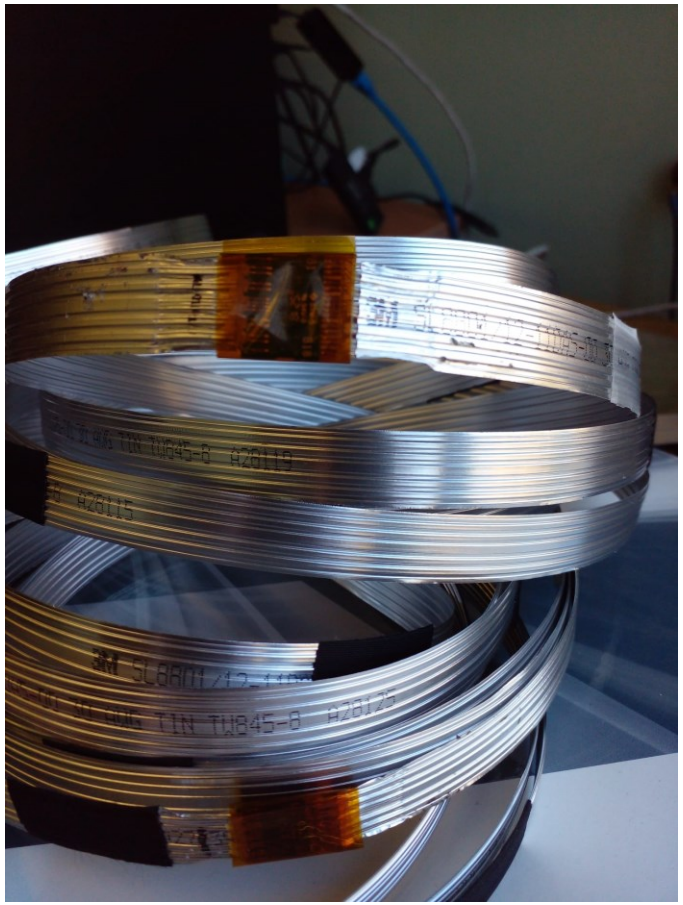
ECUE-12-999-T1-FF-01-1

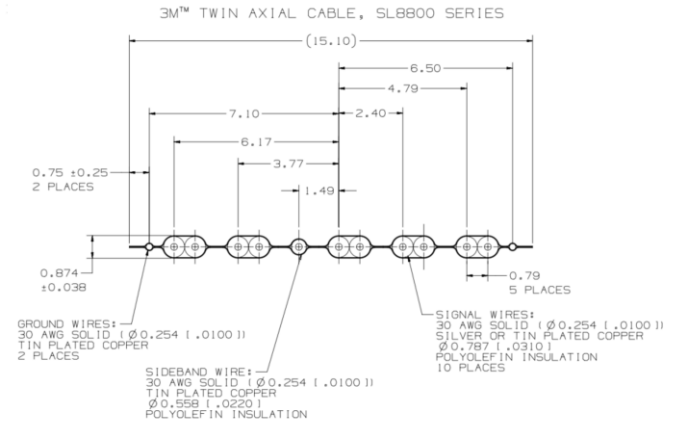
FMC to pALPIDE3 adapter

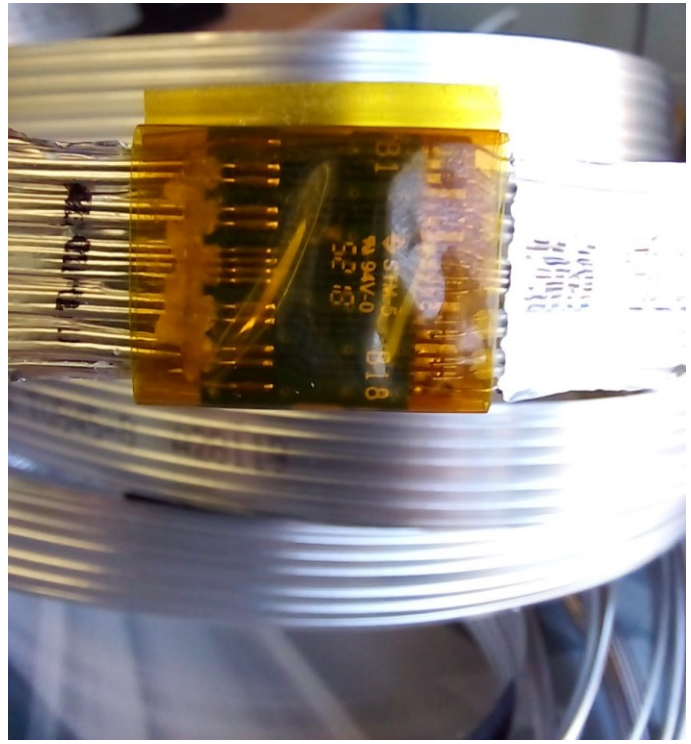
Prototype of Data cable using 3M twin axial cable , SL8800 series











Test result of cable (8 m) base on 3M twin axial cable , SL8800 series

MPD - ITS NICA

Hardware

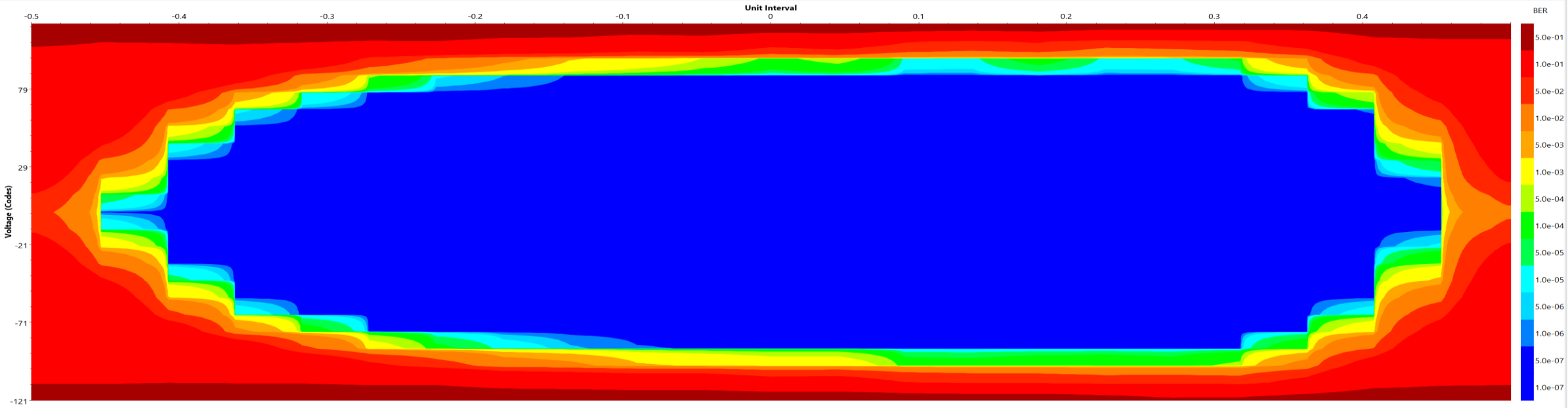
Name	Status
localhost (2)	Connected
xilinx_tcf/Digilent/210512180	Closed
xilinx_tcf/Xilinx/13724327082	Open
xcku040_0 (2)	Programmed
SysMon (System Monitor	
IBERT (u_ibert_gth_core)	
Quad_224 (5)	
COMMON_X0Y0	Not Locked
MGT_X0Y0	NO LINK
MGT_X0Y1	NO LINK
MGT_X0Y2	1.200 Gbps
MGT_X0Y3	1.200 Gbps
Quad_225 (5)	
COMMON_X0Y1	Not Locked
MGT_X0Y4	1.200 Gbps
MGT_X0Y5	1.200 Gbps
MGT_X0Y6	NO LINK
MGT_X0Y7	NO LINK

Tcl Console | Messages | Serial I/O Links | **Serial I/O Scans** | Intelligent Design Runs

Name	Link	Link Settings	Reset RX	Scan Type	Status	Progress	Open Area	Open UI %	Horz Incr	Horz Range	Vert Incr	Vert Range	Dwell	Dwell BER	Dwell Time	Start Time	End Time
Scans (4)																	
Scan 0	Auto detected link 0			2d_full_eye	Done	100%	32549	86.96	11	-0.500 UI to 0.500 UI	11	100%	BER	1e-8	0	2021-Oct-08 13:44:15	2021-Oct-08 13:45:53
Scan 1	Auto detected link 1			2d_full_eye	Done	100%	30129	86.96	11	-0.500 UI to 0.500 UI	11	100%	BER	1e-8	0	2021-Oct-08 13:46:15	2021-Oct-08 13:47:49
Scan 2	Auto detected link 2			2d_full_eye	Done	100%	29766	86.96	11	-0.500 UI to 0.500 UI	11	100%	BER	1e-8	0	2021-Oct-08 13:48:34	2021-Oct-08 13:50:06
Scan 3	Auto detected link 3			2d_full_eye	Done	100%	32428	86.96	11	-0.500 UI to 0.500 UI	11	100%	BER	1e-8	0	2021-Oct-08 13:50:18	2021-Oct-08 13:51:56

Tcl Console | Messages | **Serial I/O Links** | Serial I/O Scans | Intelligent Design Runs

Name	TX	RX	Status	Bits	Errors	BER	BERT Re...	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enab...	Inject Er...	TX Reset	RX Reset	RX PLL Sta...	TX PLL Sta...	Loopback Mode
Ungrouped Links (0)																			
Found Links (4)							Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)		Inject	Reset	Reset			None
Auto detected link 0	Quad_224/MGT_X0Y2/TX (xcku040_0)	Quad_224/MGT_X0Y2/RX (xcku040_0)	1.200 Gbps	3.935E12	0E0	2.542E-13	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)		Inject	Reset	Reset	Locked	Locked	None
Auto detected link 1	Quad_224/MGT_X0Y3/TX (xcku040_0)	Quad_224/MGT_X0Y3/RX (xcku040_0)	1.200 Gbps	3.935E12	0E0	2.542E-13	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)		Inject	Reset	Reset	Locked	Locked	None
Auto detected link 2	Quad_225/MGT_X0Y4/TX (xcku040_0)	Quad_225/MGT_X0Y4/RX (xcku040_0)	1.200 Gbps	3.935E12	0E0	2.542E-13	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)		Inject	Reset	Reset	Locked	Locked	None
Auto detected link 3	Quad_225/MGT_X0Y5/TX (xcku040_0)	Quad_225/MGT_X0Y5/RX (xcku040_0)	1.200 Gbps	3.935E12	0E0	2.542E-13	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)		Inject	Reset	Reset	Locked	Locked	None



Summary

Name:	SCAN_0
Description:	Scan 0
Started:	2021-Oct-08 13:44:15
Ended:	2021-Oct-08 13:45:53

Metrics

Open area:	32549
Open UI %:	86.96

Settings

Link settings:	N/A
Horizontal increment:	11
Horizontal range:	-0.500 UI to 0.500 UI
Vertical increment:	11
Vertical range:	100%

Conclusions

- Two unit of the first prototype of a RU based on Kintex Utrascale FPGA are under test.
- The initial firmware architecture is already designed and it need to be tested, as part of the design the components needed for Radiation effect mitigation are included.
- The specifications of PU are already defined, we have plan to finish the design and constructions of the first prototype.
- The works related to the design and development of the NICA_GBT, NICA_LD / RX ASICs are well advanced and is expected to be completed in the planned time.
- A 14 Gbps optical transceiver LDLA14 fabricated in a 55 nm CMOS process has been designed and tested for NICA MPD project. Wide-open 14 Gbps eyes have been captured in both Tx and Rx directions, BER less than 10^{-12} has been achieved in the optical loop test.
- We were able to build in the lab a data prototype cable with vary good performance using a commercially available cable, then we need to think how to scale the construction to production version.

BACKUP

Backup (12 m 3M cable)

MPD - ITS

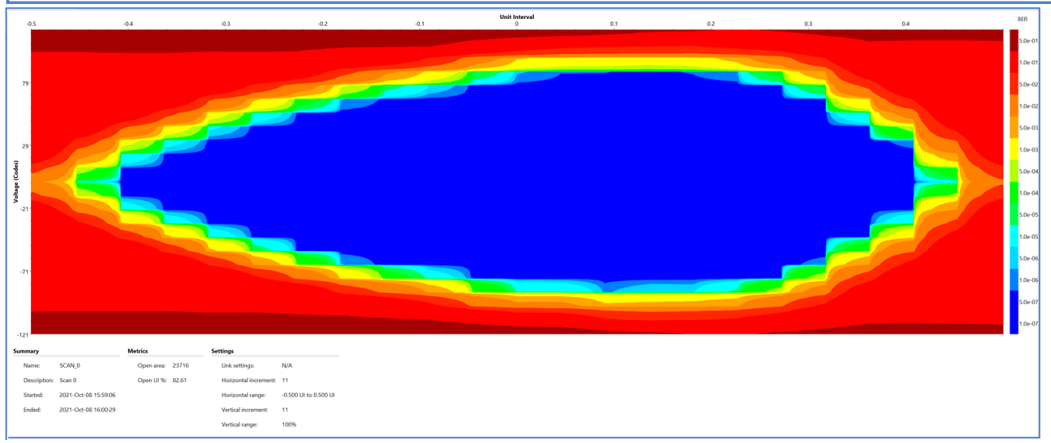
NICA

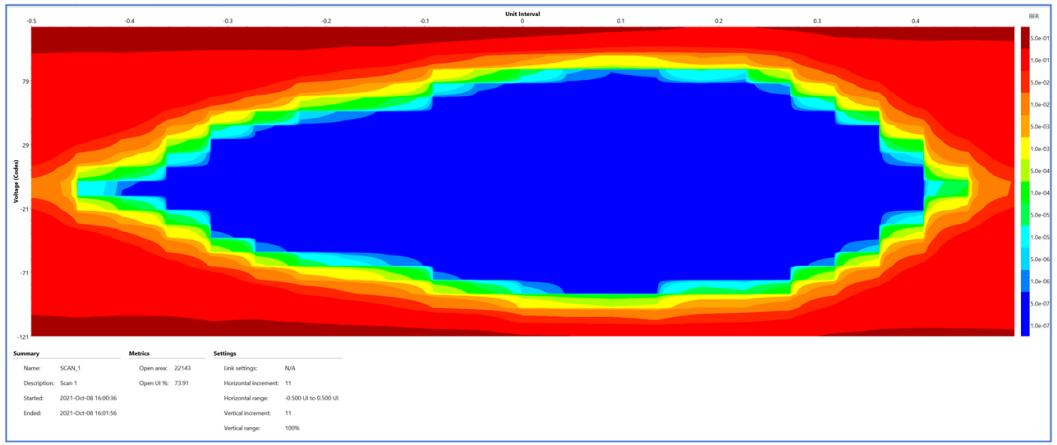
Tcl Console | Messages | Serial I/O Links | **Serial I/O Scans** | Intelligent Design Runs

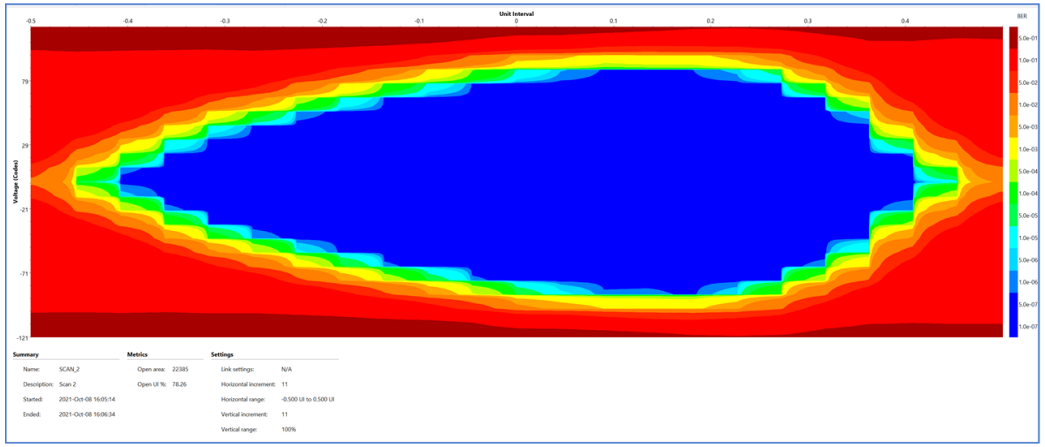
Name	Link	Link Settings	Reset RX	Scan Type	Status	Progress	Open Area	Open UI %	Horz Incr	Horz Range	Vert Incr	Vert Range	Dwell	Dwell BER	Dwell Time	Start Time	End Time
Scans (4)																	
Scan 0	Auto detected link 0		☐	2d_full_eye	Done	100%	23716	82.61	11	-0.500 UI to 0.500 UI	11	100%	BER	1e-8	0	2021-Oct-08 15:59:06	2021-Oct-08 16:00:29
Scan 1	Auto detected link 1		☐	2d_full_eye	Done	100%	22143	73.91	11	-0.500 UI to 0.500 UI	11	100%	BER	1e-8	0	2021-Oct-08 16:00:36	2021-Oct-08 16:01:56
Scan 2	Auto detected link 2		☐	2d_full_eye	Done	100%	22385	78.26	11	-0.500 UI to 0.500 UI	11	100%	BER	1e-8	0	2021-Oct-08 16:05:14	2021-Oct-08 16:06:34
Scan 3	Auto detected link 3		☐	2d_full_eye	Done	100%	24079	82.61	11	-0.500 UI to 0.500 UI	11	100%	BER	1e-8	0	2021-Oct-08 16:03:39	2021-Oct-08 16:05:06

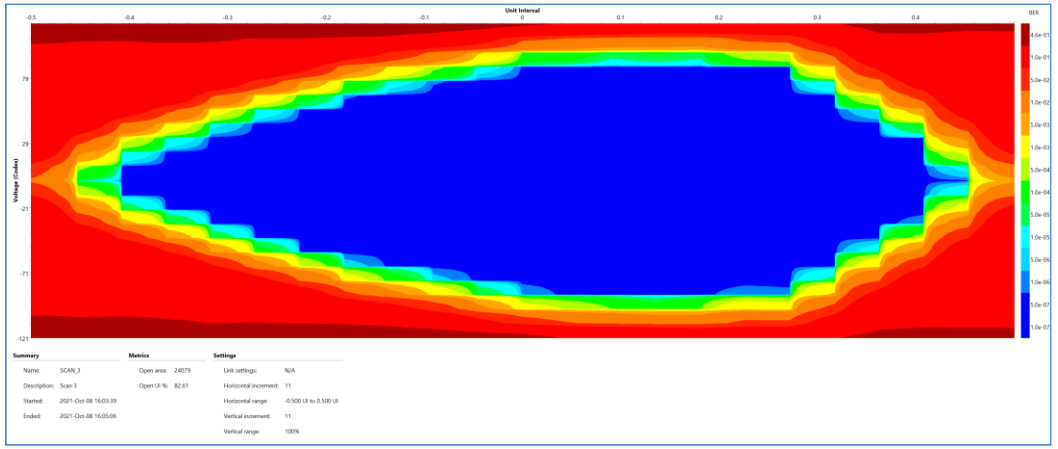
Tcl Console | Messages | **Serial I/O Links** | Serial I/O Scans | Intelligent Design Runs

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mode
Ungrouped Links (0)																			
Found Links (4)							Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)	☑	Inject	Reset	Reset			None
Auto detected link 0	Quad_224/MGT_X0Y2/TX (xcku040_0)	Quad_224/MGT_X0Y2/RX (xcku040_0)	1.200 Gbps	1.544E12	0E0	6.477E-13	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)	☑	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 1	Quad_224/MGT_X0Y3/TX (xcku040_0)	Quad_224/MGT_X0Y3/RX (xcku040_0)	1.200 Gbps	1.544E12	0E0	6.477E-13	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)	☑	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 2	Quad_225/MGT_X0Y4/TX (xcku040_0)	Quad_225/MGT_X0Y4/RX (xcku040_0)	1.200 Gbps	1.544E12	0E0	6.477E-13	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)	☑	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 3	Quad_225/MGT_X0Y5/TX (xcku040_0)	Quad_225/MGT_X0Y5/RX (xcku040_0)	1.200 Gbps	1.544E12	0E0	6.477E-13	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)	☑	Inject	Reset	Reset	Locked	Locked	None









Backup (10 m Samtec cable)

Hardware

Name	Status
localhost (2)	Connected
xilinx_tcf/Xilinx/13724327082c0	Open
xcku040_0 (2)	Programmed
SysMon (System Monitor)	
IBERT (u_ibert_gth_core)	
Quad_224 (5)	
COMMON_X0Y0	Not Locked
MGT_X0Y0	NO LINK
MGT_X0Y1	NO LINK
MGT_X0Y2	1.200 Gbps
MGT_X0Y3	1.200 Gbps
Quad_225 (5)	
COMMON_X0Y1	Not Locked
MGT_X0Y4	1.200 Gbps
MGT_X0Y5	1.200 Gbps
MGT_X0Y6	NO LINK
MGT_X0Y7	NO LINK

Serial I/O Scans

Name	Link	Link Settings	Reset RX	Scan Type	Status	Progress	Open Area	Open UI %	Horz Incr	Horz Range	Vert Incr	Vert Range	Dwell	Dwell BER	Dwell Time	Start Time	End Time
Scans (4)																	
Scan 1	Auto detected link 0			2d_full_eye	Done	100%	17061	73.91	11	-0.500 UI to 0.500 UI	11	100%	BER	1e-7	0	2021-Oct-01 11:28:26	2021-Oct-01 11:28:33
Scan 2	Auto detected link 1			2d_full_eye	Done	100%	14520	60.87	11	-0.500 UI to 0.500 UI	11	100%	BER	1e-7	0	2021-Oct-01 11:31:40	2021-Oct-01 11:31:46
Scan 3	Auto detected link 2			2d_full_eye	Done	100%	16093	73.91	11	-0.500 UI to 0.500 UI	11	100%	BER	1e-7	0	2021-Oct-01 11:30:53	2021-Oct-01 11:31:00
Scan 4	Auto detected link 3			2d_full_eye	Done	100%	16819	73.91	11	-0.500 UI to 0.500 UI	11	100%	BER	1e-7	0	2021-Oct-01 11:30:41	2021-Oct-01 11:30:48

Serial I/O Links

Name	TX	RX	Status	Bits	Errors	BER	BERT Re...	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Er...	TX Reset	RX Reset	RX PLL Sta...	TX PLL Sta...	Loopback Mode
Ungrouped Links (0)																			
Found Links (4)							Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	840 mV (1010)		Inject	Reset	Reset			None
Auto detected link 0	Quad_224/MGT_X0Y2/TX (xcku040_0)	Quad_224/MGT_X0Y2/RX (xcku040_0)	1.200 Gbps	1.398E11	0E0	7.152E-12	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	840 mV (1010)		Inject	Reset	Reset	Locked	Locked	None
Auto detected link 1	Quad_224/MGT_X0Y3/TX (xcku040_0)	Quad_224/MGT_X0Y3/RX (xcku040_0)	1.200 Gbps	1.398E11	0E0	7.151E-12	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	840 mV (1010)		Inject	Reset	Reset	Locked	Locked	None
Auto detected link 2	Quad_225/MGT_X0Y4/TX (xcku040_0)	Quad_225/MGT_X0Y4/RX (xcku040_0)	1.200 Gbps	1.399E11	0E0	7.15E-12	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	840 mV (1010)		Inject	Reset	Reset	Locked	Locked	None
Auto detected link 3	Quad_225/MGT_X0Y5/TX (xcku040_0)	Quad_225/MGT_X0Y5/RX (xcku040_0)	1.200 Gbps	1.399E11	0E0	7.15E-12	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	840 mV (1010)		Inject	Reset	Reset	Locked	Locked	None