Status and perspectives of the MPD ITS

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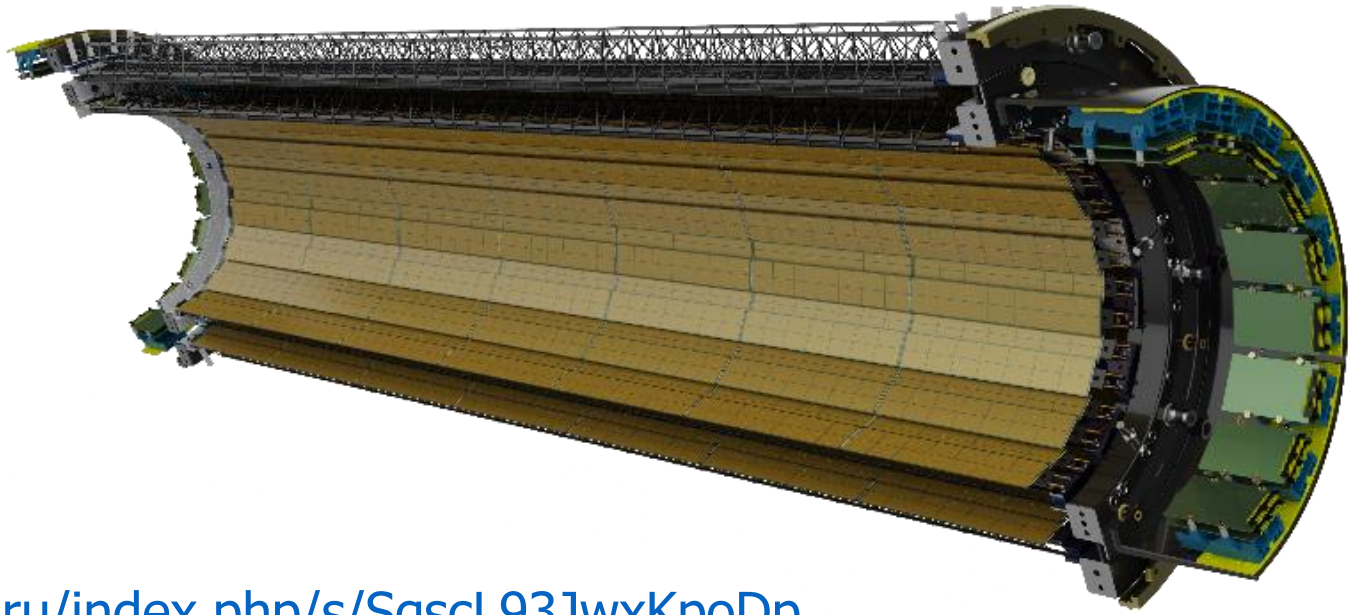


link for the MPD-ITS
TDR: https://disk.jinr.ru/index.php/s/SgscL93JwxKpoDp

https://indico.cern.ch/event/1012633/contributions/4478061/attachments/2313953/3938670/Nucleus-2021_Ceballos.pdf

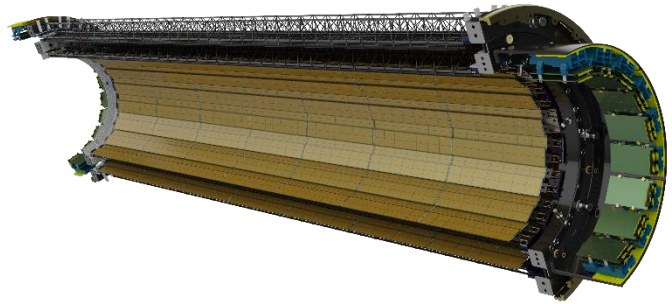
Moments of the MPD ITS story

- Protocol on transfer of MAPS ITS technology and Know-How with CERN – 2018
- Design and simulations of the ITS – 2018-2020
- Forming a collaboration with Chinese Labs in Wuhan, Lanzhou and Hefei – 2019
- Preparations for Assembly of HICs and Staves – 2018 -….
- Ban on export of 19’000 ALPIDE MAPS by Israel – 2020
- Re-design of rad-hard ALPIDE to nonmilitary graded ALTAI MAPS – 2021
- Pre-production of ALTAI chips by Towers – 2021-2022
- Suspending cooperation with EU… looking for ways around the sanctions

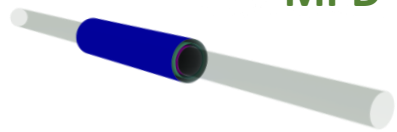
Introduction

The MAPS-based IT detector will enable charm-hadron measurements and detection of collision vertexes for the MPD experiment:

- Charm production in heavy ion collisions at the NICA energies
- Clean measurement of (multi-)strange hadron productions



MPD-ITS-Outer Barrel



MPD-ITS Inner Barrel

Stage 1: ALPIDE-based OB layers (Design of ALICE ITS2)

Stage 2: Stitched large-area MAPS IB layers

	Inner Barrel			Outer Barrel	
	Layer 0	Layer 1	Layer 2	Layer 3	Layer 4
R_{min} (mm)	18	24	30	145.8	194.4
R_{max} (mm)	18	24	30	147.9	197.6
Length (mm)	270	270	270	1468	1468
$P_{seudo\text{-}rapidity}$	±2.5	±2.3	±2.0	±2.0	±2.0
Number of chips per layer	4	4	4	3528	4704
Pixel chip dimensions (mm^2)	140 × 56.5	140 × 75.5	140 × 94	15×30	
Active area (cm^2) (2mm dead area in r-phi)	305	408	508	13 759	18 346

MAPS-based pixel

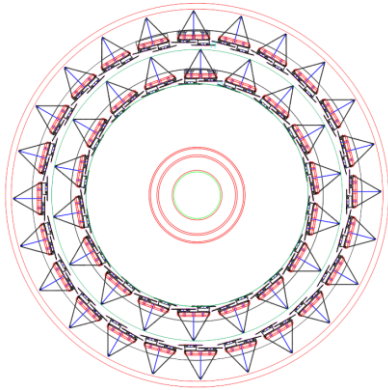
5 cylinder layers;

2 barrels (IB, OB);

4.5 x 109 pixels;

3.3 m^2 active area;

$|\eta| \leq 2.0$;



The ITS TDR

TEXT:
https://disk.jinr.ru/index.php/s/SgscL93JwxKpoDp

SLIDES:
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1. Introduction
2. The Pixel chips
3. The Detector Layout
4. Support Structure and System Integration
5. DAQ System
6. Detector Control System
7. Detector Physics Performance
8. Project Organization and Time Lines

ESSENTIALS:

Completion in two steps with first stage end of 2023; second in 2025;

Design and production of mechanics by mid 2023 ;

Capability HICs and, optionally staves, assembly at JINR under CMIS control by 2023;

Readout system and DCS development together with Chinese partners by end 2023.

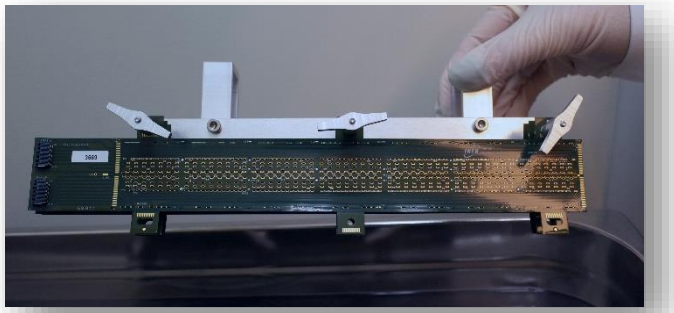
The ITS Project advances

- **Physics feasibility:** The ITS design and simulations ***(completed)***
- **Mechanics:** The ITS CF lamination workshop and reliable industrial partners ***(going on)***
- **Production feasibility:** the ITS HIC assembly under CMIS control (***feasibility demonstrated***)
- **Readout system production feasibility:** Readout system and DCS development together with Chinese partners ***(going on with first chips of the GBT set produced in China)***

Main stages of MPD ITS production follow ALICE ITS2 technology

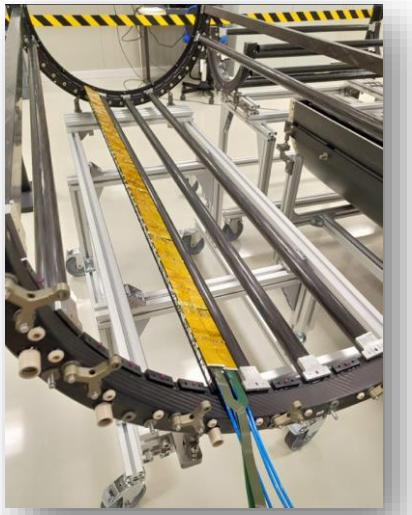
ALTAI MAPS chips

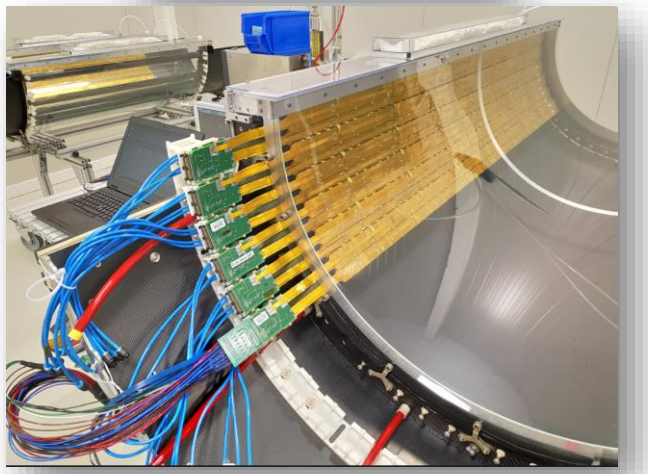
Flexible Printed Circuit (FPC)



Hybrid Integrated Circuits (HIC)

STAVE





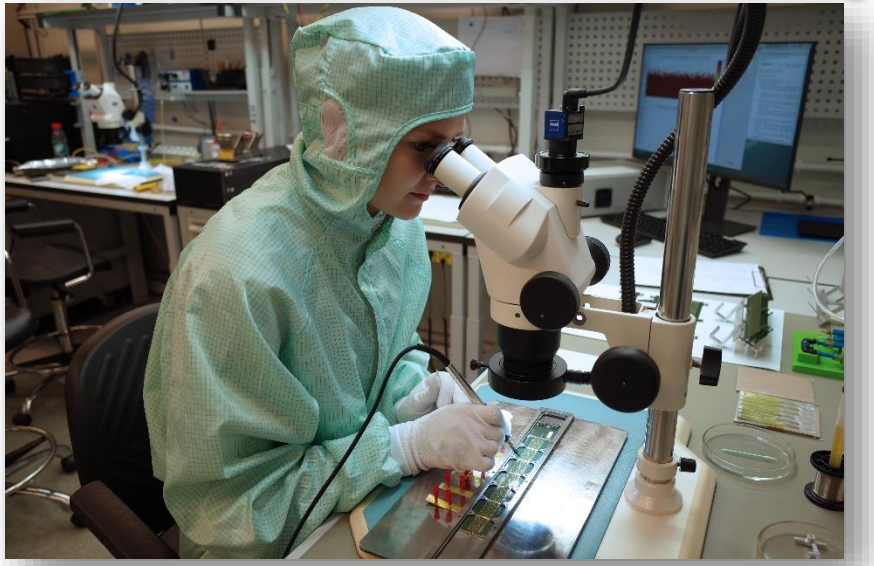
ITS Layer 4 = 18 STAVEs

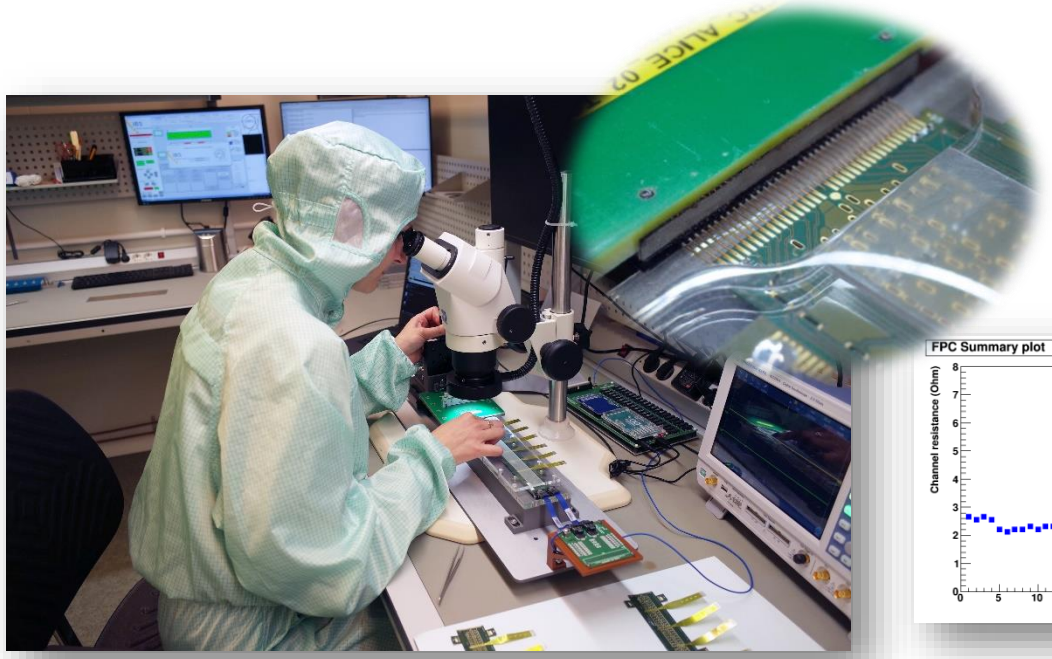
ITS Layer 5 = 24 STAVEs

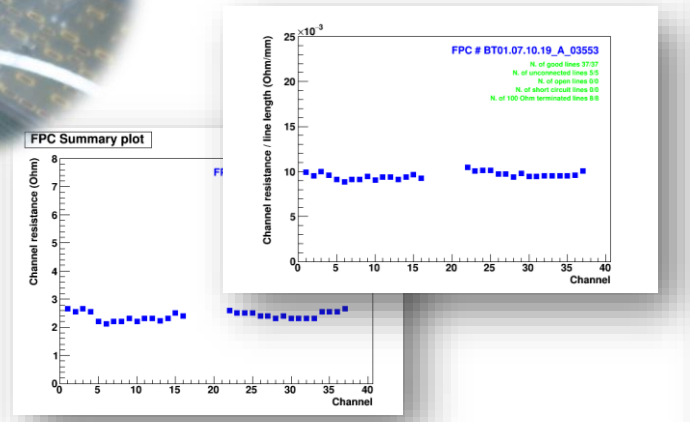
Assembly stages for ITS detectors parts 1/3 *A.Sheremetev et al.*

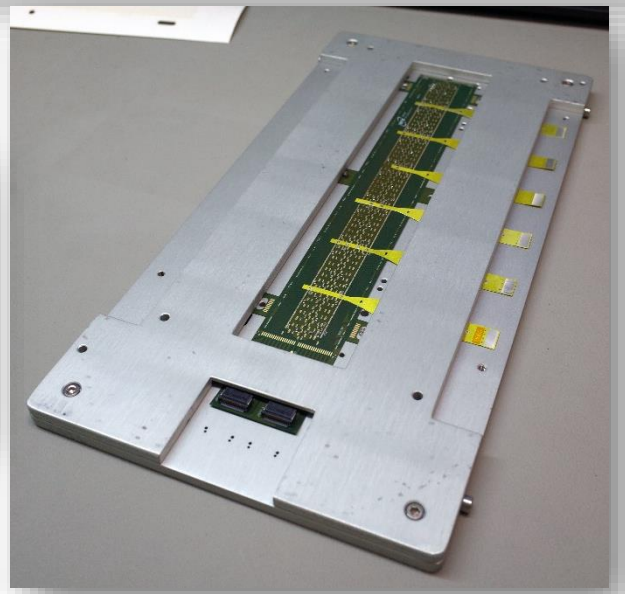
Workflow of preparing the FPC:

- Soldering Cross cable to FPC
- Cleaning the FPC in an ultrasonic bath
- Impedance test of FPC
- Storage to carrier plates





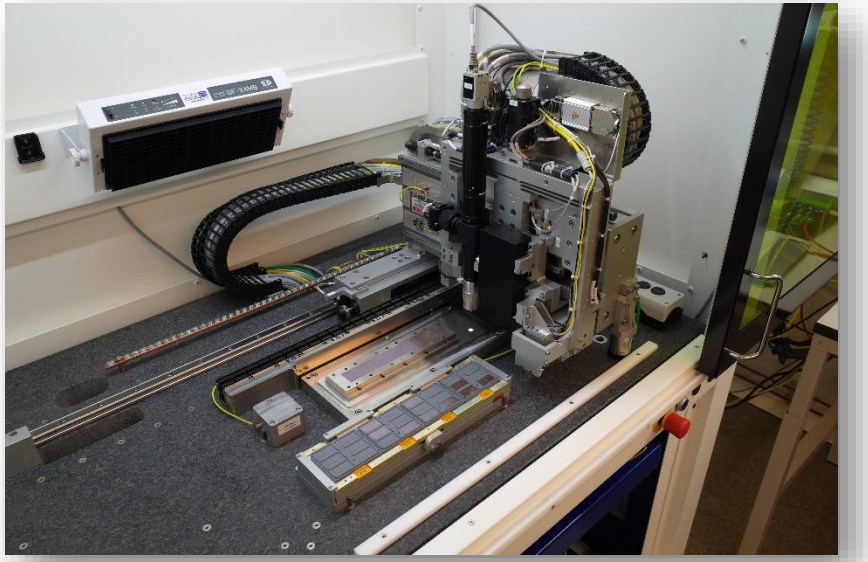


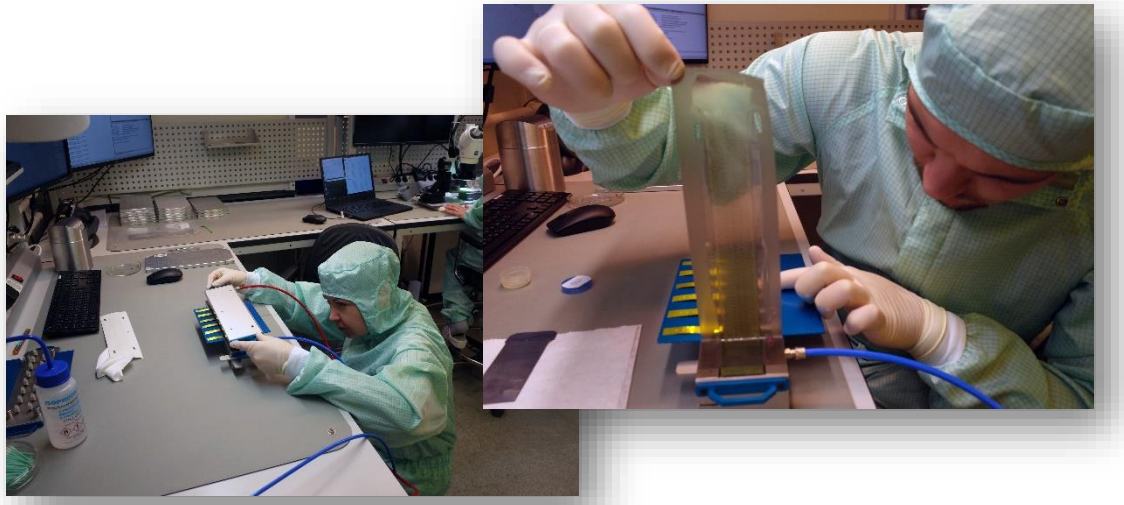


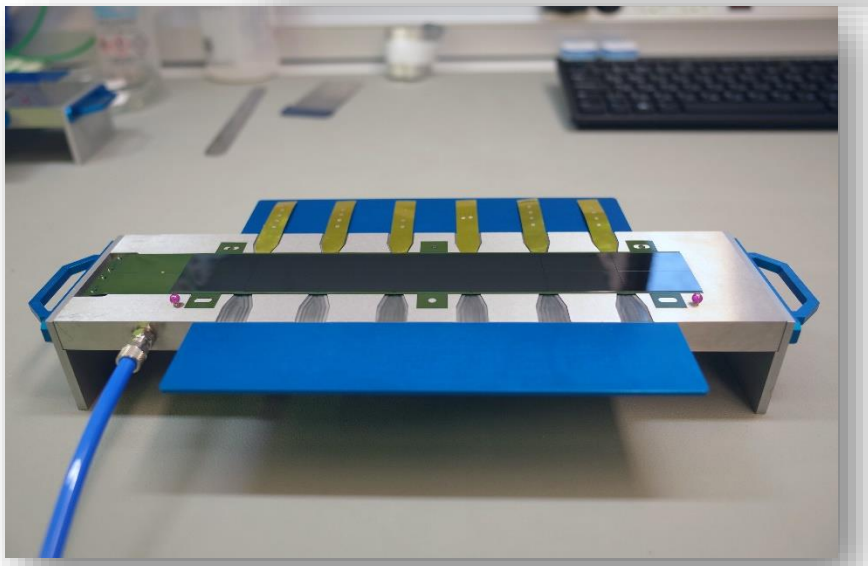
Assembly stages for ITS detectors parts 2/3 *A.Sheremetev et al.*

Workflow of assembly ALTAI MAPS chip to FPC:

- Alignment ALTAI chips in ALICIA-8
- Glue Chips to FPC
- Wire bonding with Delvotec G5
- Peel test of wire bondings of HIC
- Distractive control pull test of some HIC







Assembly stages for ITS detectors parts 3/3 *A.Sheremetev et al.*

- **Electrical test of HIC:**

  - IV curve measurement
  - Test with IR camera
  - Electrical test of single HIC
  - Endurance test of 10 assembled HICs

The ITS Project obstacles

- **Mechanics:** usage of “dual usage” graded materials **(had been overcome)**; mockup of IC installation to be completed in mid 2023
- **Electronics:** usage of “dual usage” graded components, especially, of ALPIDE chip export ban let to years delay , ALTAI chip free of this limitations but currently delivery suspended by CERN (options are being discussed with partners and true time lines to be announced soon)

Thank you for the attention!