TPC concentrator chip development: results & plans

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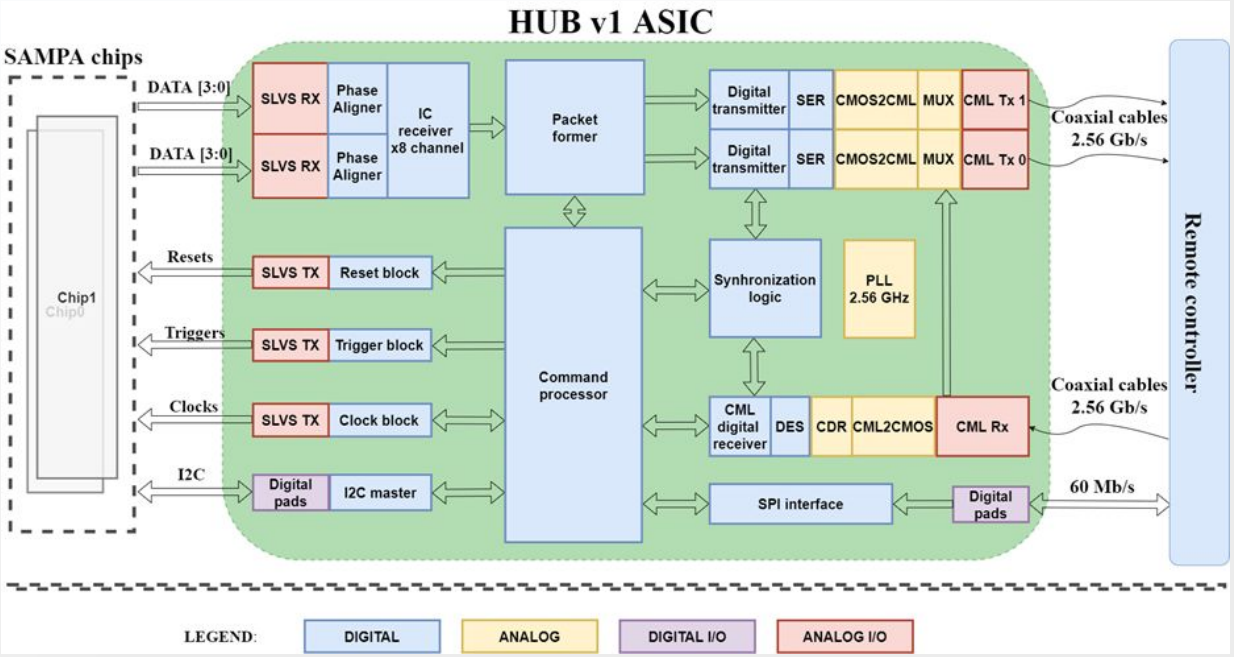
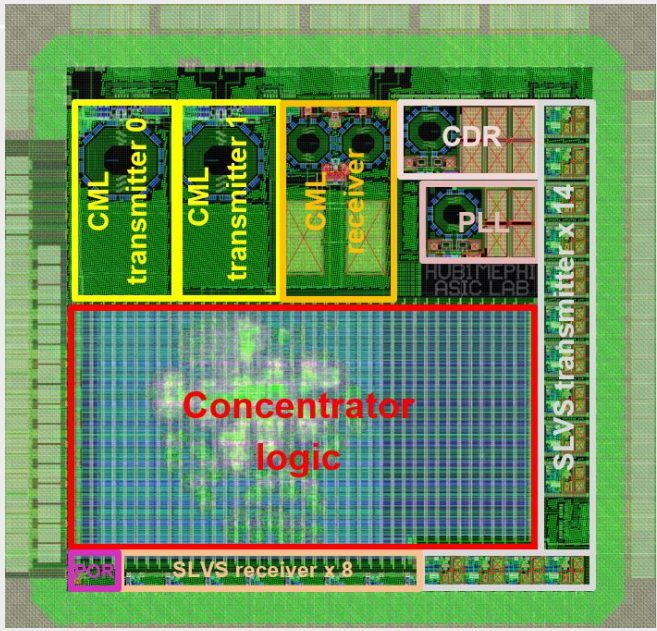
Outline

- Prototype ASIC Hub v1
- Test program, 2 PCBs
- Lab test board
- First results
- Demonstrator test bench
- Hub v2 ASIC plans

ASIC Hub v1: structure and specs

main functions: data concentration from two SAMPA chips and their transfer to counting room via fast 2.56 Gb/s bi-directional interface



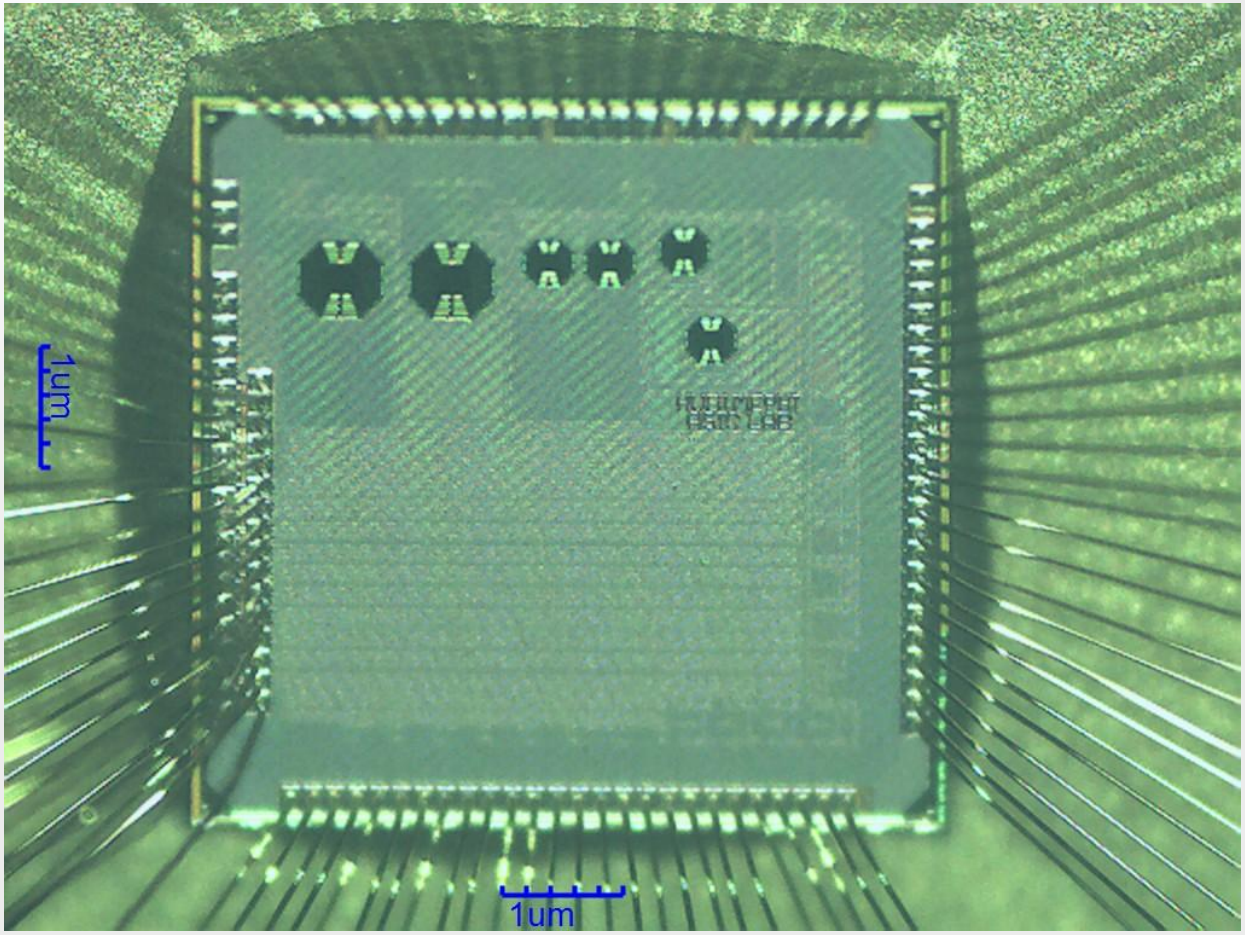


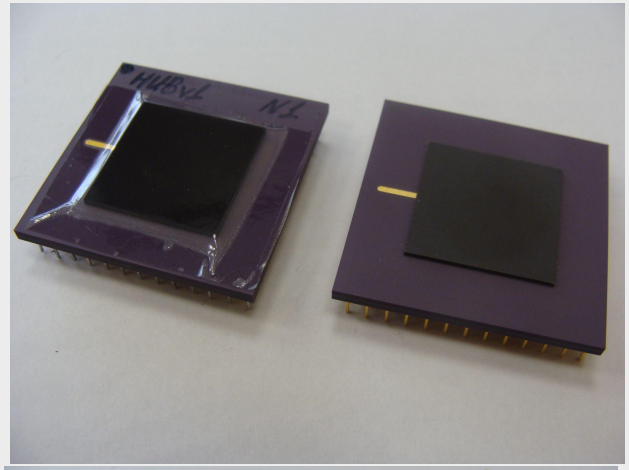
Specifications	Value
Technology	TSMC CMOS 65 nm
I/O voltage	2.5 V
Core voltage	1.2 V
Power consumption	< 500 mW

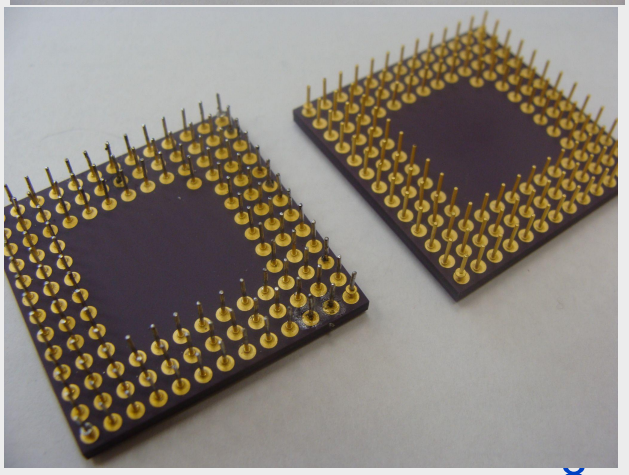
1) Process – TSMC65 LP MS RF 1P9M_6X1Z1U_RDL;
2) Chip area – 1980 x 1980 um;
3) Bond pads – 111 (37 type CUP staggered & 74 type IN-LINE)
   Pad size – 57 x 69 um
   Pad Pitch – 60 um
4) Technological run of Nov. 2020
5) Readiness – July 2021
2 types of packaging: CPGA 120 & caseless

Hub v1 photos (chip & case)

Fabricated are 10 pcs in CPGA-120 package and 80 pcs - caseless







Test program (2 boards)

1) Laboratory phase (functionality & radiation tolerance)

2) Prototype demonstrator for TPC

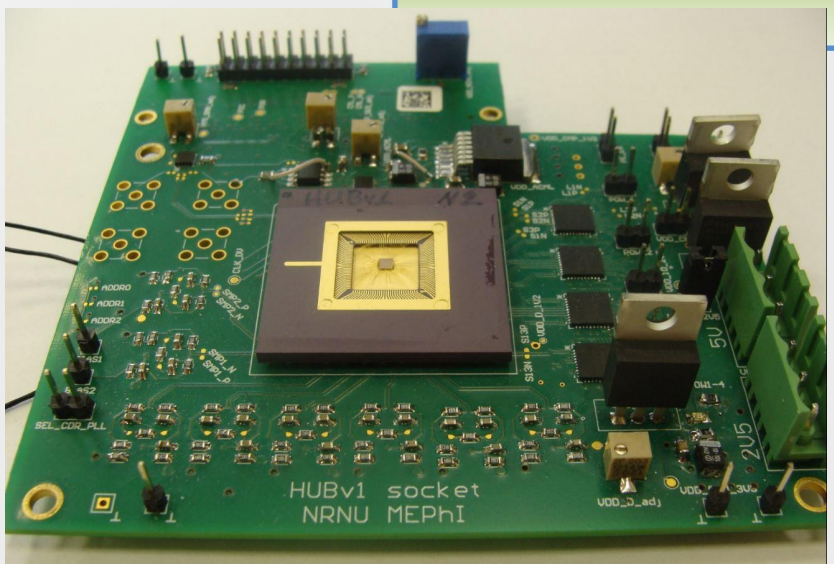
Supporting components:

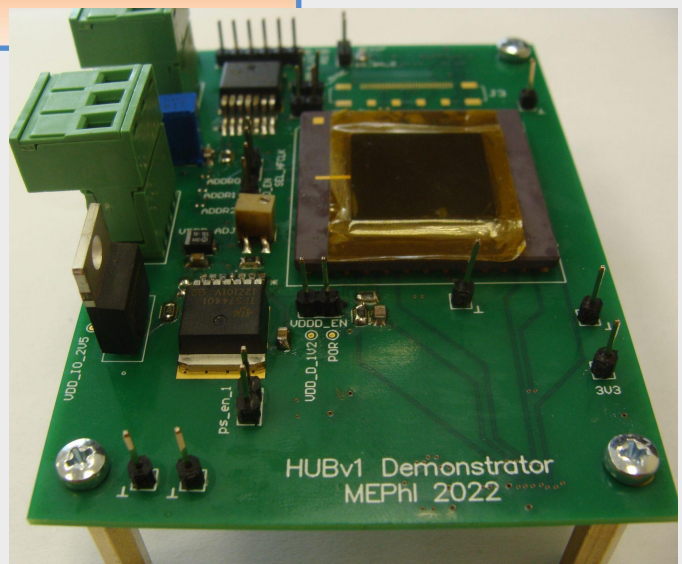
- SLVS – LVDS translators and passive components
- Comparators with adjustable hysteresis to evaluate CML eye-opening at different loads
- FMC HPC (on back side)

Testing

Laboratory testing
Functionality test – NRNU MEPhI
Radiation test – PNPI (Gatchina)

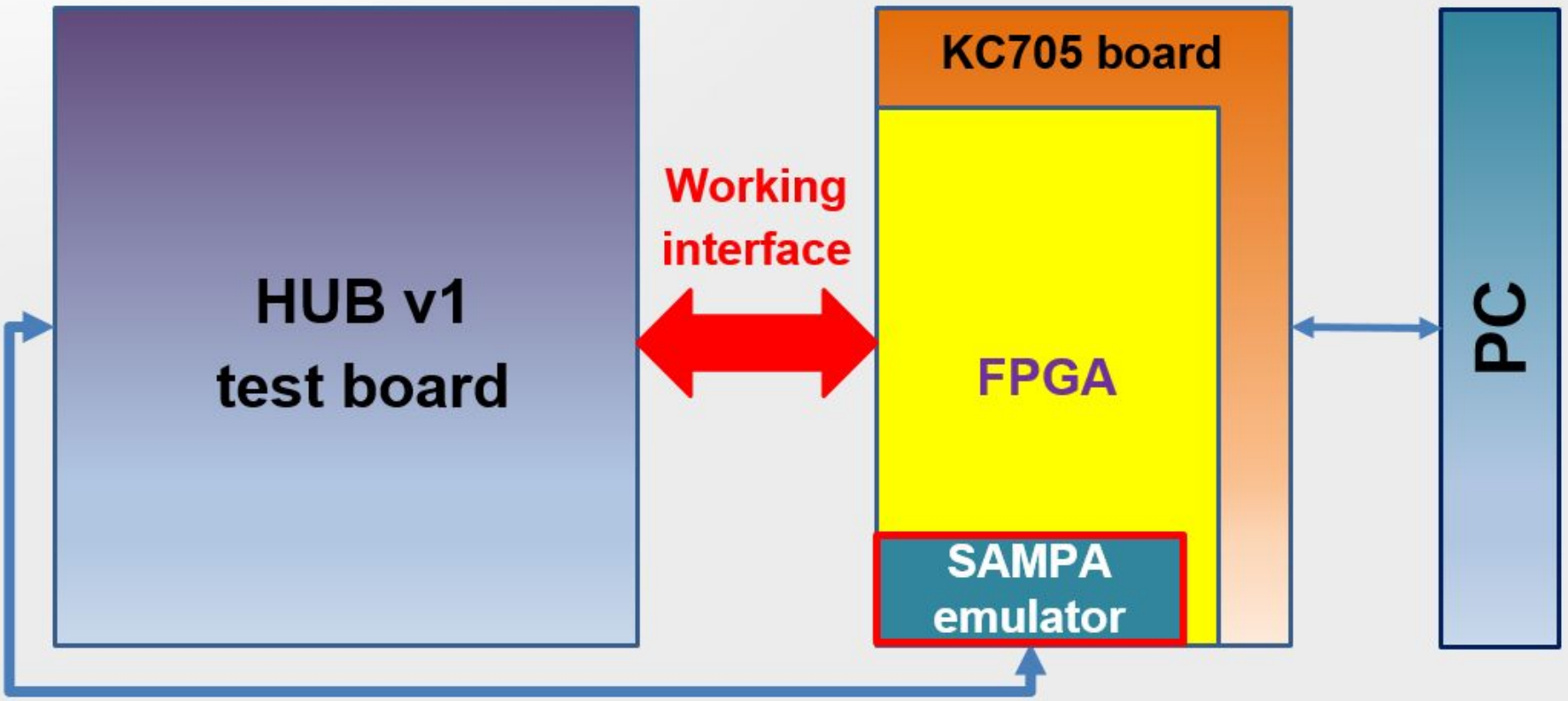
Demonstrator
NRNU MEPhI + JINR (Dubna)



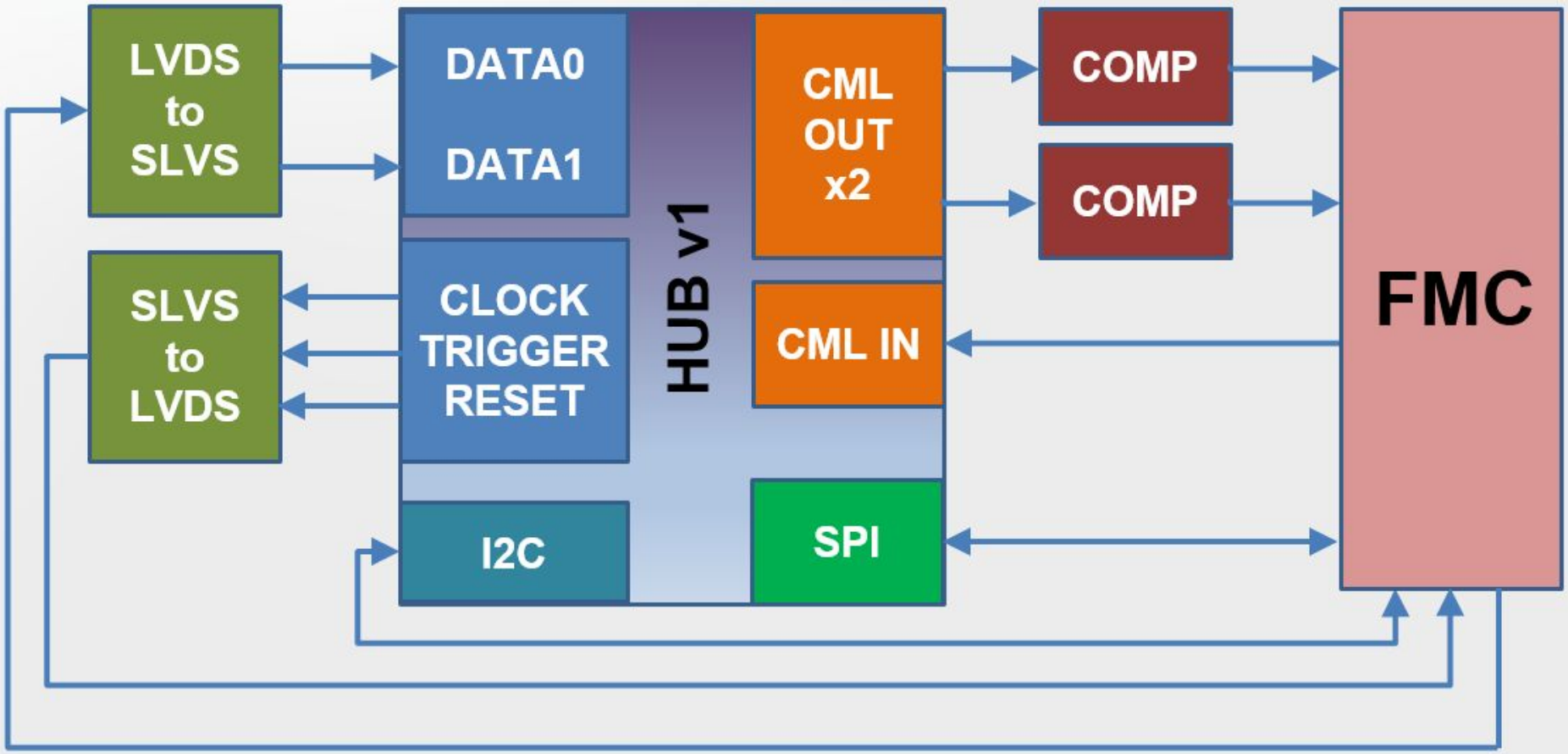


Lab test bench

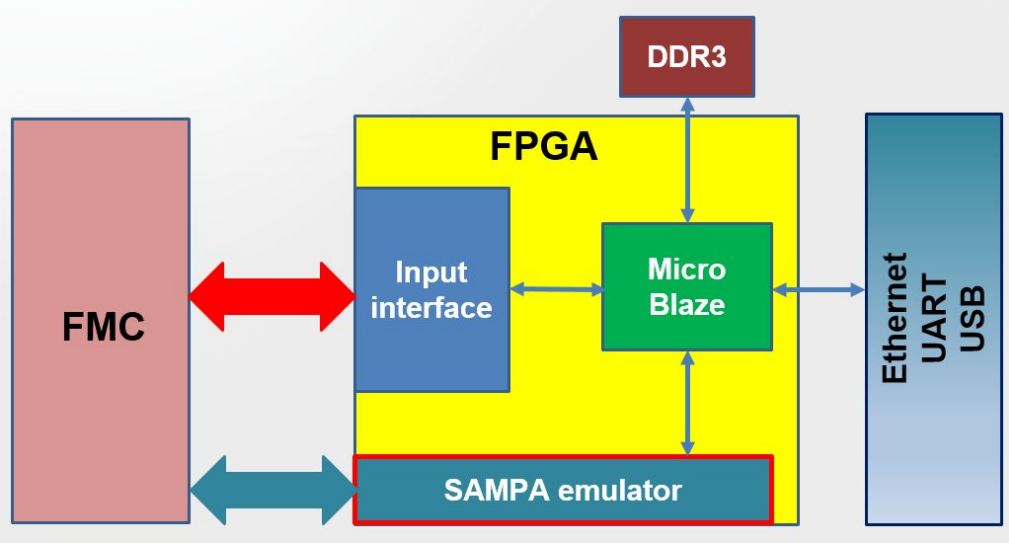
Aim - checking functionality of the chip at lab conditions



Test board block diagram



KC705 FPGA control board



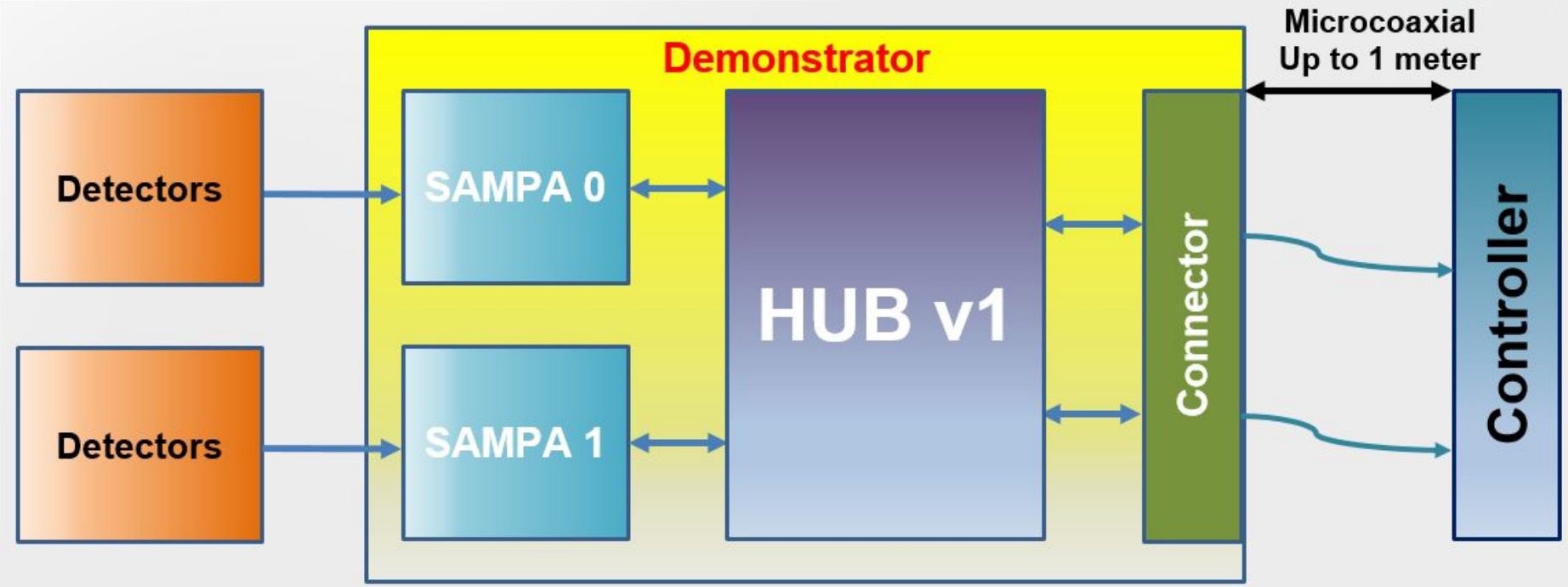
Key features:

- Kintex-7 XC7K325T FPGA with MicroBlaze capability
- 1 GB DDR3 memory
- USB port with USB-to-UART bridge
- 1000 Mb/s Ethernet interface
- FMC HPC:
  - 4 high-speed GTX transceivers
  - about 70 differential LVDS lines

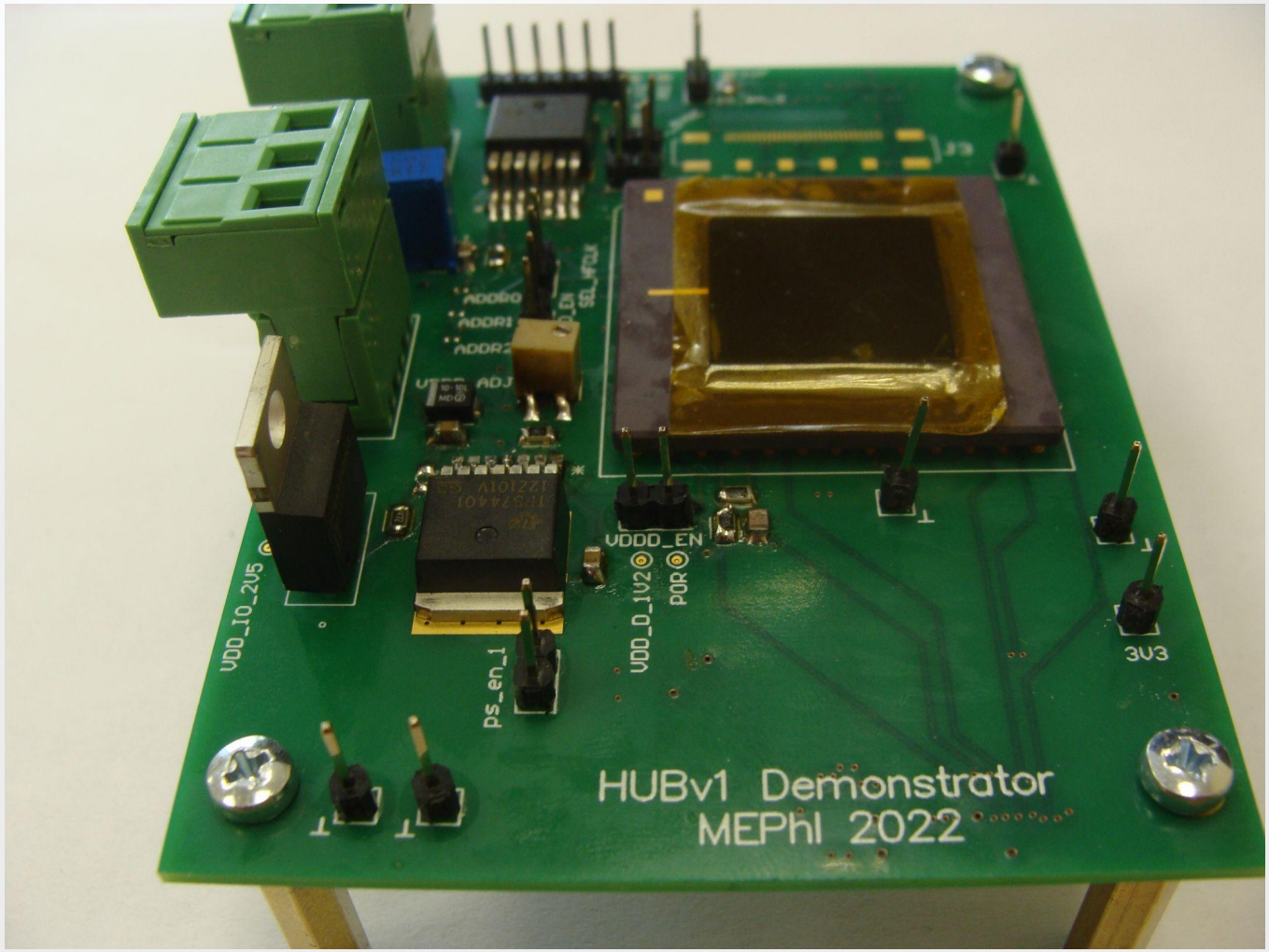
First lab test bench results for Hub v1 chip

1) Functionality has been confirmed for a few building blocks only
2) Problems have been verified. Standard digital pads do not (!) connected to the internal chip routing
3) All tests (incl. ones under irradiation) have been performed with working analog blocks only

The demonstrator concept



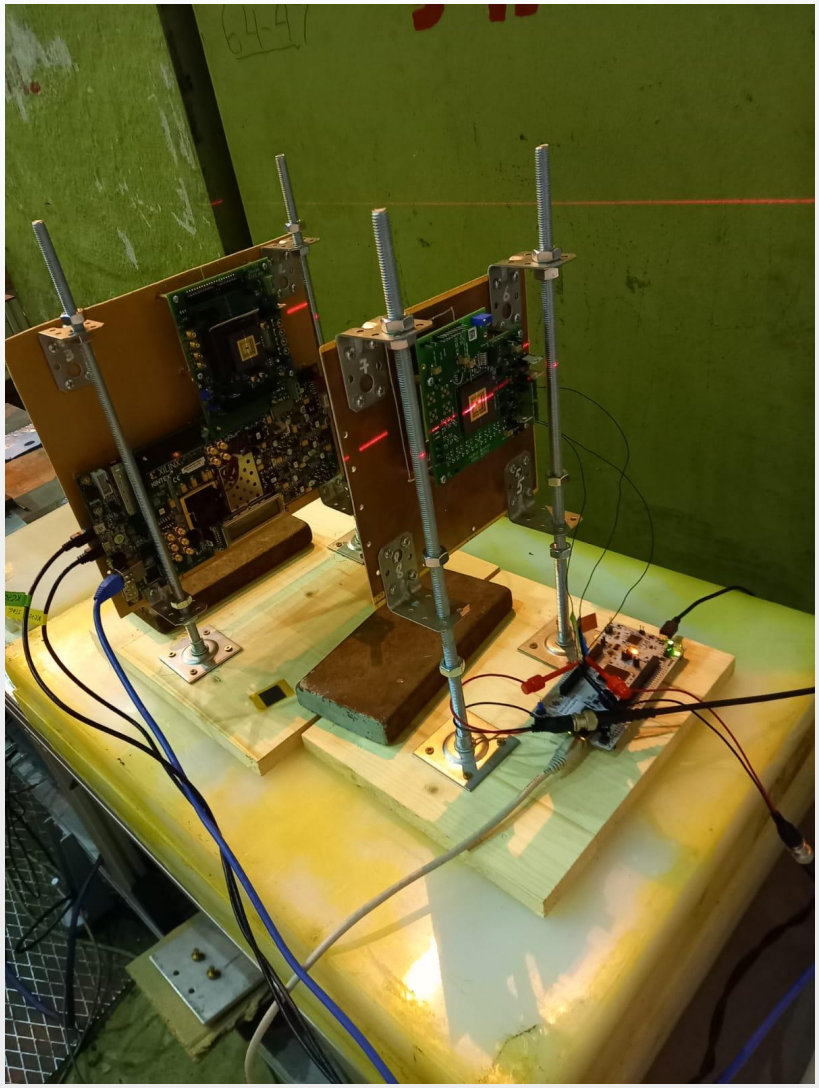
The demonstrator board photo

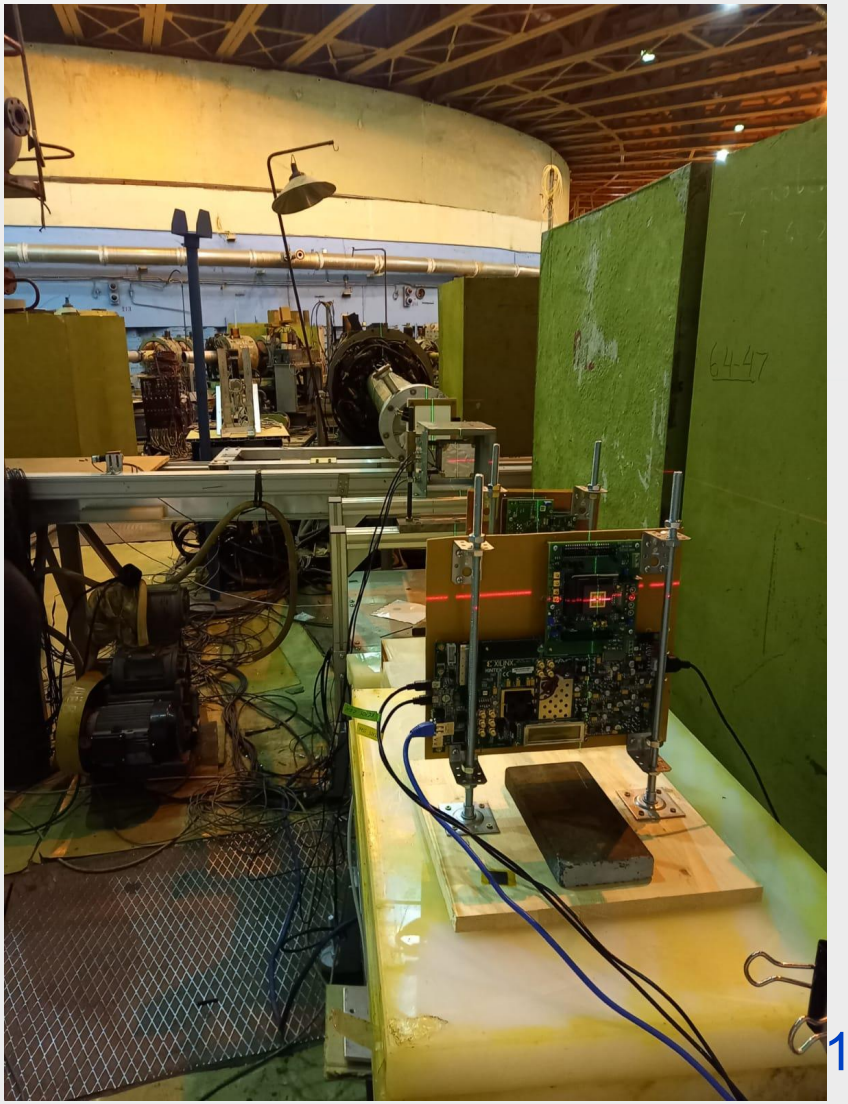


The lab testbench in calibrated beam

Purpose - checking functionality of the chip blocks against heavy particles.

Tests were done at PNPI, Gatchina in Feb. 2022





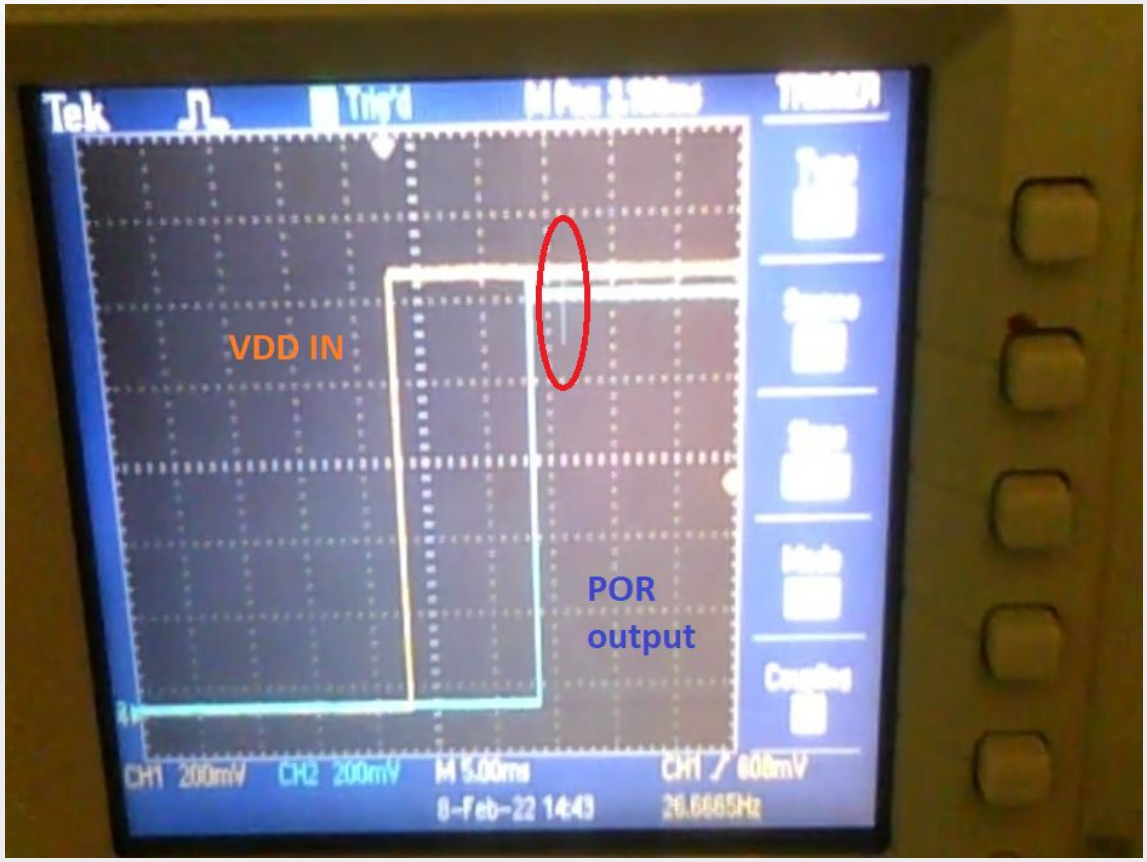
Test radiation environment

1) Radiation tests were performed in PNPI at Gatchina according to GOST 15.101-98
2) Bunch characteristics:
   a) particles, energy: protons, 1 GeV
   b) bunch diameter, uniformity: 19 mm, 5%
   c) fluence: $5 * 10^7$- $5 * 10^8$ particles / cm^2 / s
3) Experiment characteristics:
   a) Irradiation duration: 10 hours
   b) Average fluence: $2 * 10^8$ particles / cm^2 / s
   c) Total fluence: $2.54 * 10^{12}$

First results

2 types of test records:

- analog type (video record from scope to camera)
- digital one (signals, digitized by ADC) – now in data processing



Next version of the chip – Hub v2

Destination:

1) Shift to a new process – 90 nm CMOS of Mikron (Zelenograd).
2) Study measures to improve the radiation resistance of the IP blocks against heavy charged particles
3) Optimize the size and functionality of the digital blocks
4) Study chip caseless usage at board level. The flip-chip technique is not considered at the moment
5) The chip should be a socket compatible with the manufactured Demonstrator board (one for Hub v1 chip)

Hub v2 schedule

1) Redesign of the Hub v1 from TSMC 65 nm CMOS process to Mikron 90 nm one (readiness of the GDSII-file – Feb. 2023)
2) Chip processing at Mikron (late 2023, tens pcs.)
3) Lab evaluation board design and manufacturing (late 2023)
4) Test results (spring 2024)

Summary

- Since the last MPD meeting two versions of PCBs for study the Hub v1 ASIC were designed and manufactured to develop:

  - Lab test bench to check chip functionality
  - Demonstrator board for TPC

- Elaboration of the specifications for the 2nd chip version has been started. It should be compatible with 90 nm CMOS process of Mikron factory at Zelenograd