Range (Muon) System Status Report

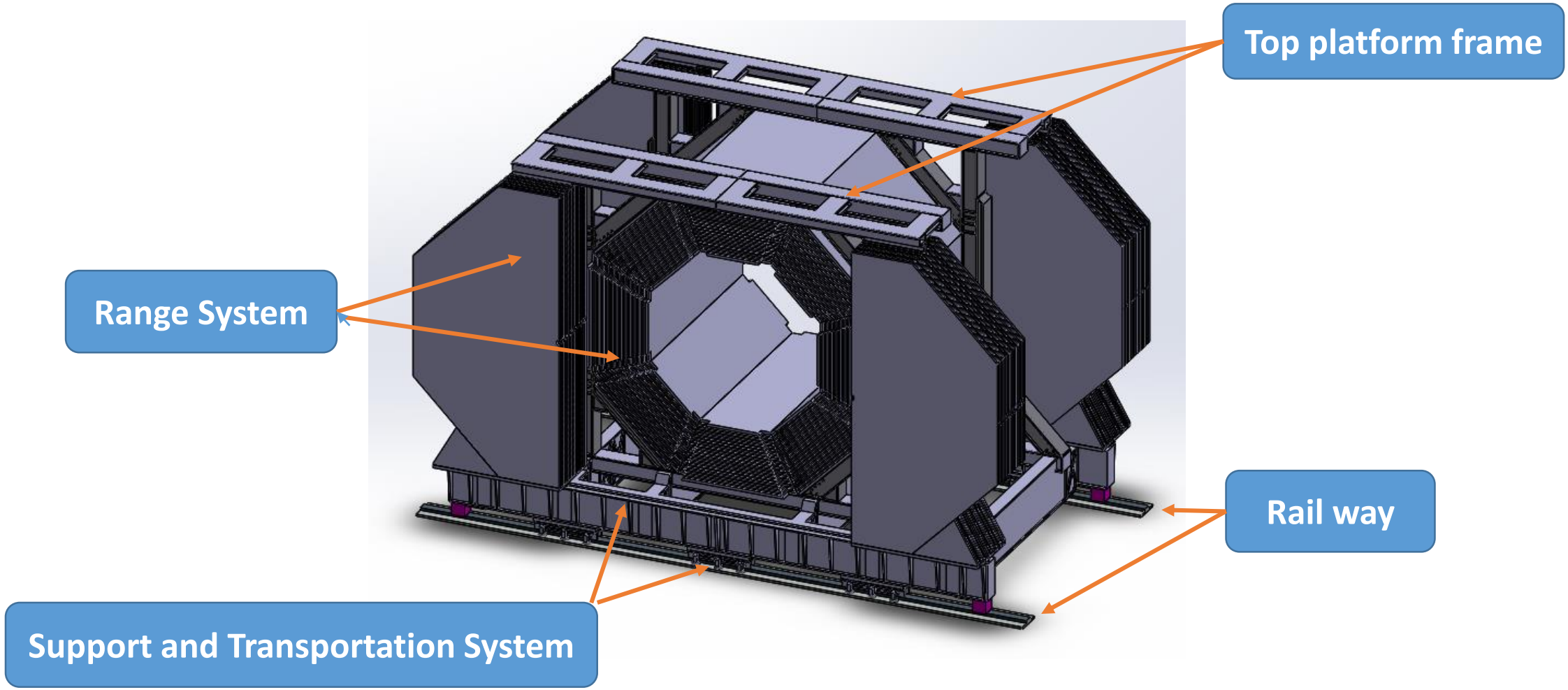
G.Alexeev, SPD collaboration meeting, Dubna, 4 October 2022

- **Main results for last year (brief review):**
  - **The basis for MDTs mass production is established** – JINR directorate has finally decided to deliver building 73 to the Laboratory of Nuclear Problems for deployment of MDTs workshop
  - AGRISOVGAZ has produced pilot bunch of extruded ALU profiles (main component of MDTs)
  - Mechanical FEA calculations (deformation, stress) for the whole SPD setup is finalized (adding of magnetic forces is pending the final version of the solenoid)
  - Test stand (imitation of the RS slot with MDTs, strip boards and analog FEE) is in progress
  - RS prototype for Nuclotron test beam is close to completion: MDTs, analog and digital cards are in place; gas, HV, LV systems are connected; DAQ software is in progress
  - New ASIC chips (Ampl-8.52, basis for analog FEE) with very low input impedance for wire and strip readout are manufactured by Integral (Minsk), and amplifier is close to its final version
  - Software/algorithms - > particles identification in Range System

- **Plans for 2023**
- **Conclusion**

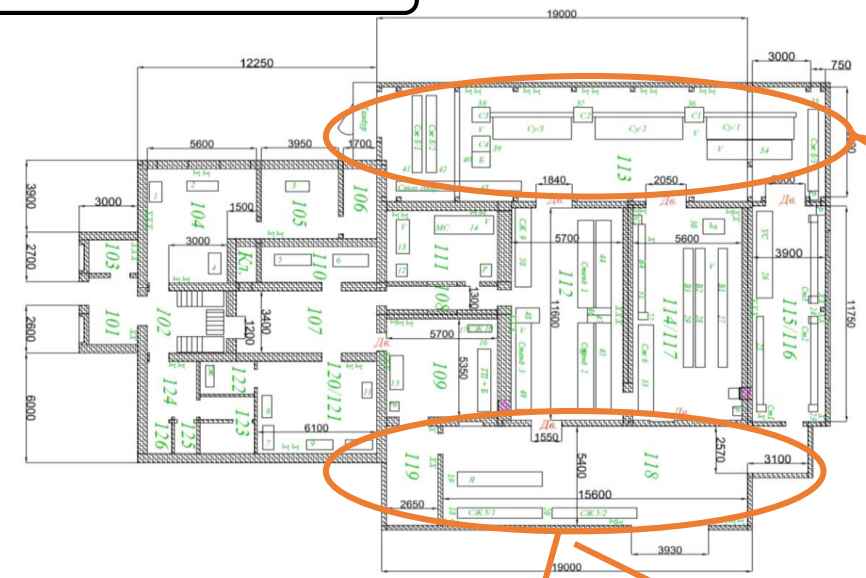
Full 3D model of SPD setup (SPD TDR), total weight 1147 ton

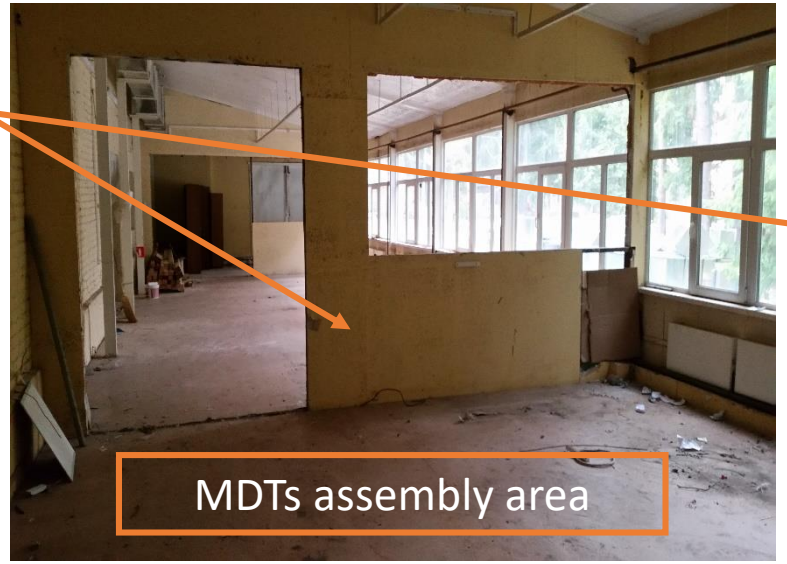
used for FEA calculations (stress and displacement), including all inner detectors, solenoid, etc.



Basis for deployment of MDTs assemble and test areas

Bld.73, 1-st floor plan

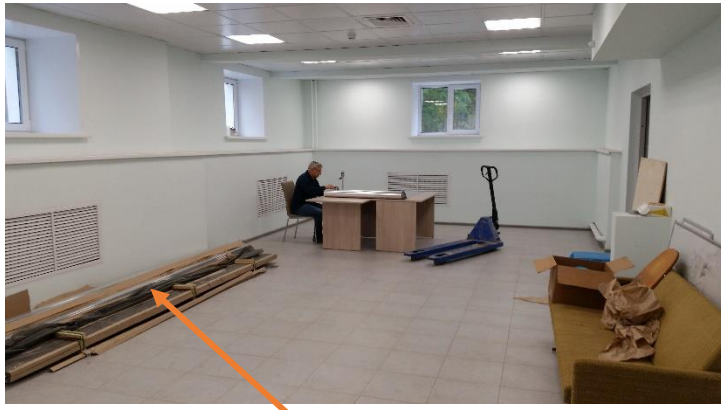




Stand-imitator of the RS slot

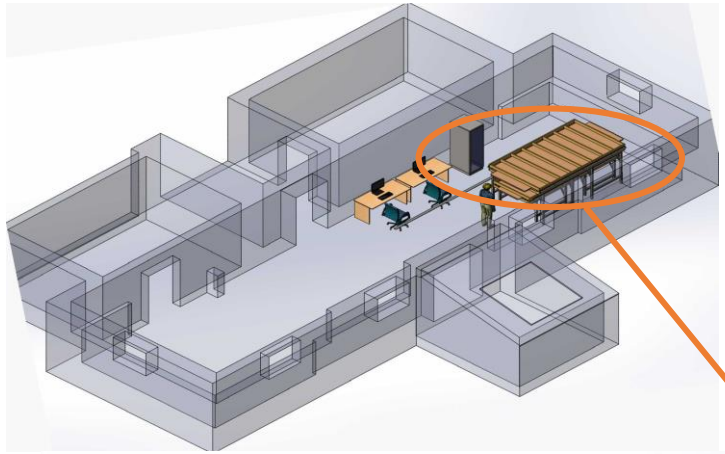
(35 mm gap between Fe plates of absorber)

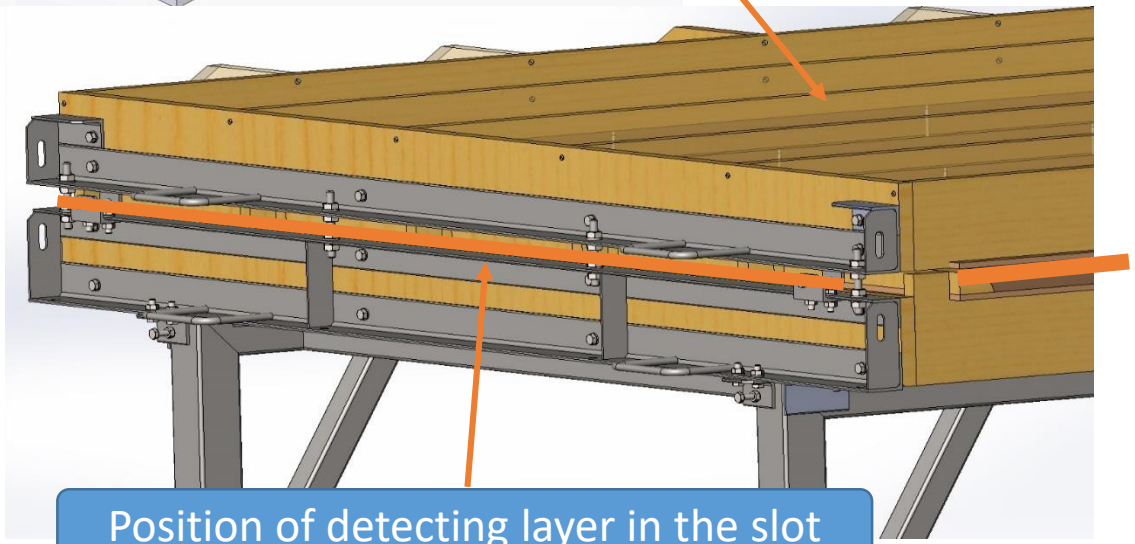
Photos of the Lab with first bunch of ALU profiles



First portion of aluminum profiles (basic component of MDT detectors): 110 units by 4 m long each (~ 110 kg)

3D model of the Lab with stand-imitator: optimization of MDTs positioning, strip board design, analog FEE cards, cabling, etc.





Position of detecting layer in the slot

Main components of the stand-imitator at DLNP workshop:

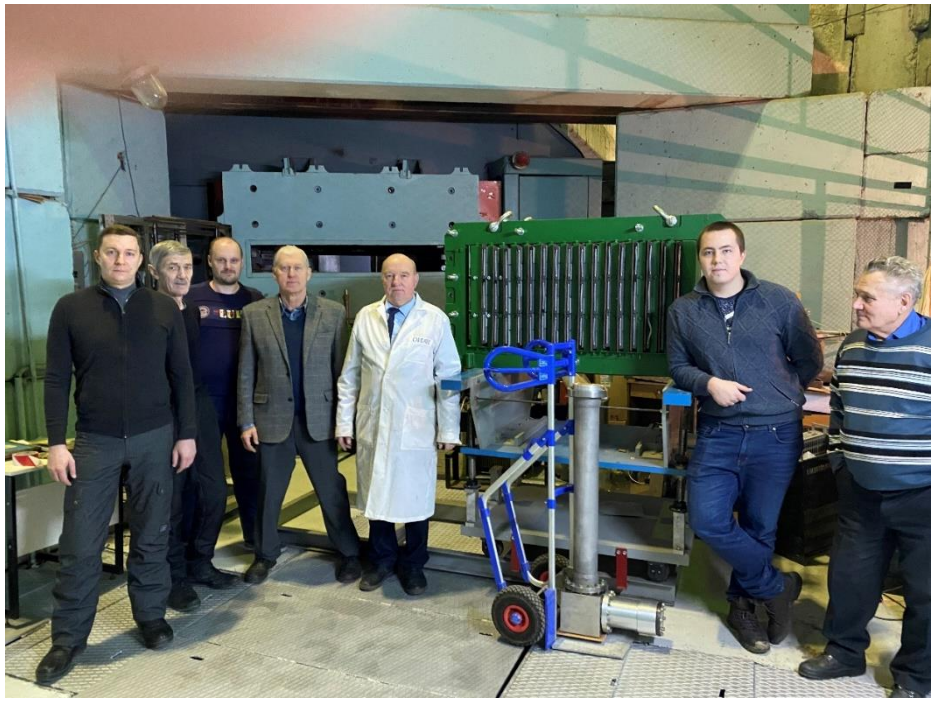
steel support&transportation frames

(special)plywood&wood structures

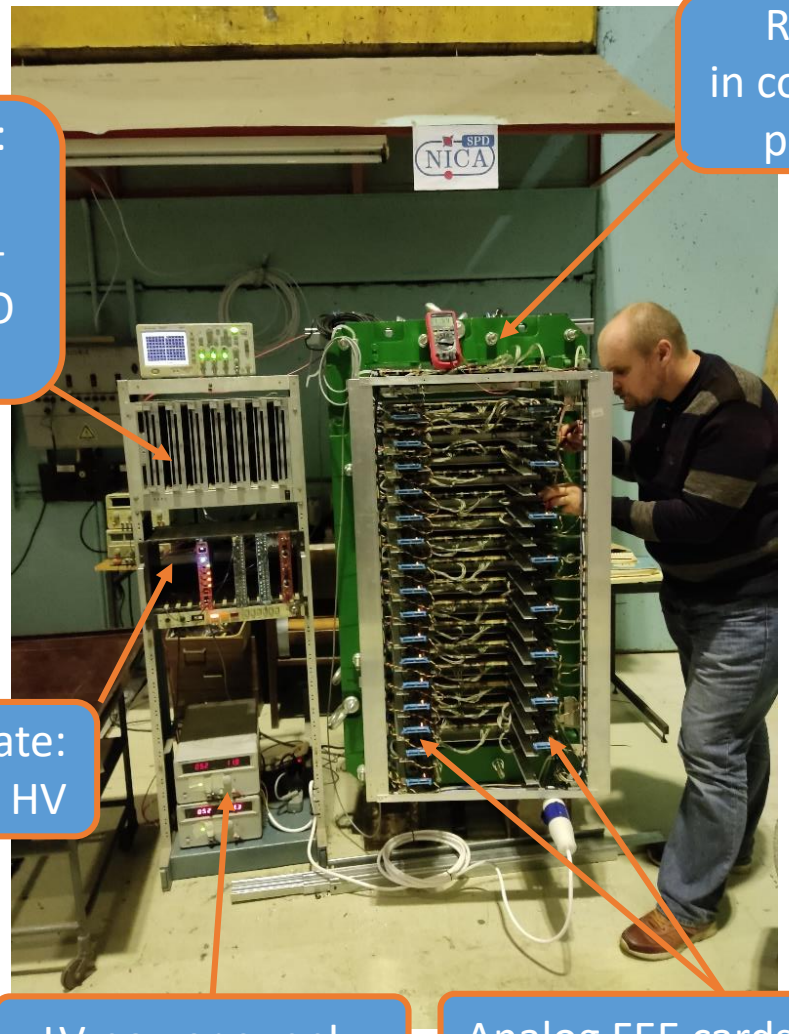
Two slots will be modeled: smaller (3.9 x 1.22 m2) and bigger (3.9 x 1.76 m2)

Range System Prototype at Nuclotron test beam area

December, 2021



October, 2022



RSProto in cosmic test position

VME 6U crate: 7 digital FEE cards (MFDM-192), 1344 R/O channels

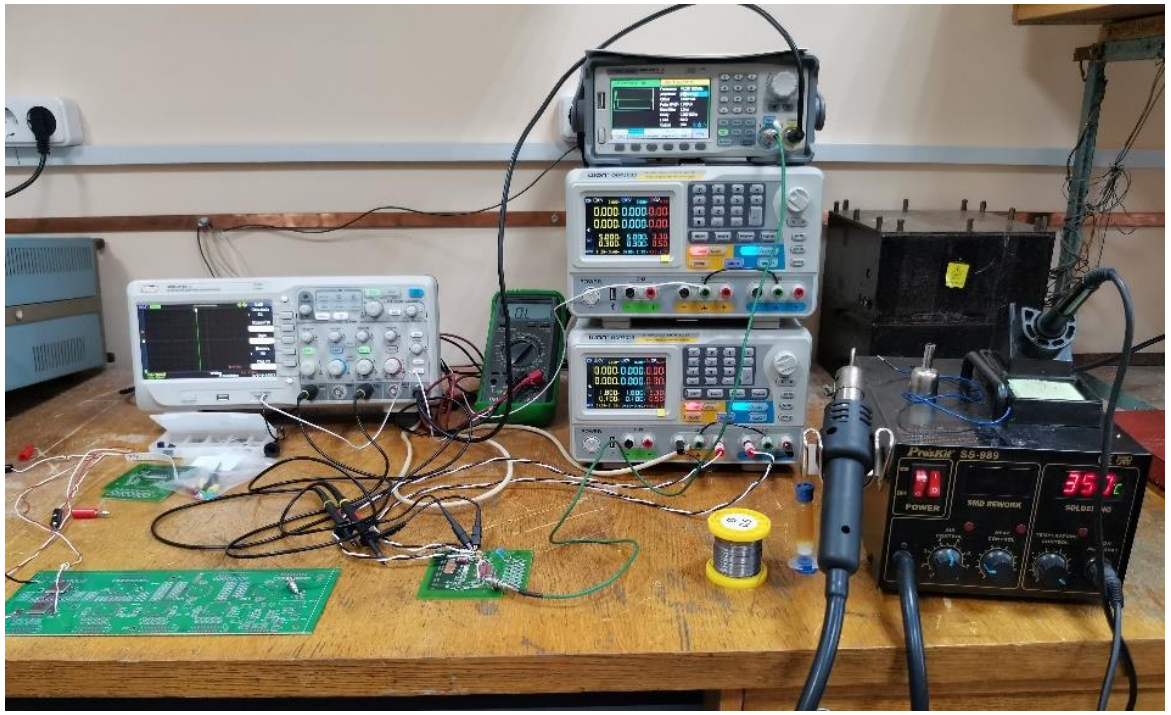
NIM crate: trigger, HV

LV power supply

Analog FEE cards (ADB-32)

Ampl-8.XX R&D progress

2021 status: **Ampl-8.51** (low input impedance amplifier for both wire and strip signal R/O) was designed and manufactured. Tests revealed multiple operation problems due to mistakes in chip topology, but tests of Ampl-8.51 single channel (individually powered channel with disconnected common chip busses) proved that its parameters perfectly fit the design request.



Ampl-8.52 and Ampl-8.11R test stand

New tasks!

- **Ampl-8.52.** Design of a new metallization for unfinished Ampl-8.51 that would eliminate or minimize poor topology effects to prove possibility of a combined 8-channel stable operation of the chip
- **Ampl-8.11R.** Parallel design of a low input impedance current amplifier that can be used as a preamplifier for strip R/O in tandem with Ampl-8.3 or Ampl-8.5x.

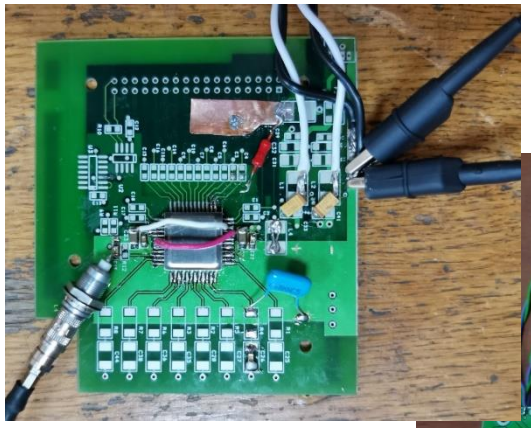
Both tasks were fulfilled this year!

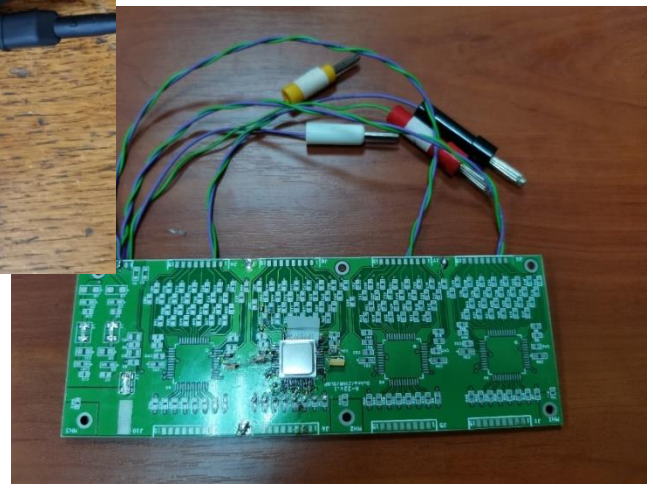
- **Ampl-8.52** was designed, manufactured and tested. Reliability of its 8-channel operation is proved, general parameters fit the request!
- **Ampl-8.11R** was designed, manufactured and tested. General parameters fit the request!

New task!

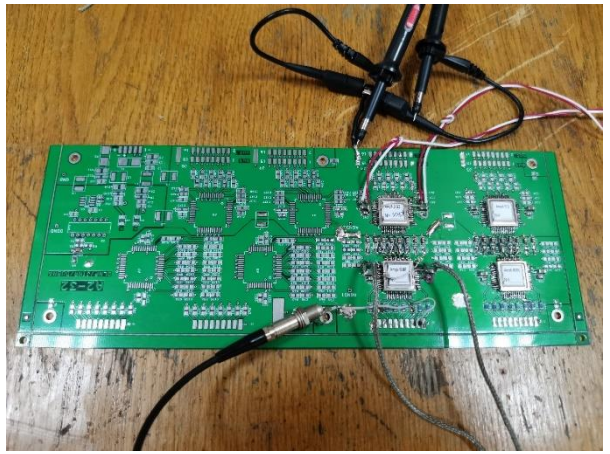
- **Ampl-8.53.** As Ampl-8.52 is just a partial correction of Ampl-8.51 chips, we still need a totally new design of chip topology that will correspond all circuit peculiarities and will fully reveal its potential.

Ampl-8.52 & Ampl-8.11R

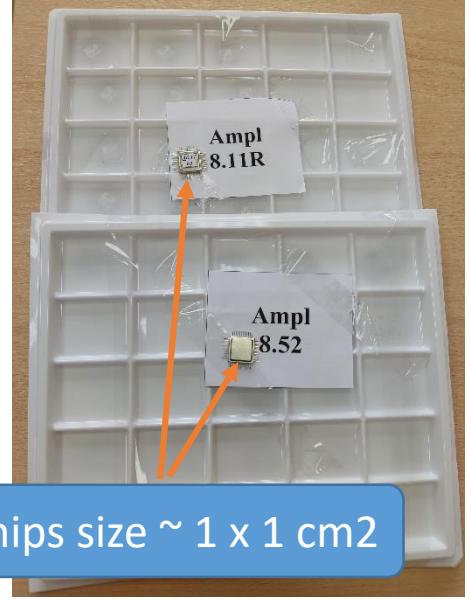




Ampl-8.52 ready for tests



Ampl-8.11R in tandem with Ampl-8.52



40 pcs of each type manufactured

	Simulation for Ampl-8.51	Measured for Ampl-8.52
Input impedance (10MHz)	0,9÷2,2 Ohm	0,6 + 8,43 (9,03)Ohm*
Gain	100÷150 mV/µA	120 mV/µA (Vps= ±2,2V)
		148 mV/µA (Vps= ±3V)
Output offset, V	≤ 1V	≤ 0,3V
Rise time/fall time	8÷12 ns	5÷8 ns
Inoise (CD= 1,8nF)	315 nA	240 nA
Dynamic range (CD= 0nF)	48 dB	~ 50 dB
Crosstalk	< -40 dB	< -57 dB
Dissipated power (Vps= ±3V)	510 mW	423 mW

Ampl-8.11R	Simulation	Measured
Input impedance (10MHz)	3,5÷4 Ohm	3,9 Ohm
Gain	2,85÷3,13	3
Rise time/fall time	3÷4 ns	5 ns
Dissipated power (Vps= ±3V)	192 mW	201 mW

* 0,6 Ohm (perfect result!) is an input impedance of the channel itself, but the input connection lines of the produced Ampl-8.52 chips have 8,43 Ohm impedance (instead of 2÷2,5 Ohm) resulting in increased summary input impedance. We should pay this a special attention while producing next (final) teration -> Ampl-8.53.

Digital FEE units

COMPASS-like DAQ -> test beam

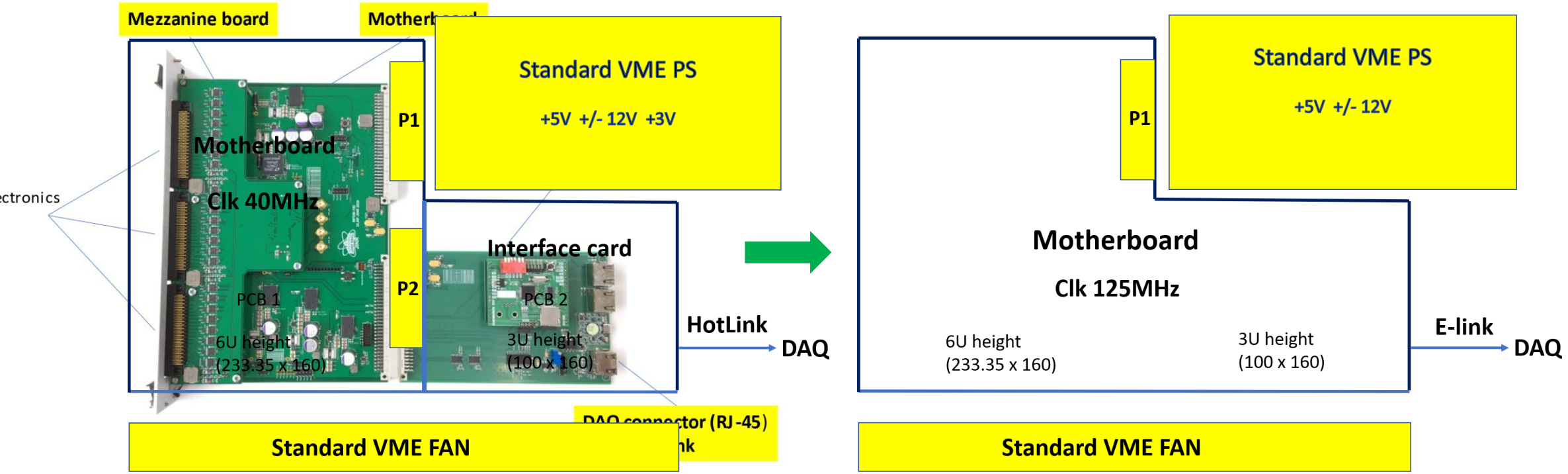
MFDM-192, two PCboards,

7 units (1344 R/O channels) for RSProto

SPD DAQ -> NICA

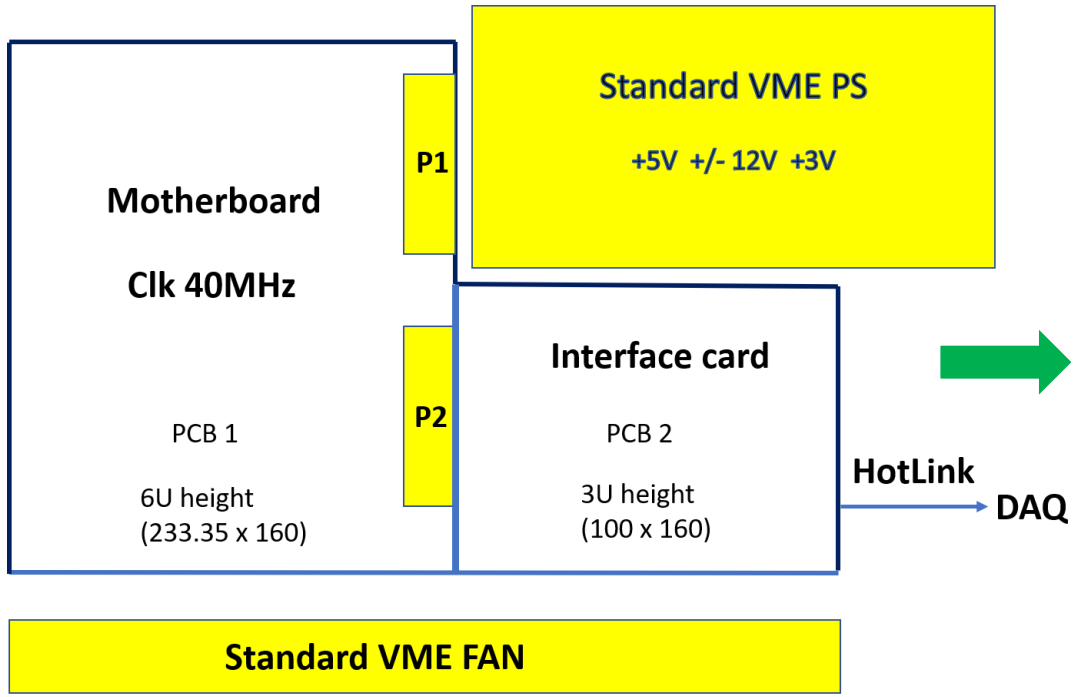
FDM-192, single board,

in development

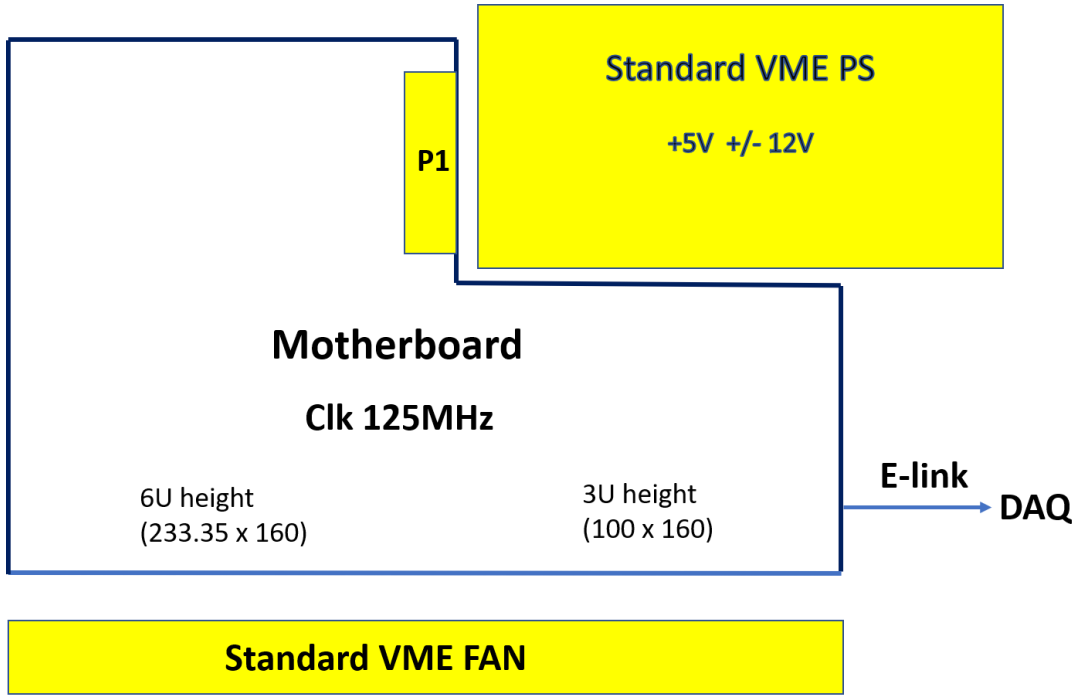


Digital FEE units in different VME 6U crates

Standard VME crate with P1 & P2 connectors/backplane



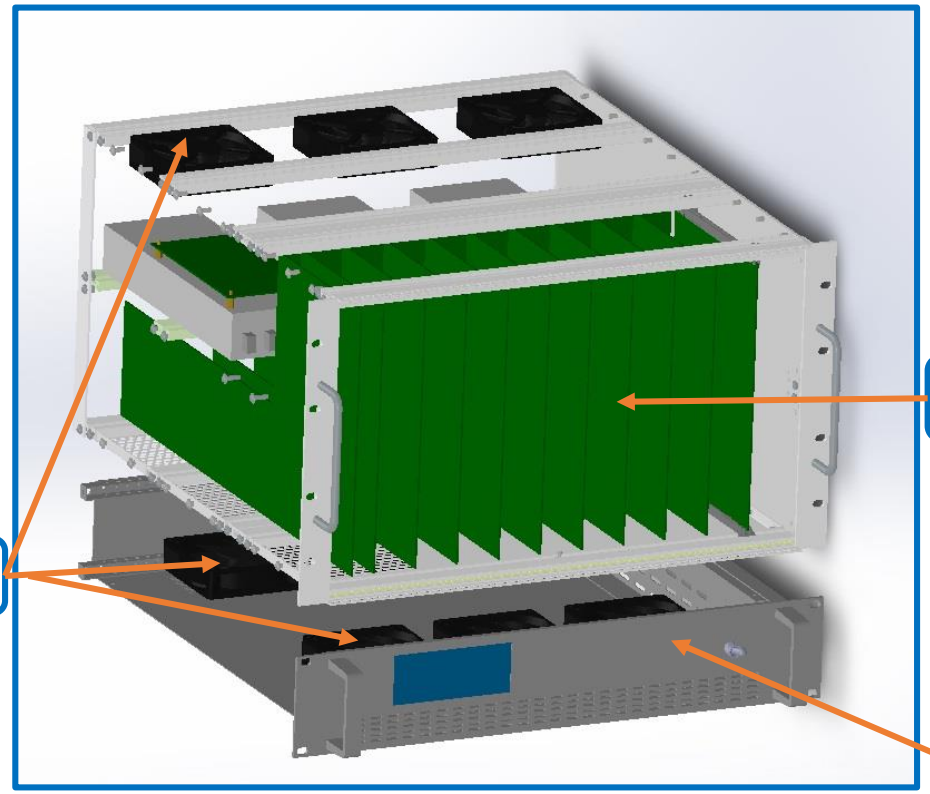
Special (for RS) VME crate with only P1



VME 6U crates (3D model)

to be produced in 2023

Front view

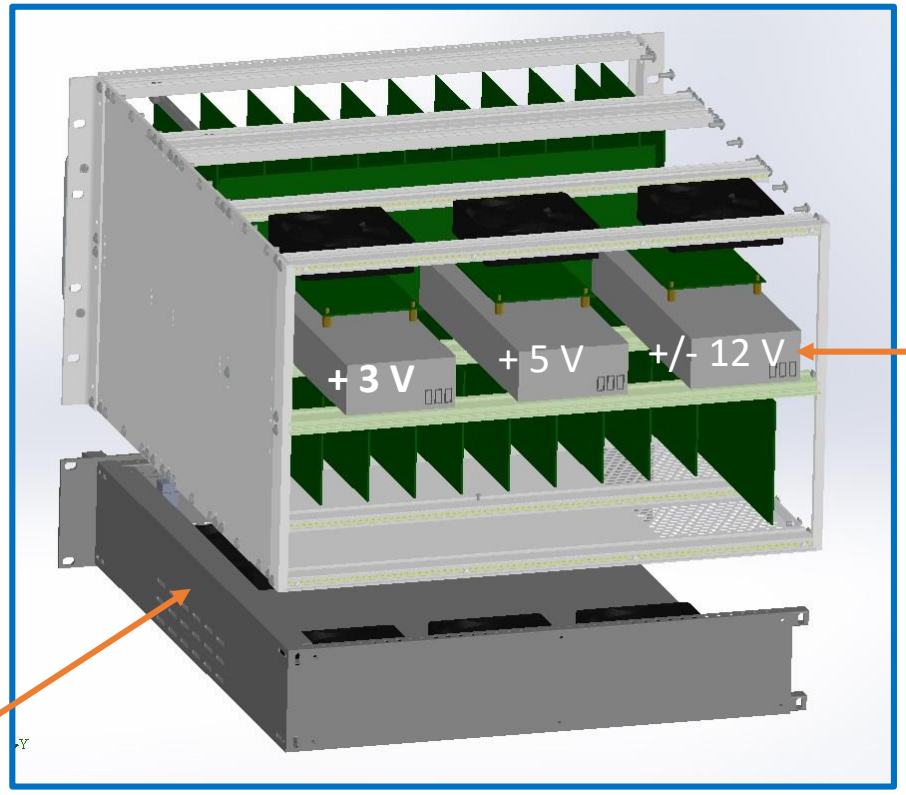


VME cards

Fans

Fan tray

Back view



Power Supply units

Plans for 2023

- **Reconstruction of bld.73 and deployment of MDTs workshop**
- **Finalizing mechanical FEA calculations (including magnetic forces)**
- **Start of stand-imitator for optimizing the detecting layers design**
- **Putting RS-prototype and pressurized Cherenkov counter in operation at test beam**
- **Production and tests of the final version of amplifier ASIC chip(s)**
- **Design and production of “final” digital FEE unit with E-link interface**
- **Design and production of VME 6U crates**
- **Continue work on software/algorithms developments**

CONCLUSION

Decisive moves which happened this year in getting the basis for MDT detectors production, restart of aluminum profile production by AGRISOVGAZ and development and production of analog ASIC chips in Minsk and digital FEE modules in Moscow provide the foundation for further progress of Range System.

At present we feel confident that provided the proper financing it is possible to start Range System construction in 2024.

Backup slides

Digital FEE unit (FDM-192) and VME crates

Status

The hardware design of a “final” digital FEE unit with E-link interface (**FM-192**) is close to be completed. The contract on production of test units is close to be signed.

The design of a **6U VME crates** for digital FEE units is in preparation with an aim of their further production in Russia. Presently we plan to develop two types of crates: a standard one (with full backplane, connectors P1, P2), and a special one for the RS system (connector P1 only).