SPD DAQ, current view

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on behalf of DAQ group

Estimation of raw data flow

Bunch crossing each 80 ns; crossing rate 12.5 MHz,
Collision rate ~3–4 MHz →
Triggerless DAQ to avoid any hardware biases

Data flux was estimated for the maximum luminosity L = 10^{32} $cm^{-2}c^{-1}$ and maximum energy √s = 27 GeV.

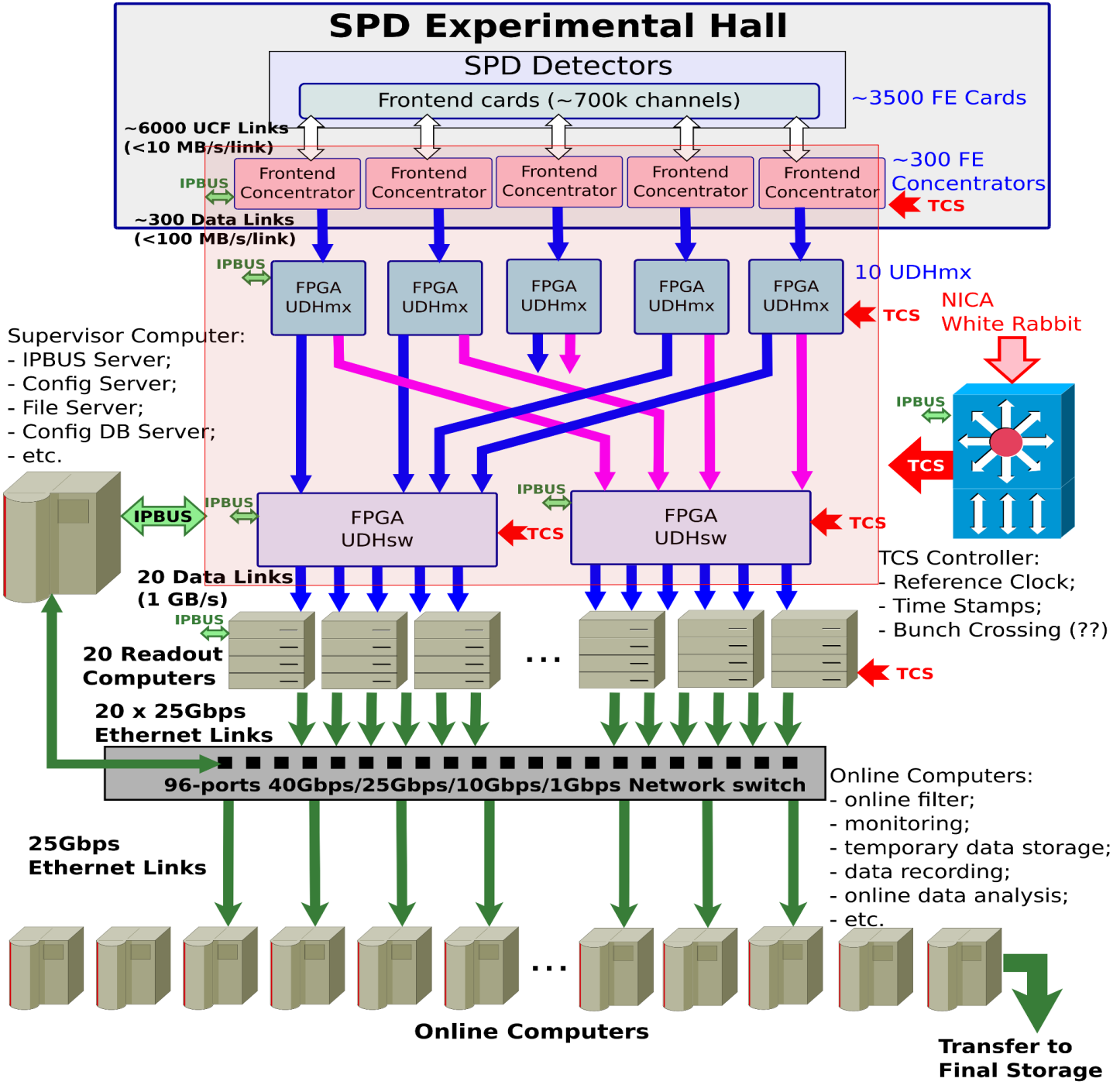
Within simplified simulation and some safety margin the data flux is estimated as 20 GBytes/s.

Front-end electronics for the free-running DAQ-SPD

Front-end electronics of the detectors has to meet the requirements of a free-running DAQ

General FEE requirements from the DAQ system:

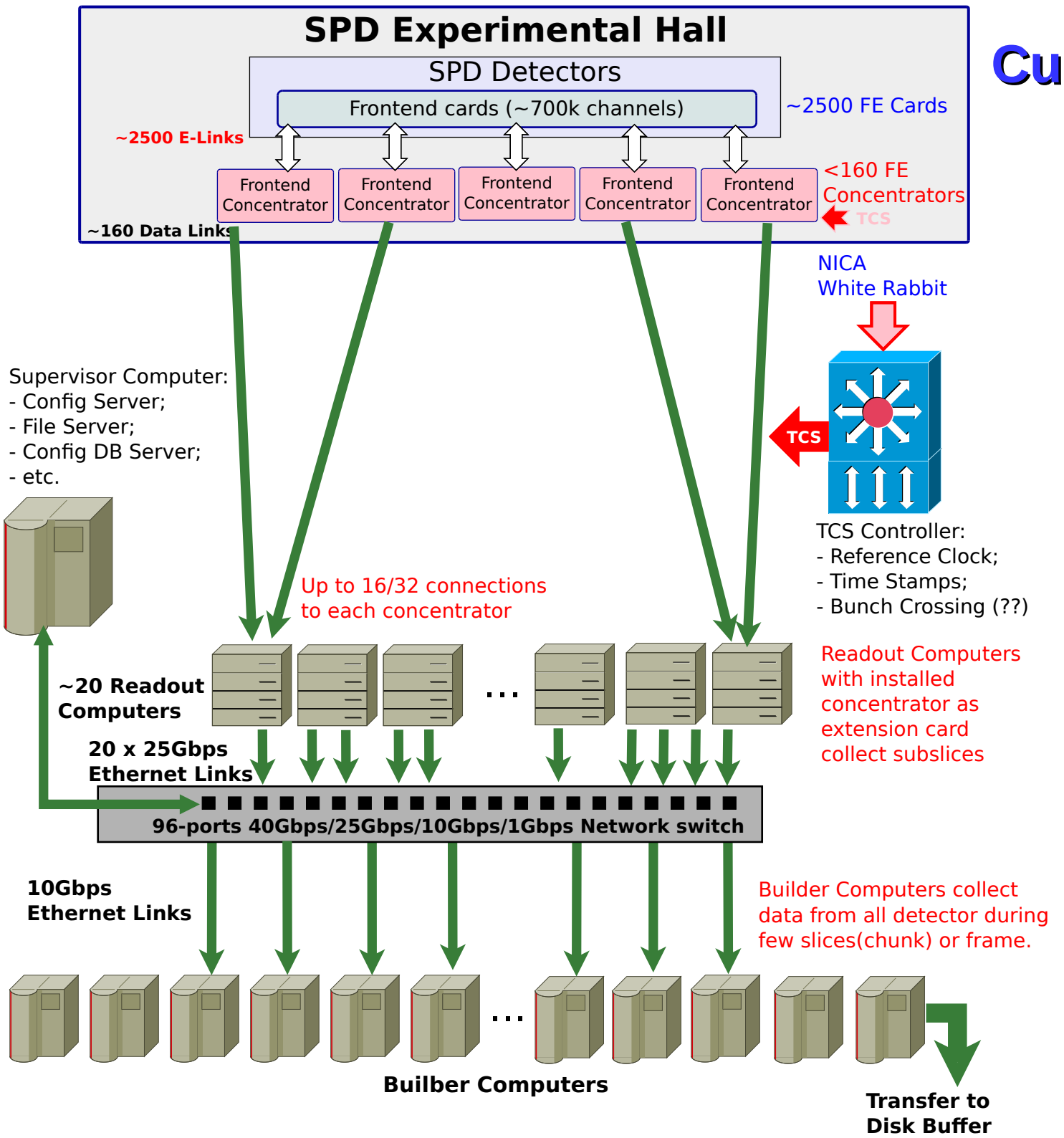
- Self-triggered (*trigger-less*) FEE operation
- Digitizing on-board
- Timestamp included in the output format
- Large memory to store the data accumulated in a time slice
- Zero suppression



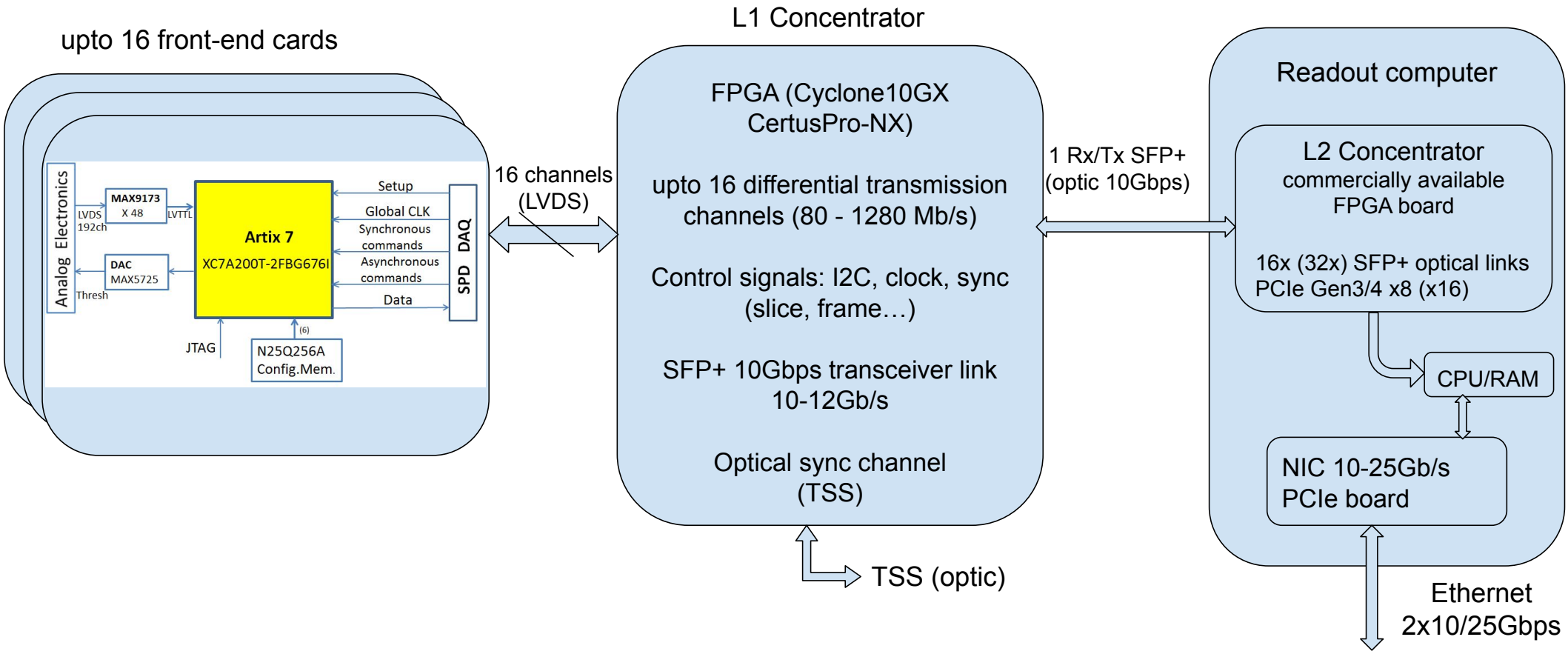
CDR version of DAQ have been based on ideas and hardware developed by Igor Konorov group from the Technische Universität of München (TUM) for COMPASS/AMBER experiment

Thanks to colleagues for the big help at our start.

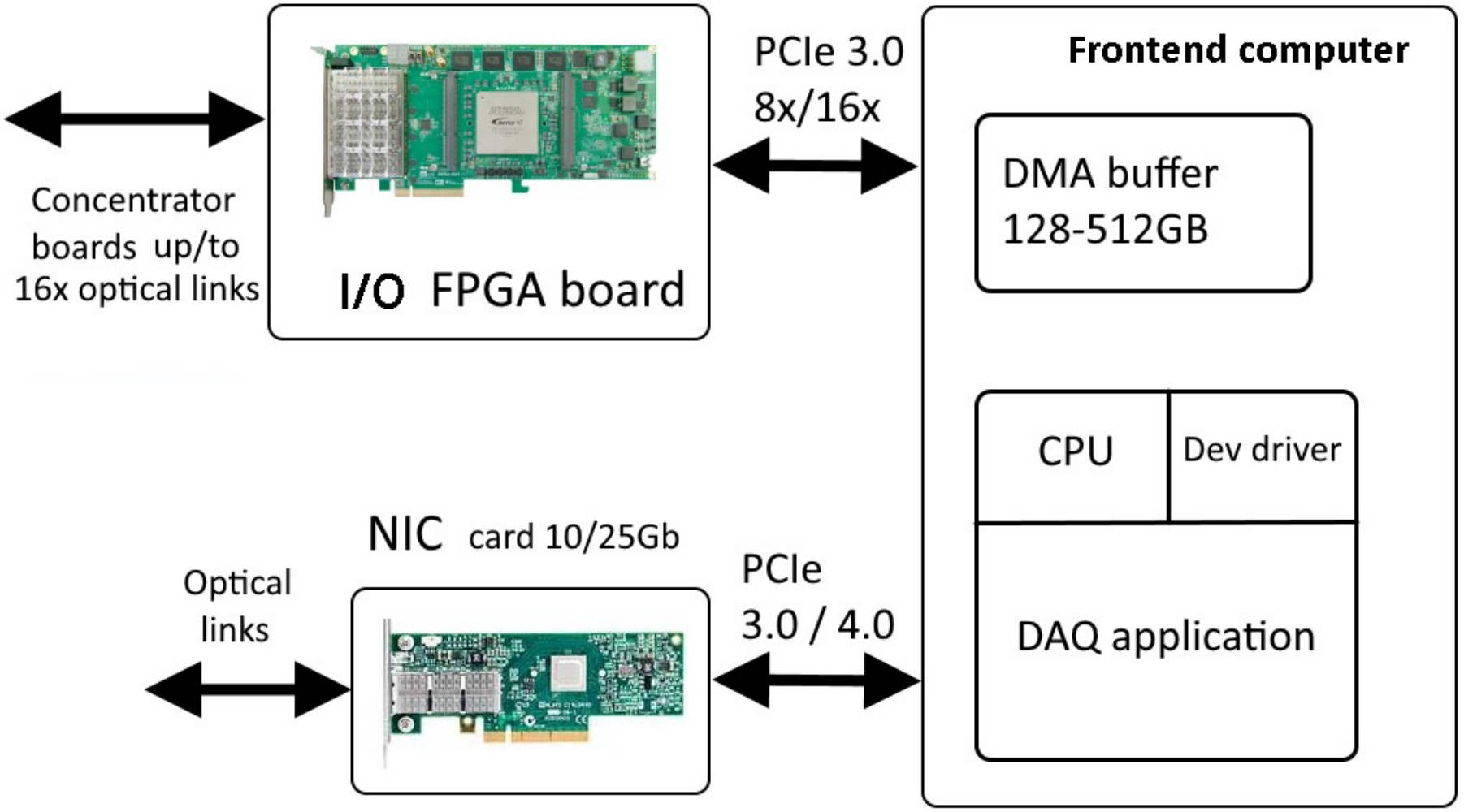
Current idea of DAQ



Current idea of DAQ



Frontend computer



E-link signals for Range System via the displayport cable

FrontEnd DisplayPort Connector		
Signal Type	**Pin Name**	**Pin**
GND	GND	2
Out	ML_Lane 0 (p)	1
Out	ML_Lane 0 (n)	3
GND	GND	5
In	ML_Lane 1 (p)	4
In	ML_Lane 1 (n)	6
GND	GND	8
In	ML_Lane 2 (p)	7
In	ML_Lane 2 (n)	9
GND	GND	19
In	Hot Plug Detect	18
IO	CONFIG1	13
In	CONFIG2	14
GND	GND	11
In	ML_Lane 3 (p)	10
In	ML_Lane 3 (n)	12
GND	GND	16
In	AUX_CH (p)	15
In	AUX_CH (n)	17
	DP_PWR	20

Data e-link

Start of slice

Start of frame

Reset

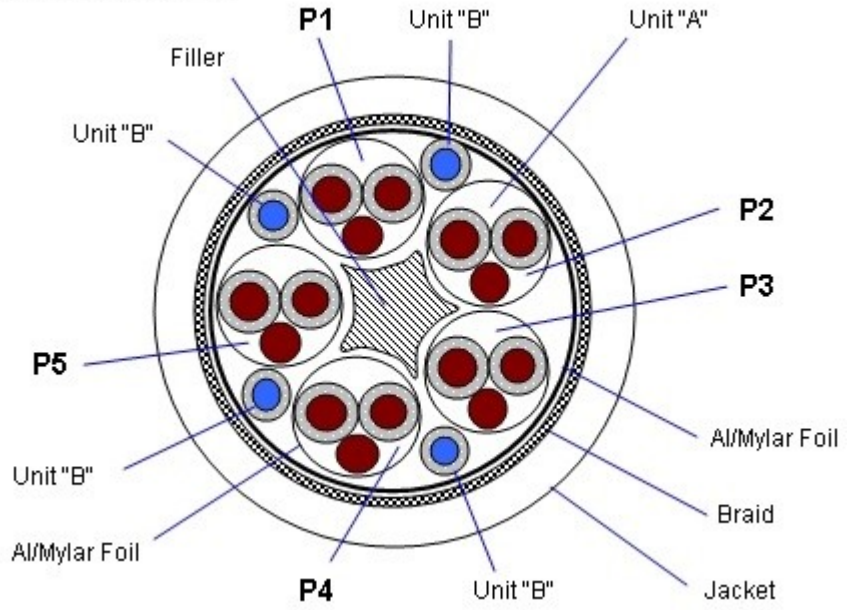
I2C SDA SCL

Set Next Frame

Global clock

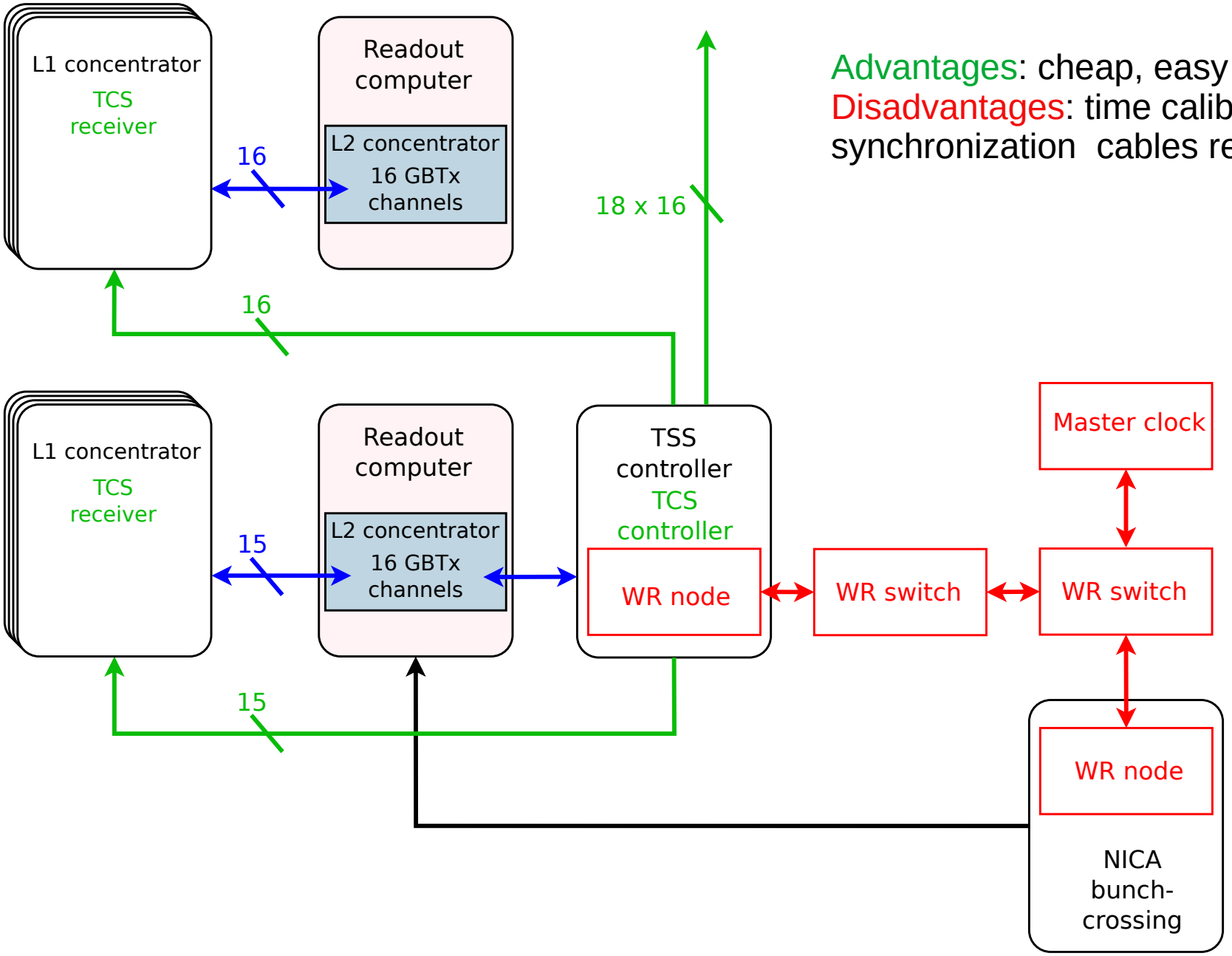
spare signal

Cable construction:



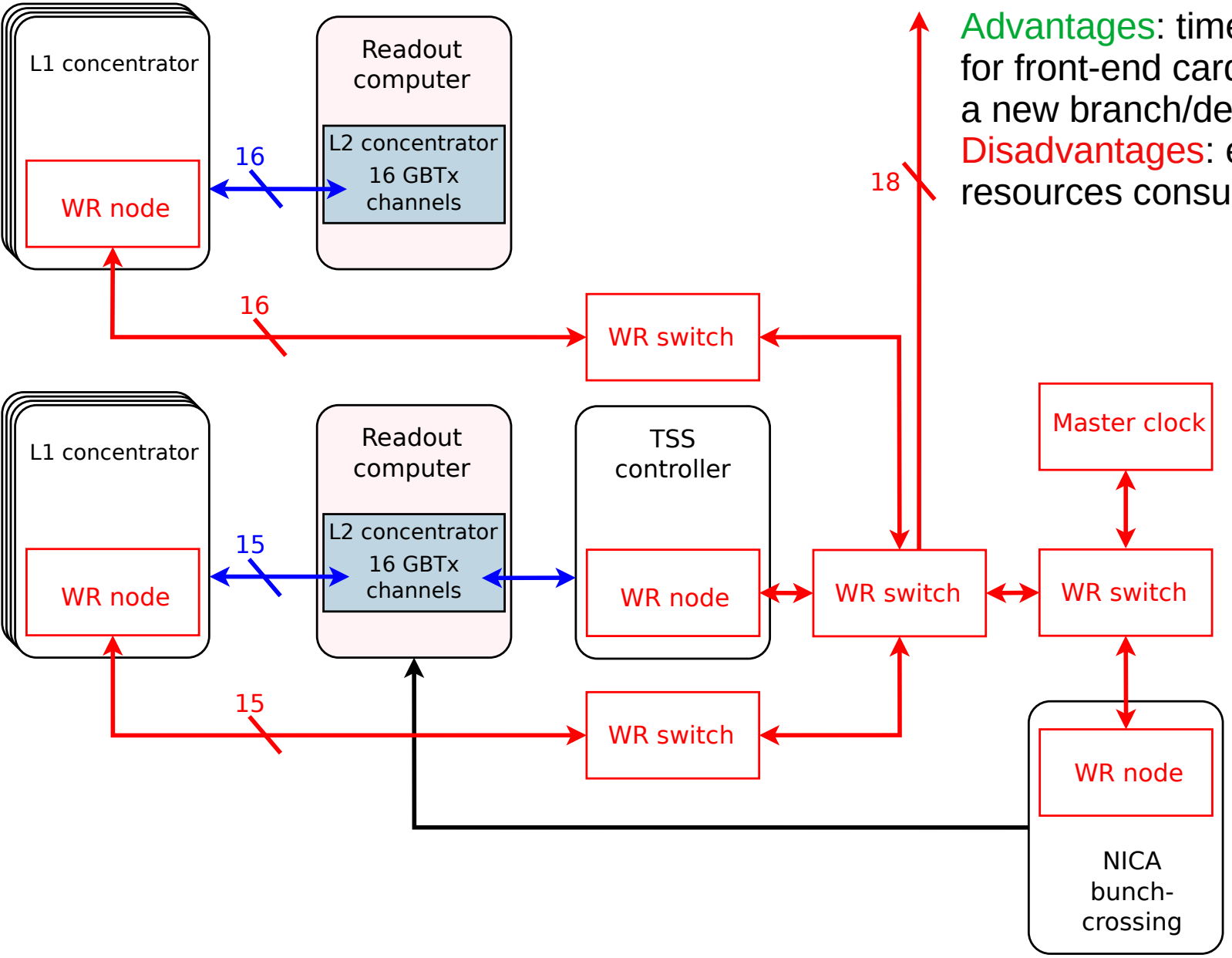
- Cable/connector – DisplayPort (20 pins)
- 5 differential signals (link 1(2), clock, slice, frame)
- I2C bus
- 3 control signals (reset, hotplug, spare)

Time Synchronization System with TCS-based delivery



Advantages: cheap, easy implantation.
Disadvantages: time calibration of all synchronization cables required.

Time Synchronization System with WR-based delivery



Advantages: time calibration needed for front-end cards only. Easy adding of a new branch/detector at any distance.
Disadvantages: expensive, time and resources consuming implementation.

Open questions

- Front Electronics cards exists for RS only. Development of dedicated ASICs is started.
- Development of L1 Concentrator: Which FPGA circuit ???
- Where L1 Concentrator will be installed: inside or outsides the Range system?
(e-link <10m)
- Radiation hardness of FPGA, in the case of installation of L1 Concentrator inside the Range system
- Which Time Synchronization: White Rabbit or TCS. A working bench for development of the White Rabbit node now is under production.

R&D is required

Thank you for your attentions.