DAQ hardware

Exploring the possibilities of L1, L2 concentrators' design

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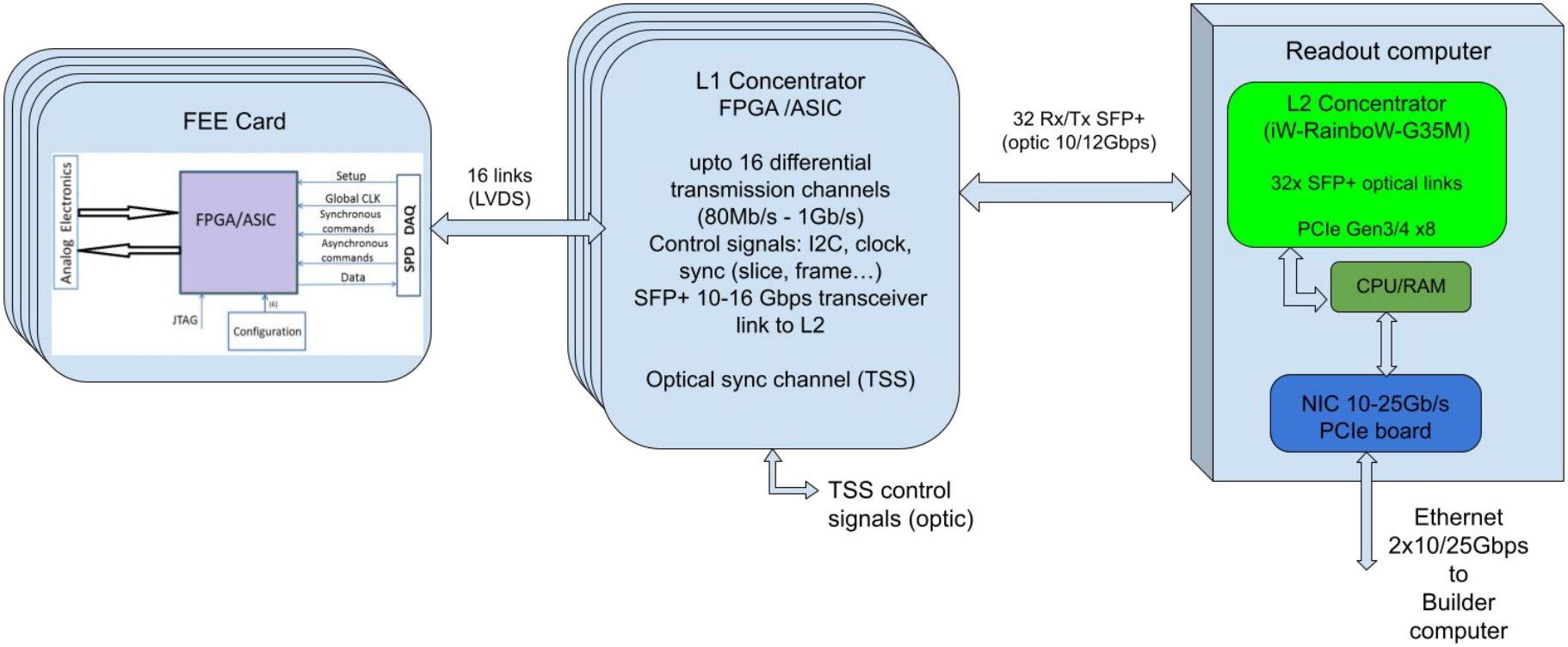
SPD detectors' outputs (at the first stage)

Sub-detector	Information type	Number of channels	Channels per FE card	Number of e-links
Micromegas	T + A	~15000 (25600)	128	118 (200)
Straw tracker	T + A	30208	128	236
BBC (inner+outer)	T + (T + A)	256 + 500	32	8 + 12
Range System	T	130200	192	679
ZDC	T + A	1050	64	17
Total (max)		177214 (179598)		1070 (1152)

Hardware requirements at the first stage

- number of channels is over ~180000
- e-link quantity ~1100
- If we assume that one link is supposed to read one FEE board, then we need ~70 L1 concentrator boards (each with 16 links)
- In this case, we need 3 L2 concentrator boards (each with 32 links)
- The data rate estimation for the full scale experiment does not exceed 20 GB/s (for the full scale experiment)
- The total bandwidth of 70 L1 concentrator boards (with 10Gb/s transceivers) is about 700 Gb/s
- If we use the PCIe 3.0 x16 bus for L2 concentrator boards , the total bandwidth will be about 36GB/s

SPD readout chain



L1 concentrator board

Unfortunately, today we do not have a clear solution for the L1 concentrator board. Today we have no possibility to purchase the appropriate chips for an FPGA-based solution, and on the other hand, we have not necessary amount of chips for an ASIC-based solution. Besides, ASIC-based solution seems to be very expensive.

iW-RainboW-G35M module as possible base for L2 concentrator board

- SoC
  - Xilinx Zynq UltraScale+ MPSoC
  - Quad Cortex A53@1.5GHz
- Memory:
  - 4GB DDR4 for PS with ECC
  - 8GB eMMC Flash
- On SOM Features
  - 10/100/1000 Ethernet
- Interfaces:
  - PL GTY Transceivers x 16 @ 32.7Gbps
  - PL GTY Transceivers x 32 @16.3Gbps
  - 48 LVDS/96 SE/32

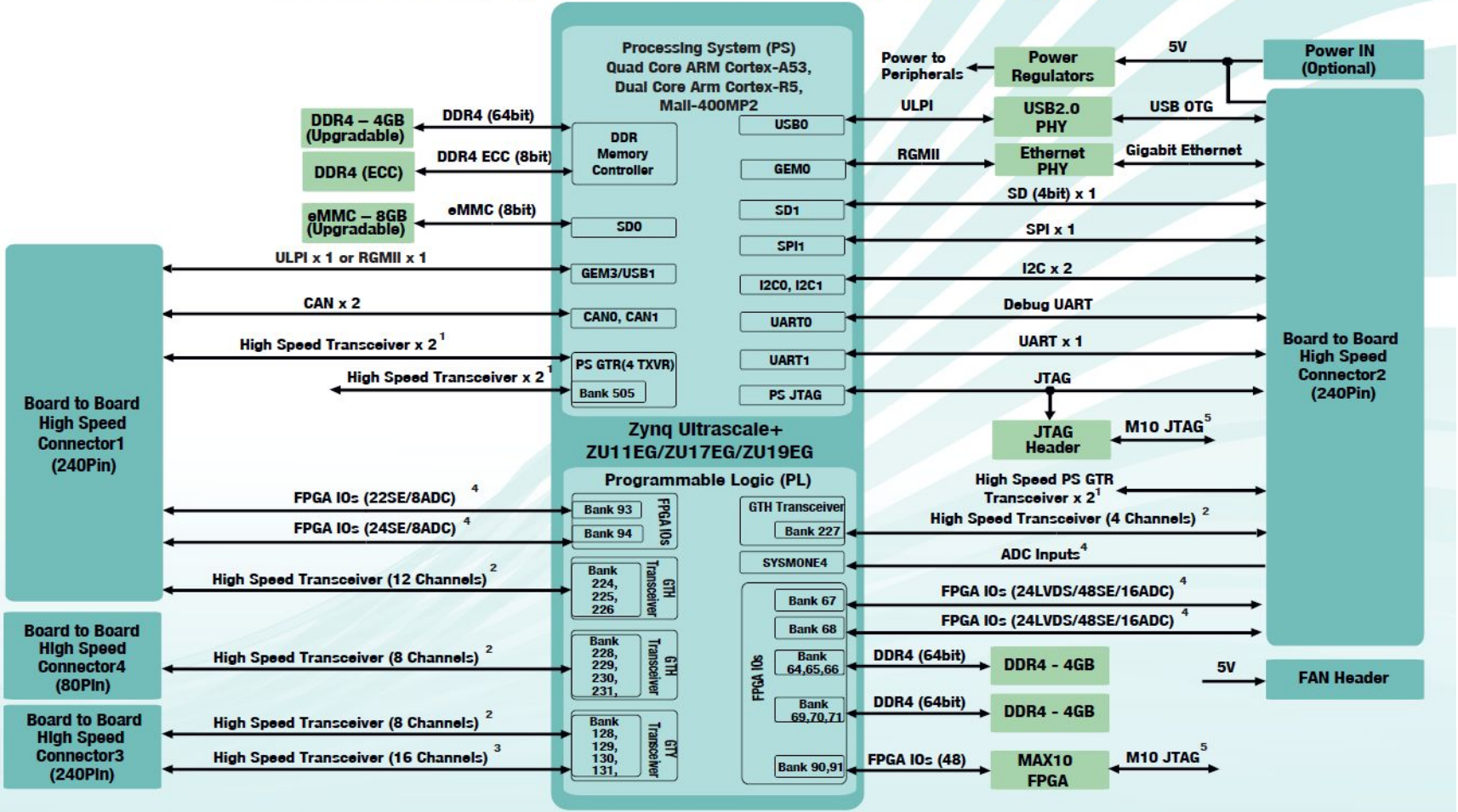
Form Factor: 110mm x 75mm

Conclusions

- Today, we do not have a feasible solution for L1 concentrator board.
- If the situation goes not worse, then the option of creating an L2 concentrator board based on the iW-RainboW-G35M module looks quite reasonable.

Backup

ZU19/17/11 Zynq Ultrascale+ MPSoC SOM Block Diagram



Test with 10Gb ethernet (over UDP)

A trial version of the firmware for the Cyclone 10GX chip has been made and it allows us to transfer data to a computer at a data rate of 10Gb/s.