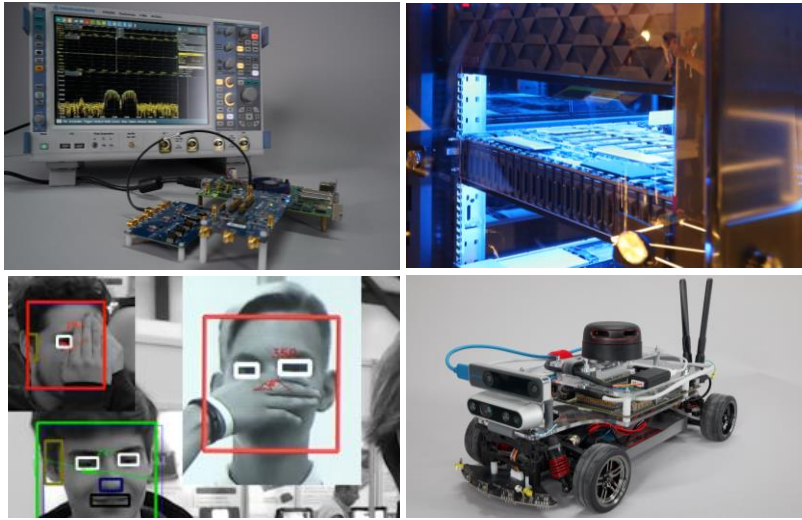
POLYTECH
Peter the Great
St.Petersburg Polytechnic
University

POLYTECH
Advanced Manufacturing
Technologies Center
National Technology Initiative

POLYTECH
Laboratory
Industrial Systems for
Streaming Data Processing



SPD Collaboration Meeting

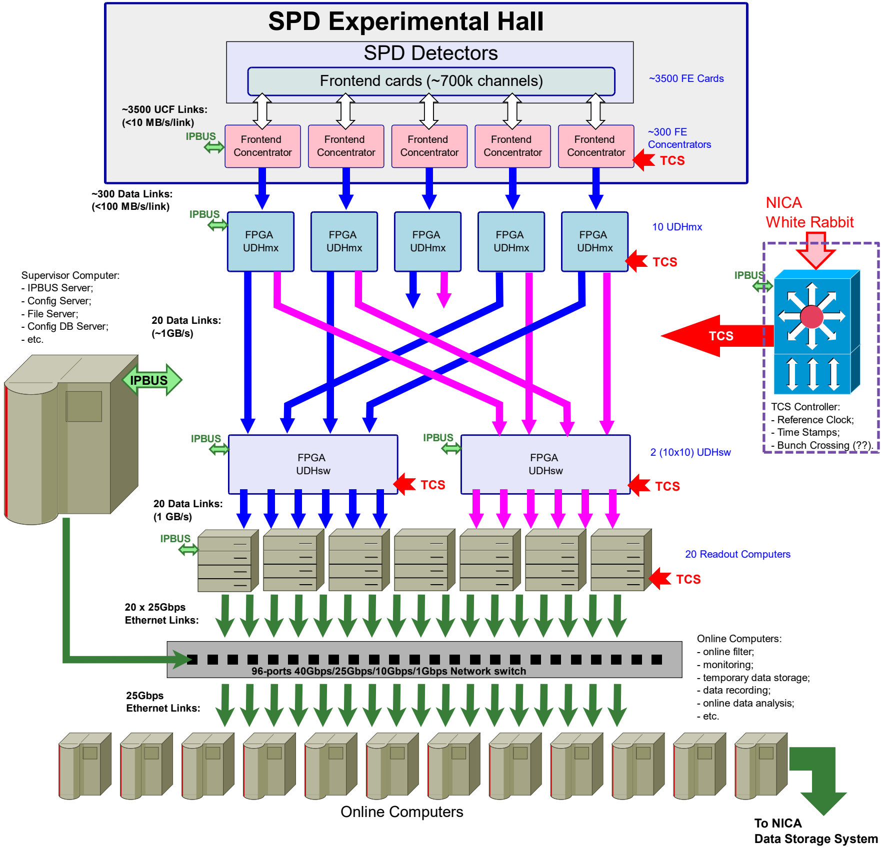
October 3rd, 2022

COMPASS compatible TCS encoder on modern hardware components

Peshkov Daniil

Laboratory “Industrial Systems for Streaming Data Processing”, SPbPU NTI Center

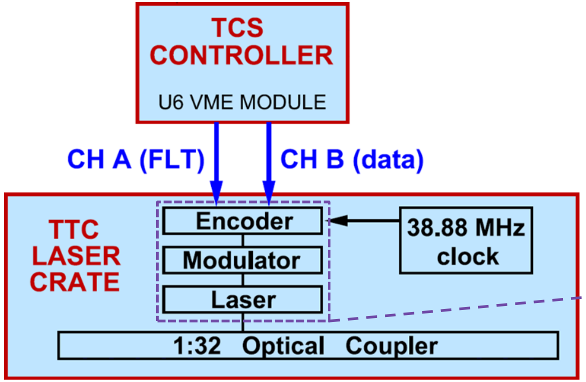
TCS (COMPASS) reengineering for DAQ-SPD

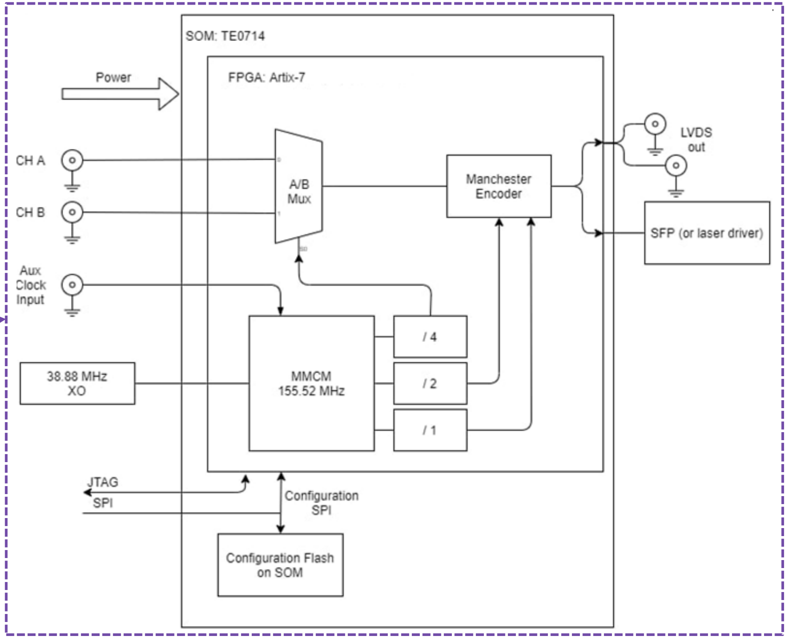


TRIGGER (TIMING) AND CONTROL SYSTEM – PILOT PROJECT

- Heart of the DAQ – orchestrates work of the whole system
- Pretty simple but crucial system component
- COMPASS TCS is not suitable for the triggerless DAQ-SPD system
- High demand for performance improvement in DAQ-SPD
- COMPASS TCS hardware is based on obsolete components
- Little to no technical support from the developers

TCS Encoder reengineering for DAQ-SPD



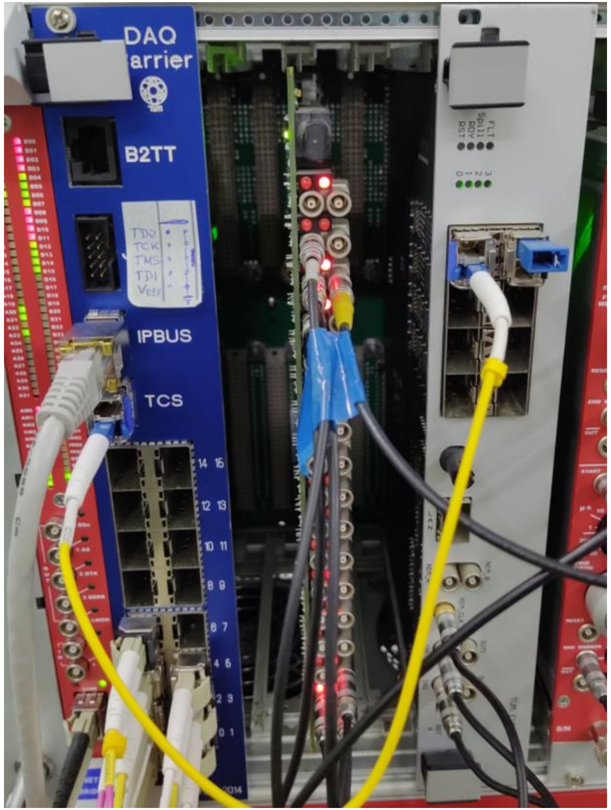


- Fully function-compatible with the original COMPASS TCS
- Xilinx Artix-7 FPGA-based hardware platform
- Rapid device development using Trenz TE0714 SoM
- Different form factor – no need of using VME for standalone device
- Planned implementation in a 19-inch rack unit with standard AC power supply – TCS does not require high-precision or exotic supply voltages
- Low-cost solution

TCS (COMPASS) reengineering for DAQ-SPD

ROADMAP: TCS FOR STRAW TRACKER

- **Schematic and PCB design – TCS Controller + Encoder**
- **TCS Encoder FPGA design**
- **TCS Encoder debugging and testing in the real straw tracker experiment environment**
- Full TCS FPGA design
- Full TCS debugging and testing in the real straw tracker experiment environmentC



ROADMAP: FURTHER STEPS

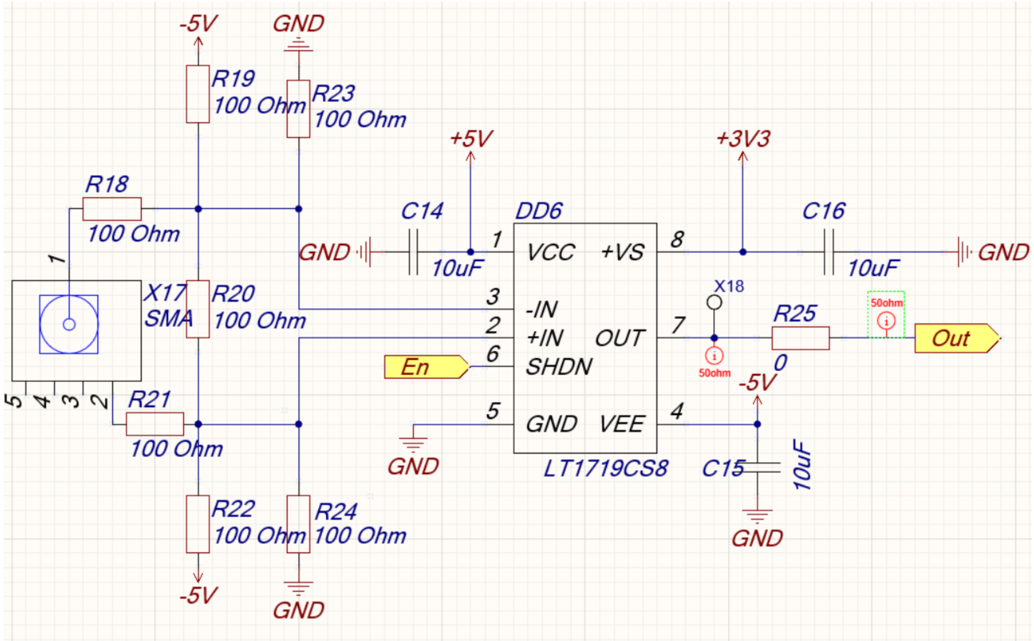
- TCS architecture redesign for DAQ-SPD: adding WR node
- New TCS development, debugging and testing
- Optimization of online processing tasks and DAQ

Hardware Platform

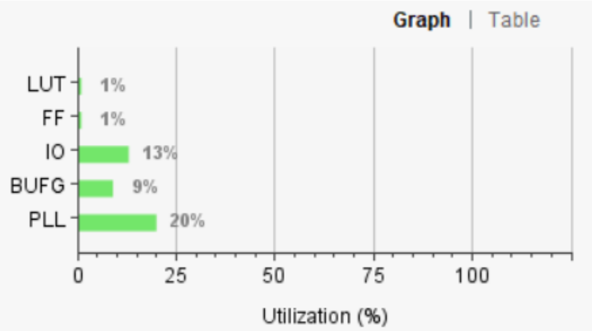
- 2 SFP Cages (tx for TCS receiver and IPBUS)
- 9 LEMO inputs (2 NECL, 7 NIM)
- 6 LEMO outputs (NIM)
- 5-12V DC power input

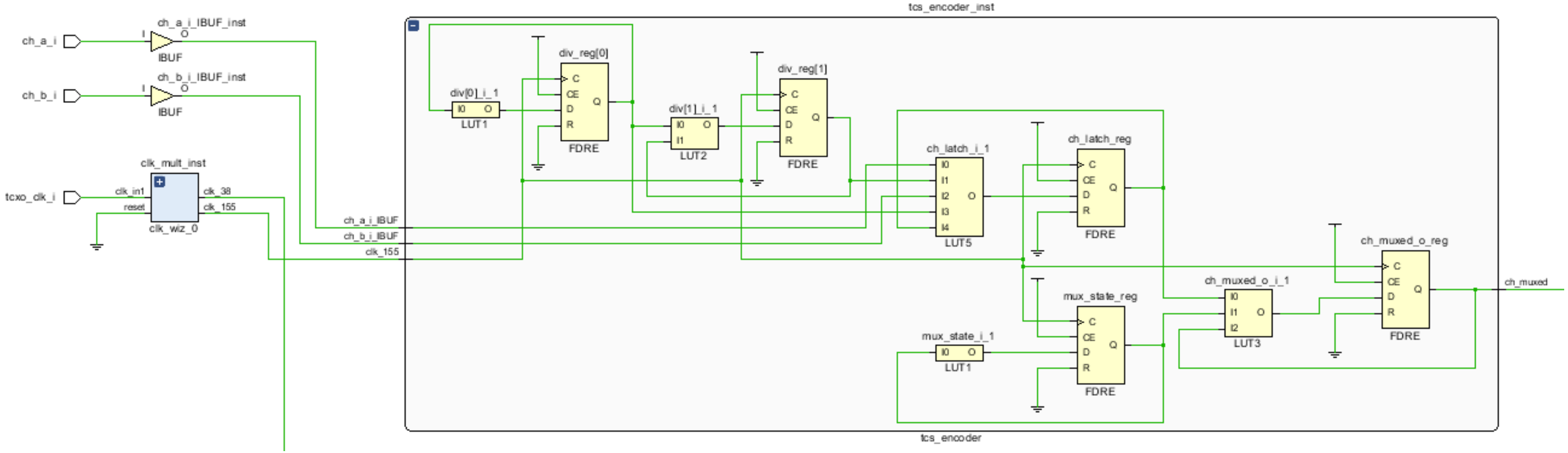
Physical level

- Configurable
- Less error prone



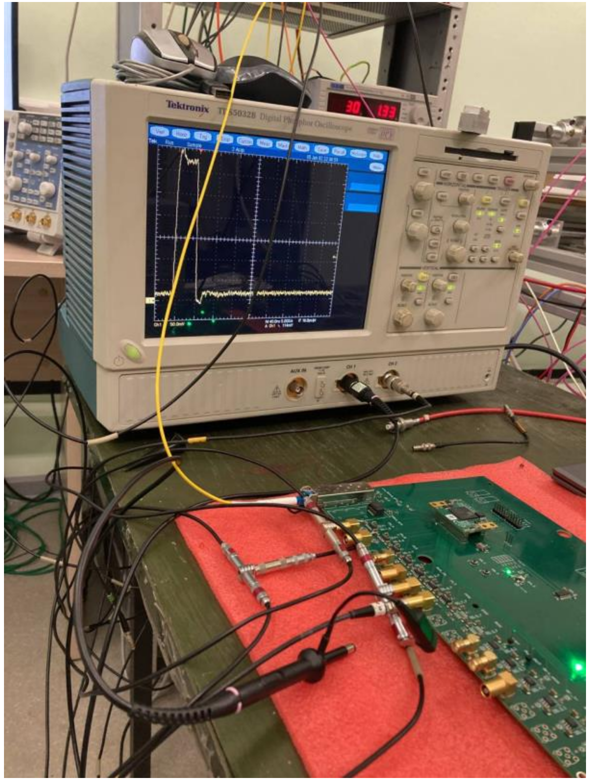
FPGA project





In-system testing (straw-tracker)

- First, tested our TCS encoder implementation in parallel with the original TCS encoder and its clock
- Achieved the same output signals to the same A and B channels from the TCS controller
- Removed the original TCS encoder from the system and switched it to our 38.88 MHz clock



Features and benefits

- Low cost: components and manufacturing < $200
- Better components availability
- Low-power
- Versatile

Further steps

- Implementation of TCS Controller along with TCS Encoder (if needed)
- Moving to TSS

Thank you for your attention

Contacts

Daniil Peshkov

Engineer

E-mail: daniil.peshkov@spbpu.com