Development of the SPD NINO prototype ASIC

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for ASIC Lab of NRNU MEPHI

DAQ & front-end session at SPD collaboration meeting, 03/10/22

Outline

- Introduction
- ASIC structure
- Channel structure
- Building blocks
  - Preamplifier
  - Stretcher
  - Impedance adjustment
- Summary and outlooks

Introduction

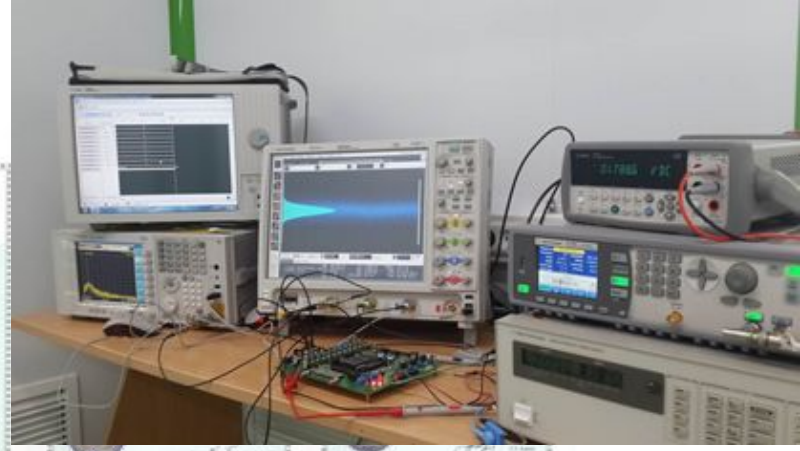
we are from ASIC Lab at NRNU MEPhI (https://asic.mephi.ru):

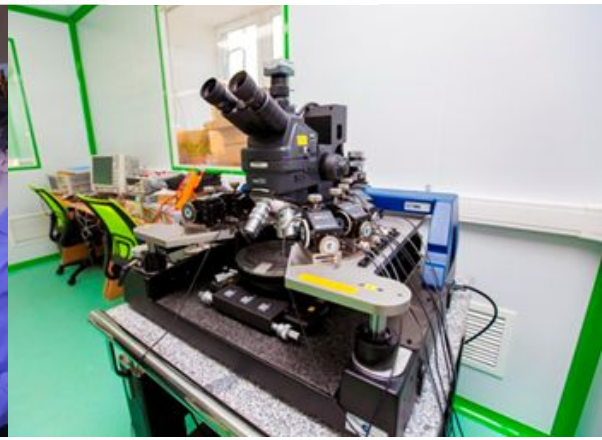
– server cluster for computer-aided design an advanced measuring (e.g. ISO7 clean room) infrastructure

– more than 30 tape-outs mostly for experimental physics, in different CMOS (BiCMOS) processes, 350-28 nm nodes

– manpower includes teaching staff of Electronics and Microelectronics departments + young graduates + PhD and master students

– since 2009, 8 methodological All-Russia and International workshops on CAD have been organized by our lab at MEPhI (each 100-250 attendees), including training courses, finalizing by Cadence certificates





Aims & schedule

Main aims:

– Approbation of ASIC start-to-finish design route, relevant to 180 nm CMOS process HCMOS8D at Mikron fab in Zelengrad

– Design of building functional blocks for a front-end electronics of SPD

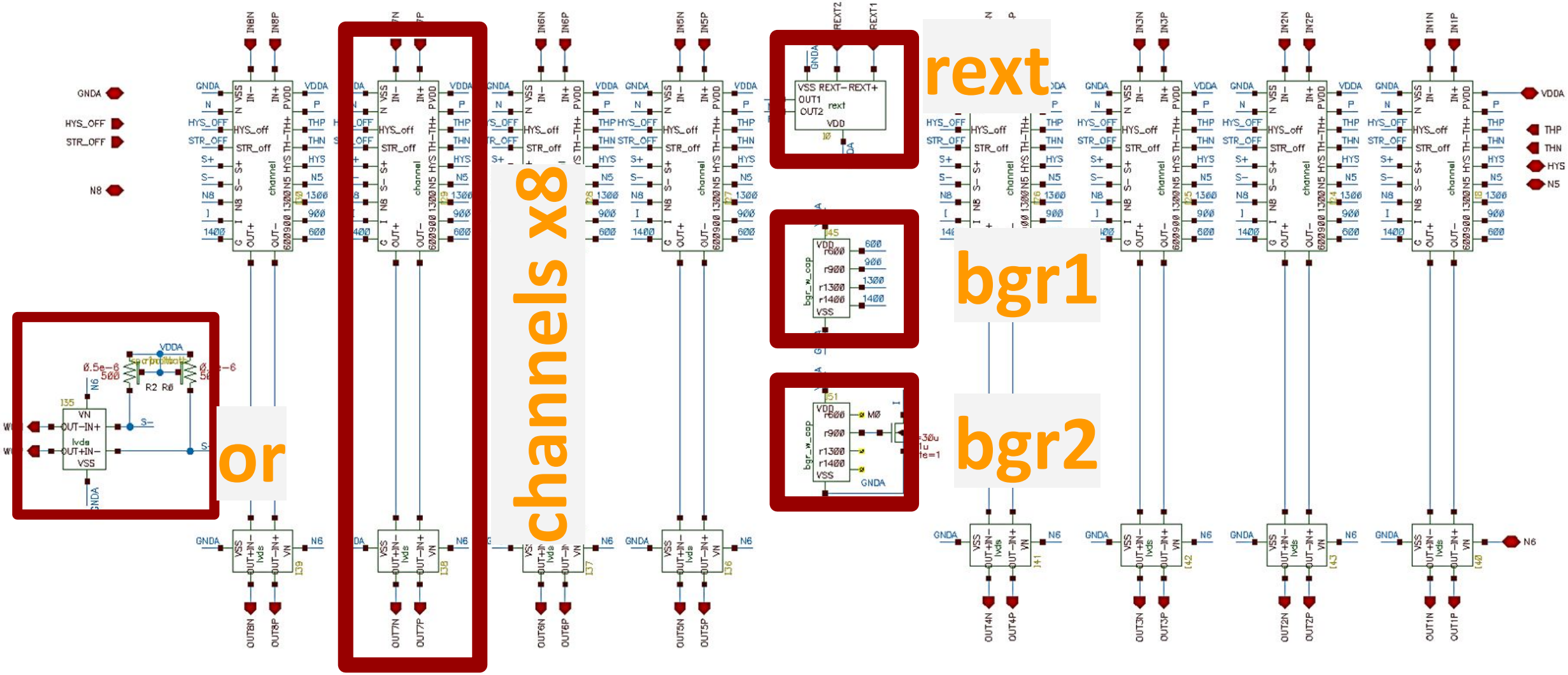
ASIC design stage. Very short working time frame – 3 months only (late May to late August 2022)

- Literature analysis (05.2022)
- Structural scheme and behavioral simulation (05.2022)
- Preliminary chip planning (05.2022-06.2022)
- Building blocks schematics design & integration (05.2022-07.2022)
- Block layout design (07.2022 - 08.2022)
- Design rules verification (DRC, LVS, ERC, PEX) (07.2022 - 08.2022)
- ASIC layout design (08.2022)
- Deadline for GDSII submission to the MPW (25.08.2022)
- Chip manual preparation (up to 30.11.2022)

Next (board) stage:

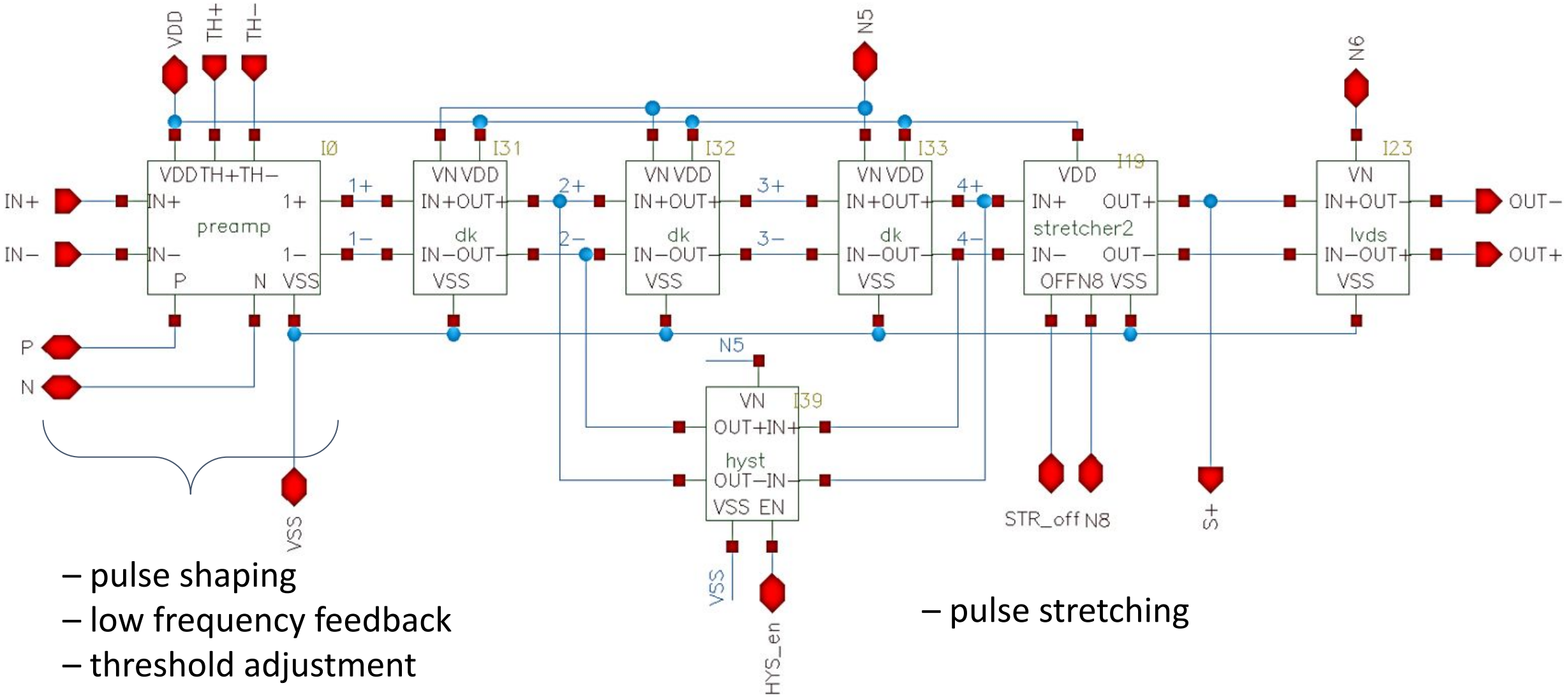
- Design of lab test bench and technique (~03.2023)
- Lab test PCB design and manufacturing (~06.2023)
- Receiving of fabricated samples (~09.2023)
- Chip experimental samples` testing (~10.2023)

ASIC structure



The reference (functional analog) for the design is NINO ASIC (NIMA, Volume 533, Issues 1–2, 2004, pp. 183-187)

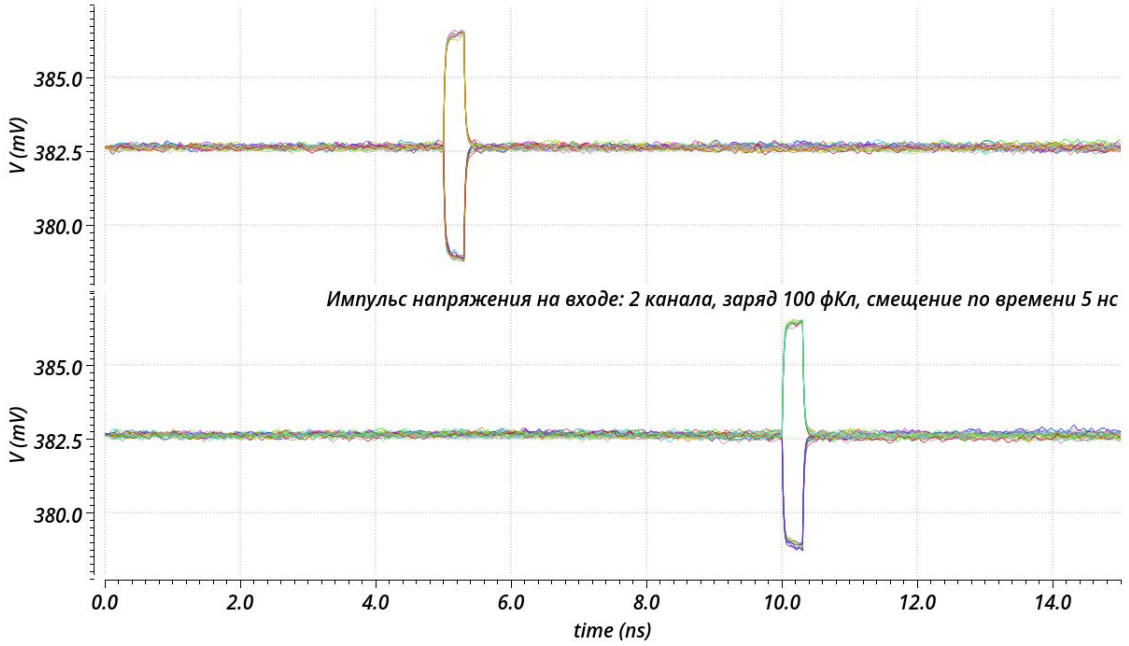
Channel structure

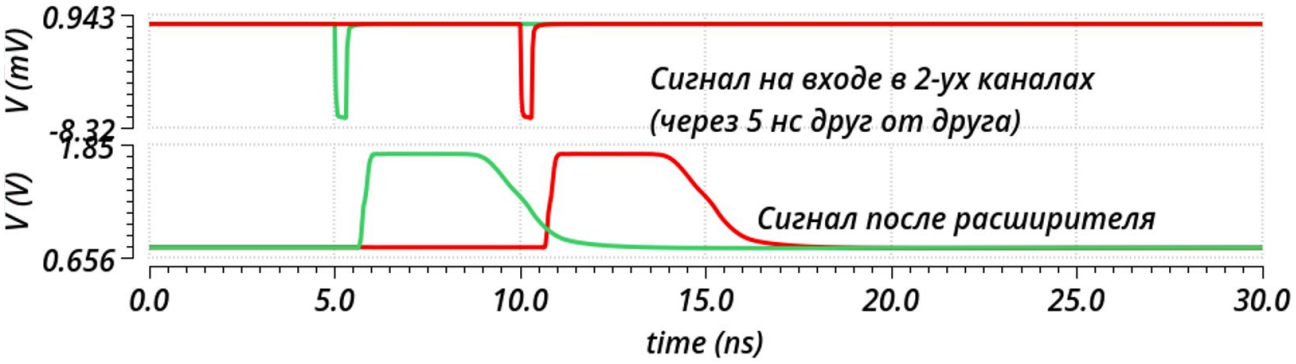


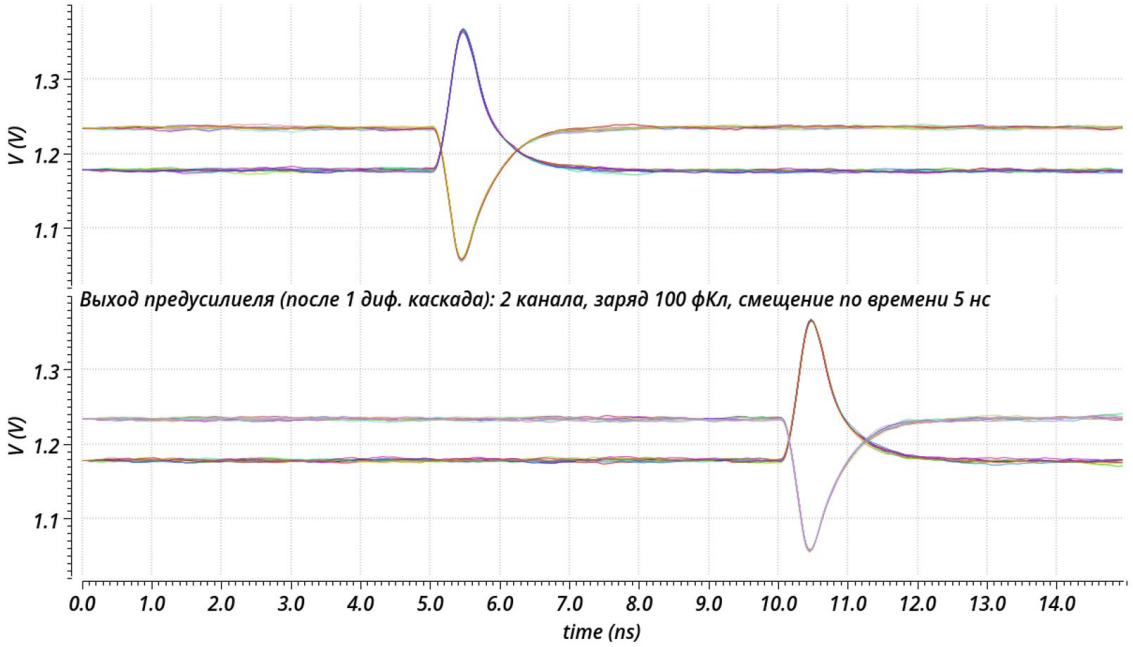
– pulse shaping
– low frequency feedback
– threshold adjustment

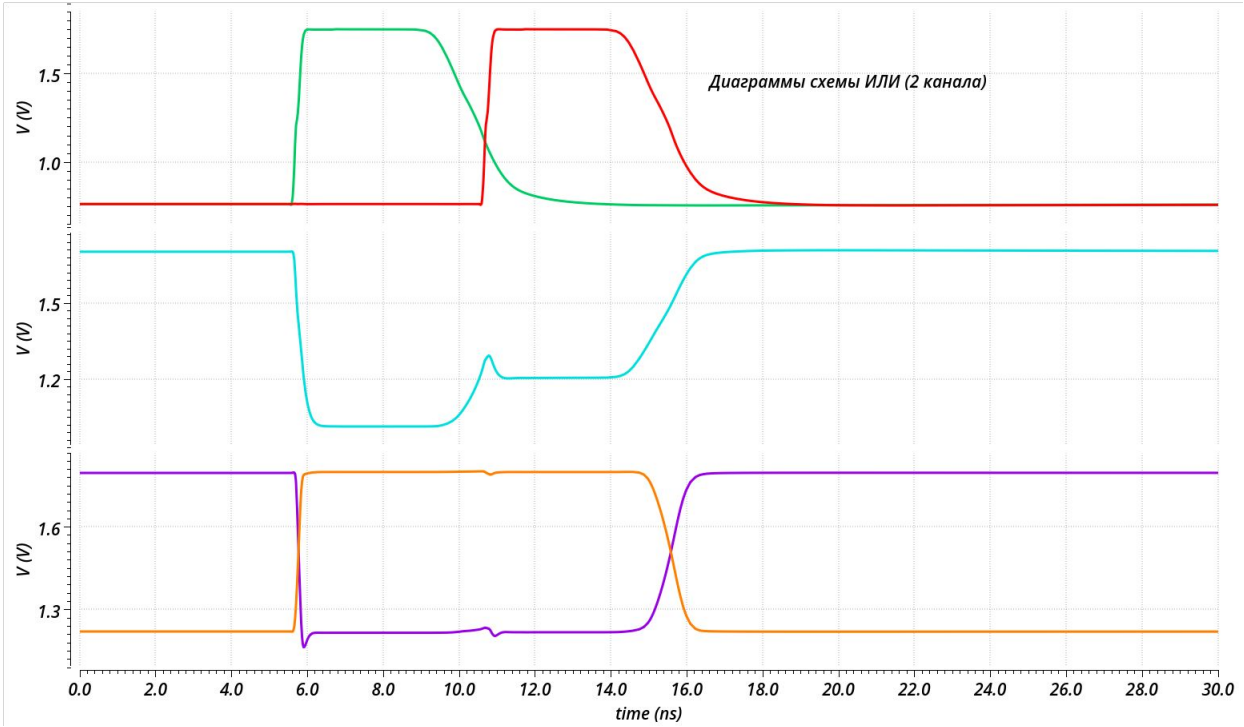
– pulse stretching

Typical time diagrams

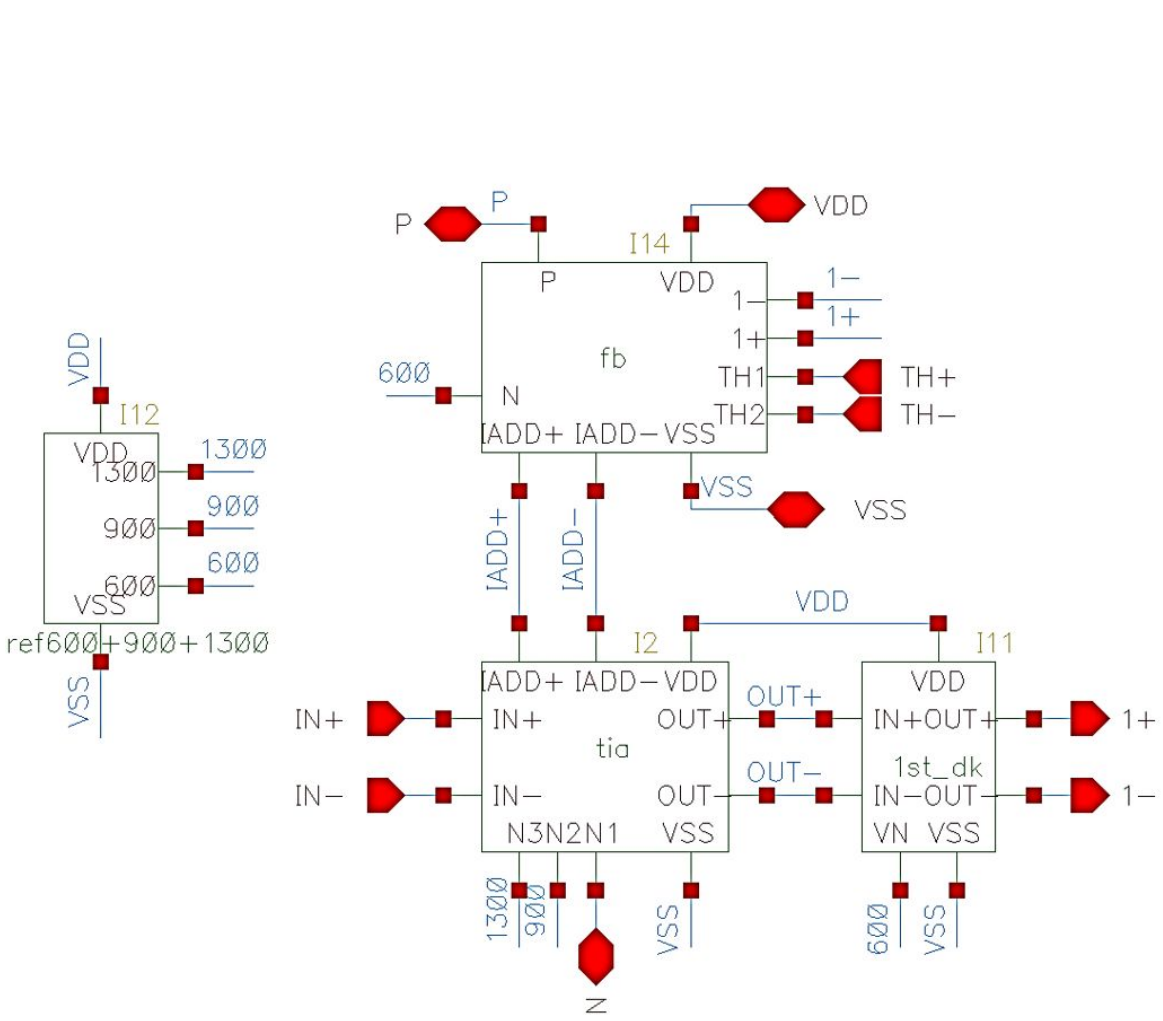


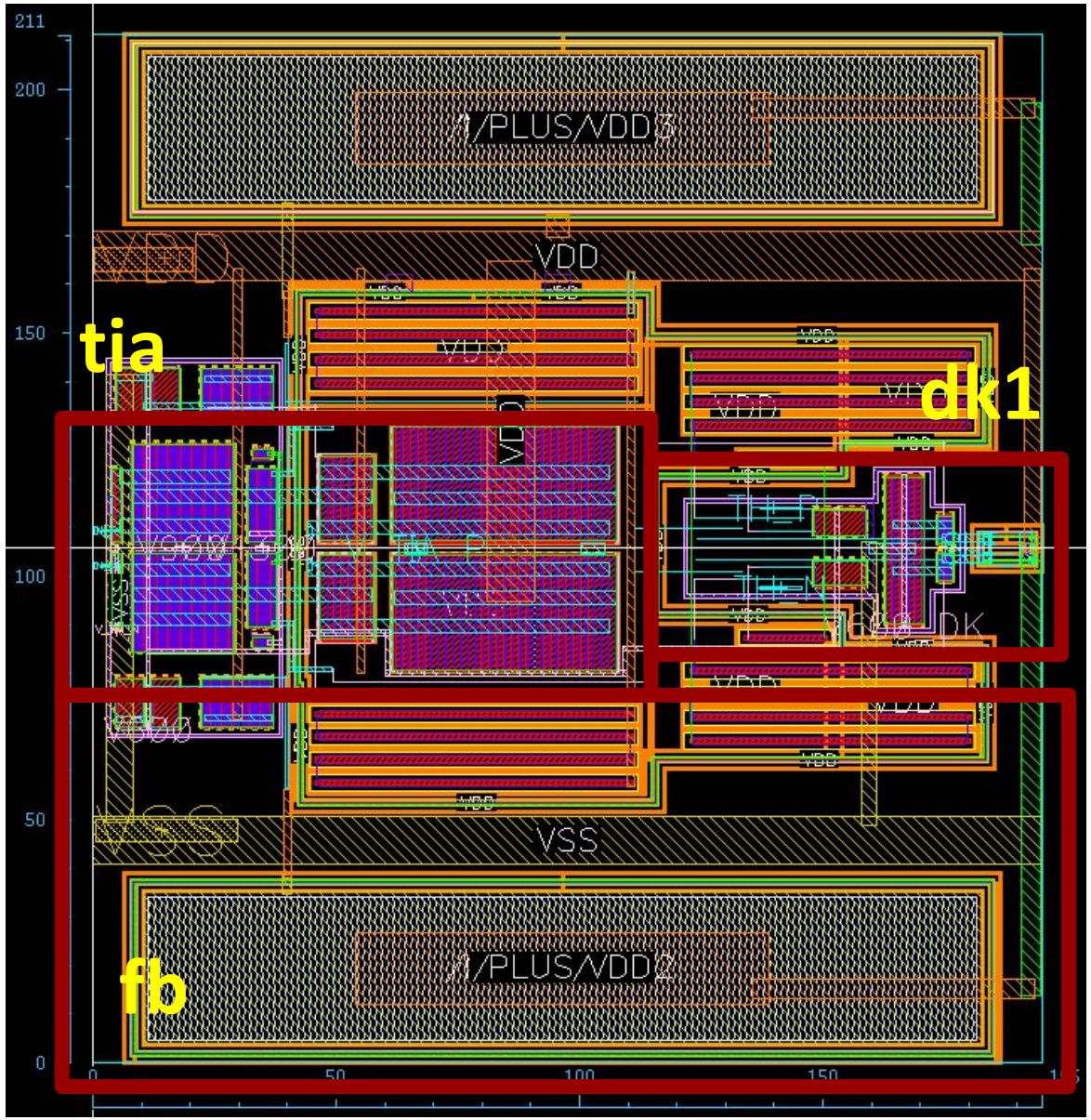






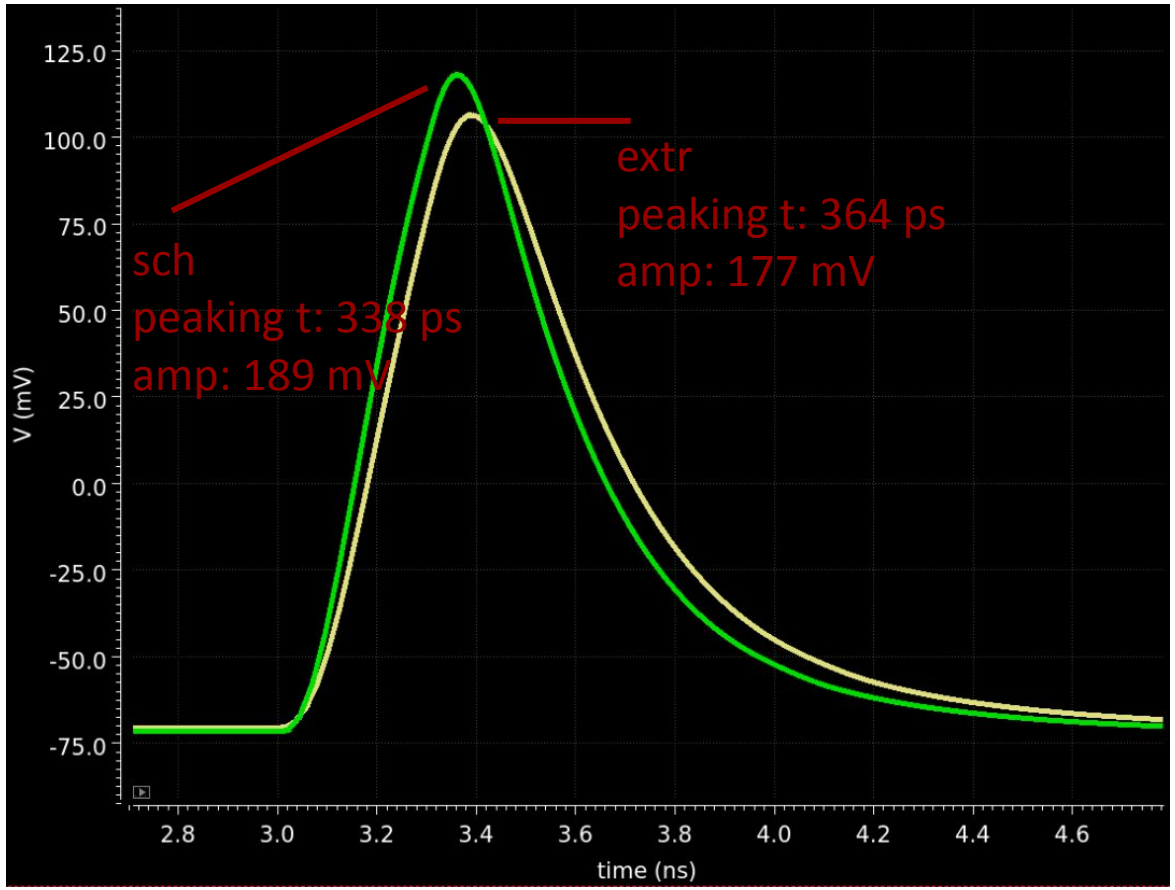
Preamplifier (1): Structure and layout





Preamplifier (2): Key parameters

Schematic and extraction pulses, with peaking times



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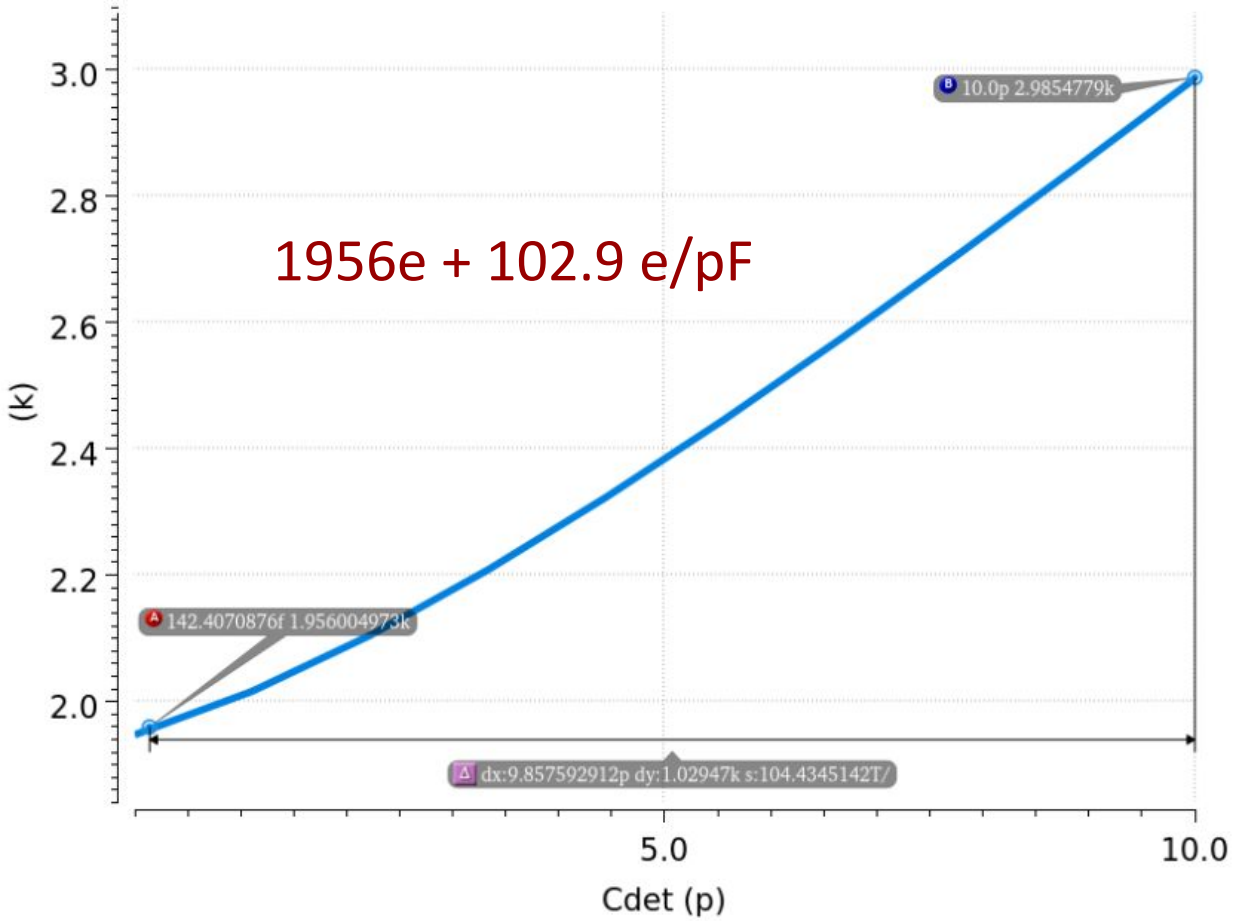
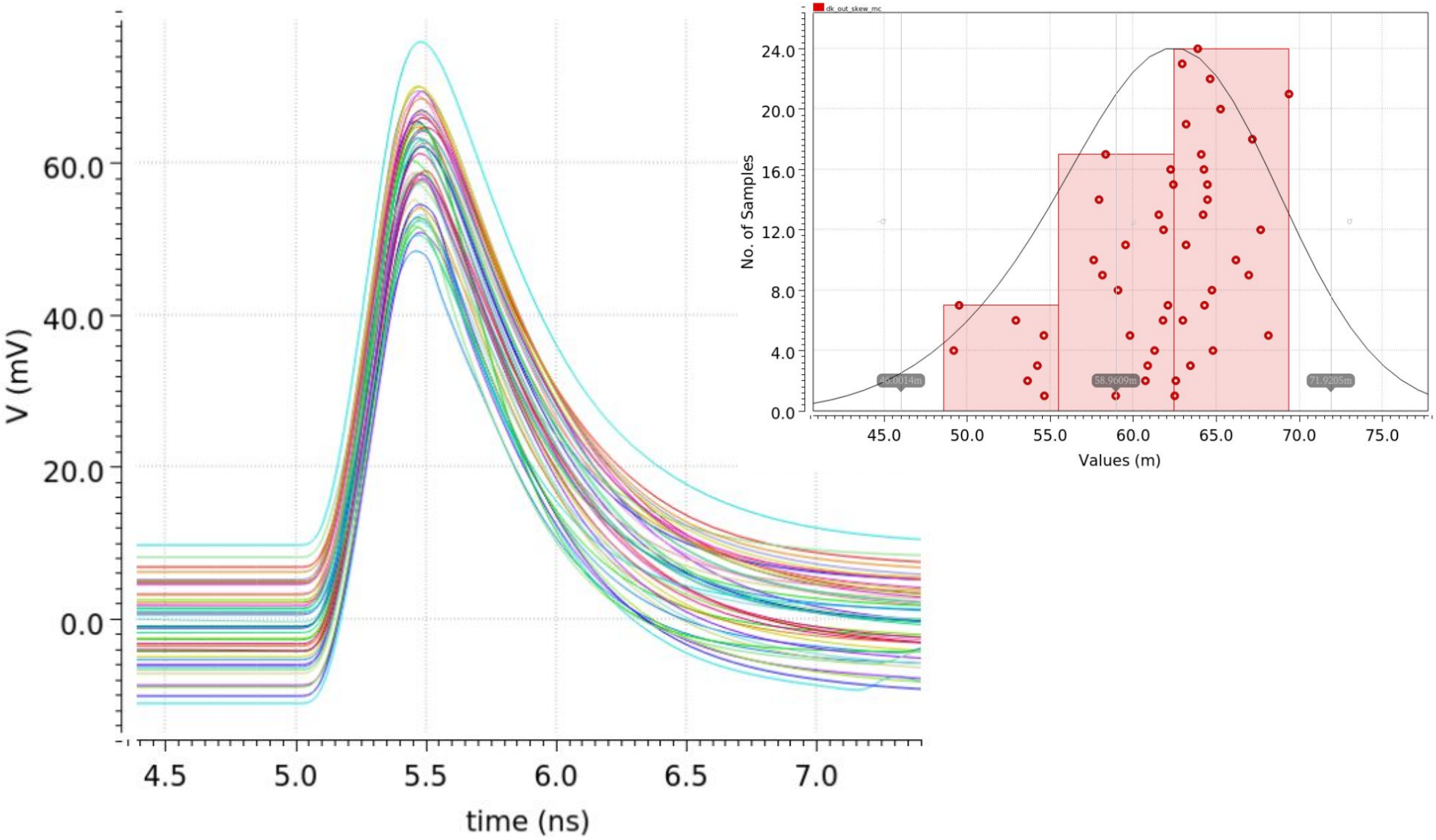
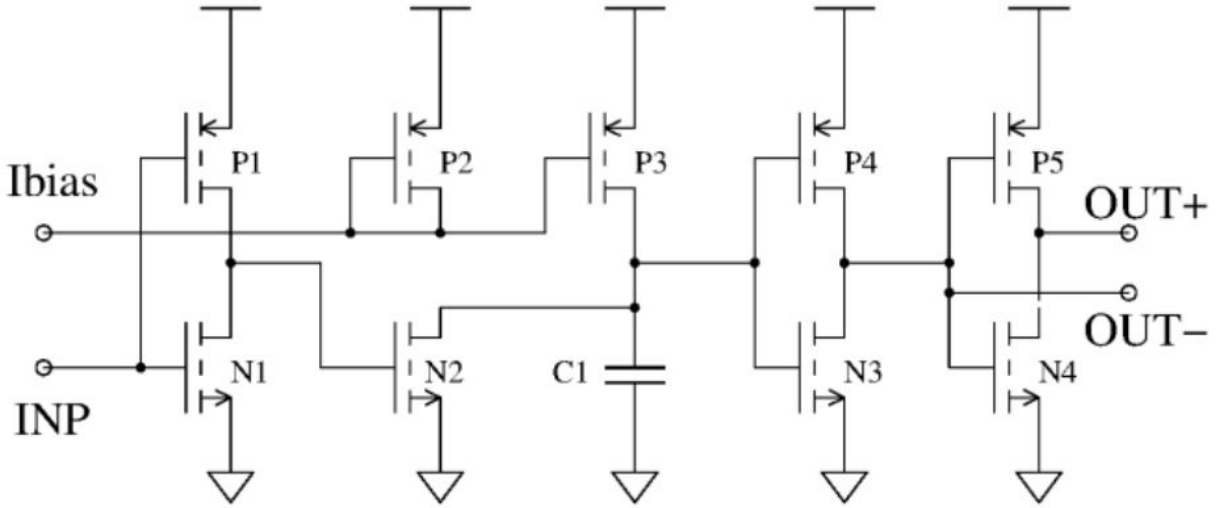
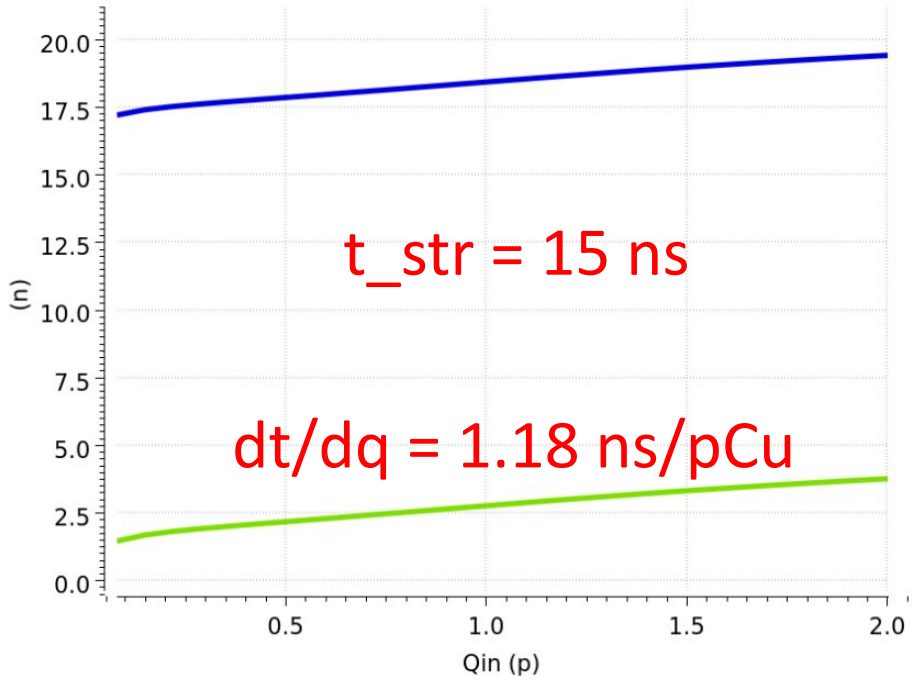


Preamplifier (3): Skew of amplification factor

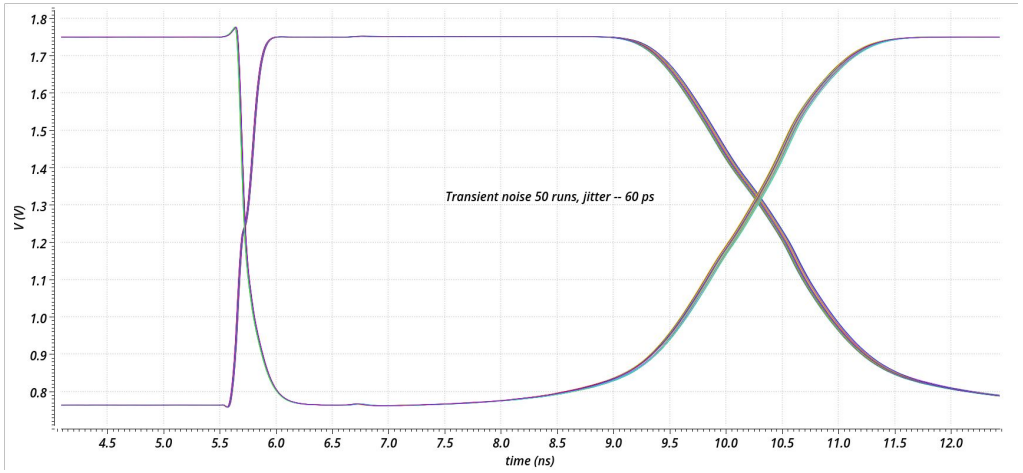


Stretcher

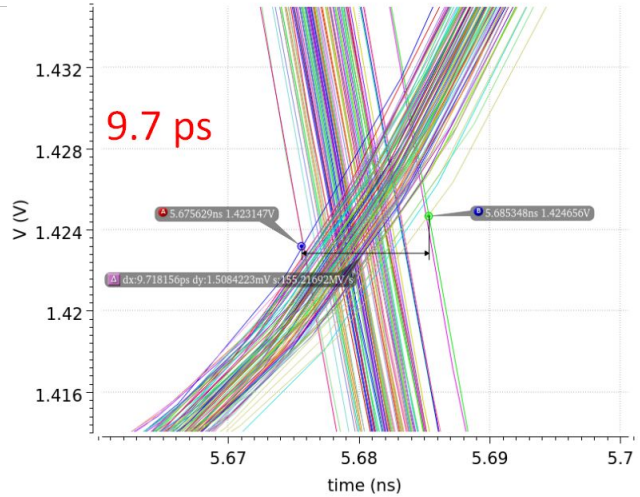




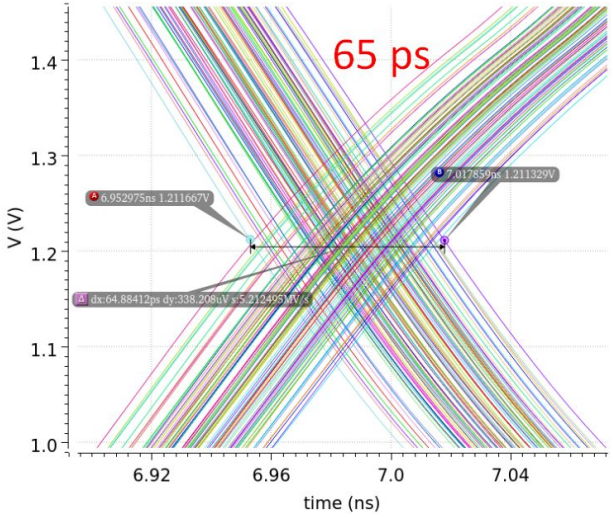
Differential version of the stretcher has been adapted from PADI ASIC stretch cell (IEEE Transaction on NS, April 2021, PP(99):1-1)



Output pulse shape

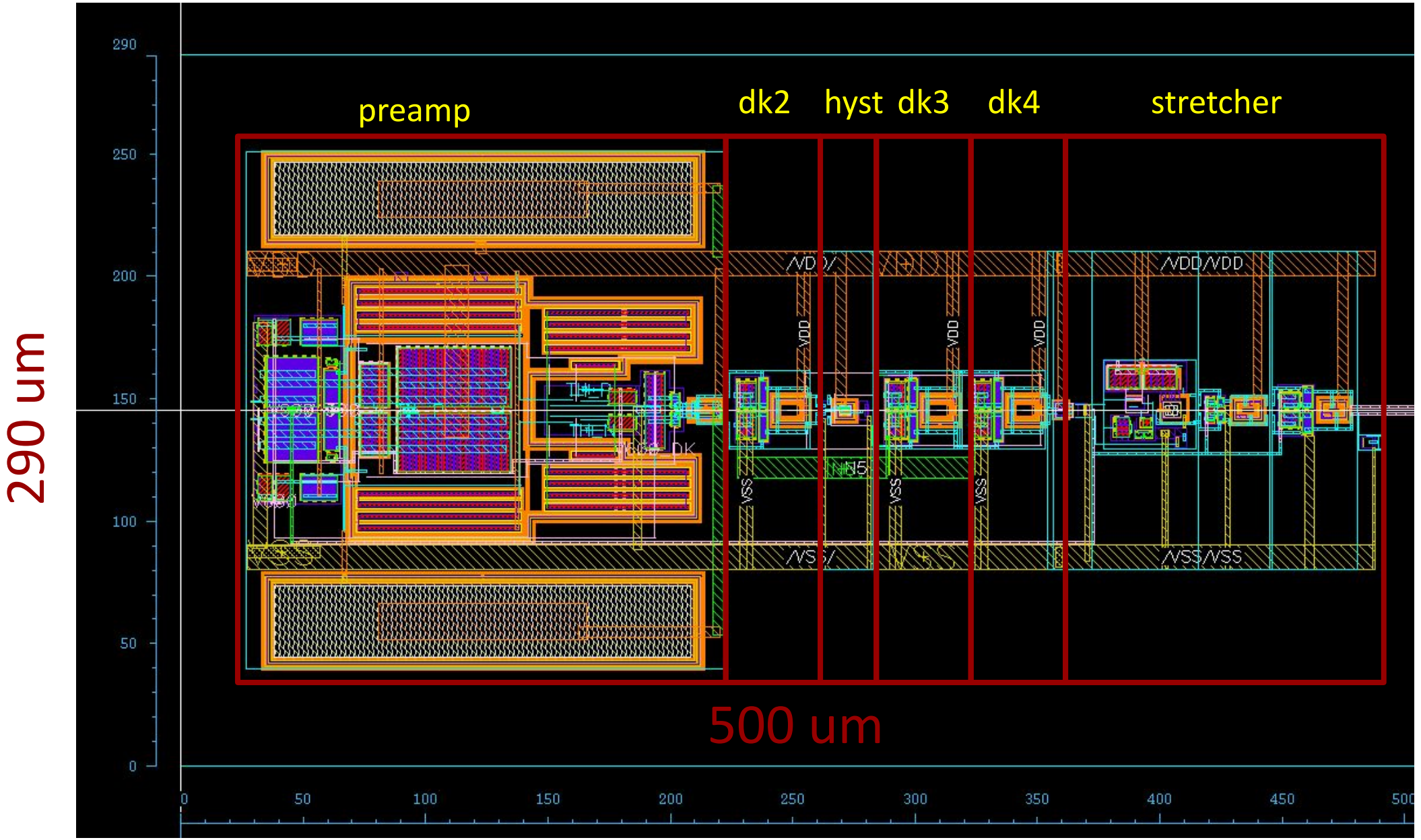


Rising edge

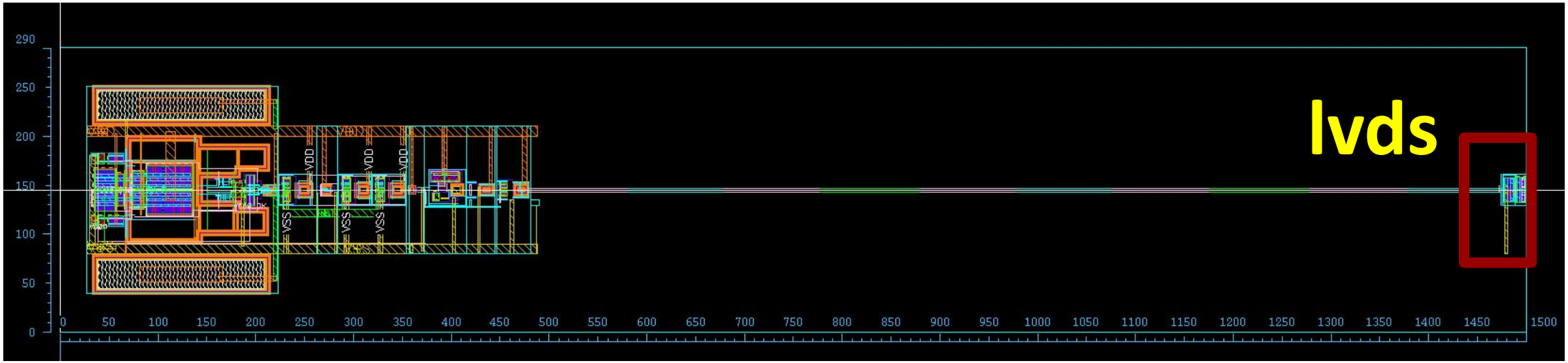


Falling edge

Channel layout (1)

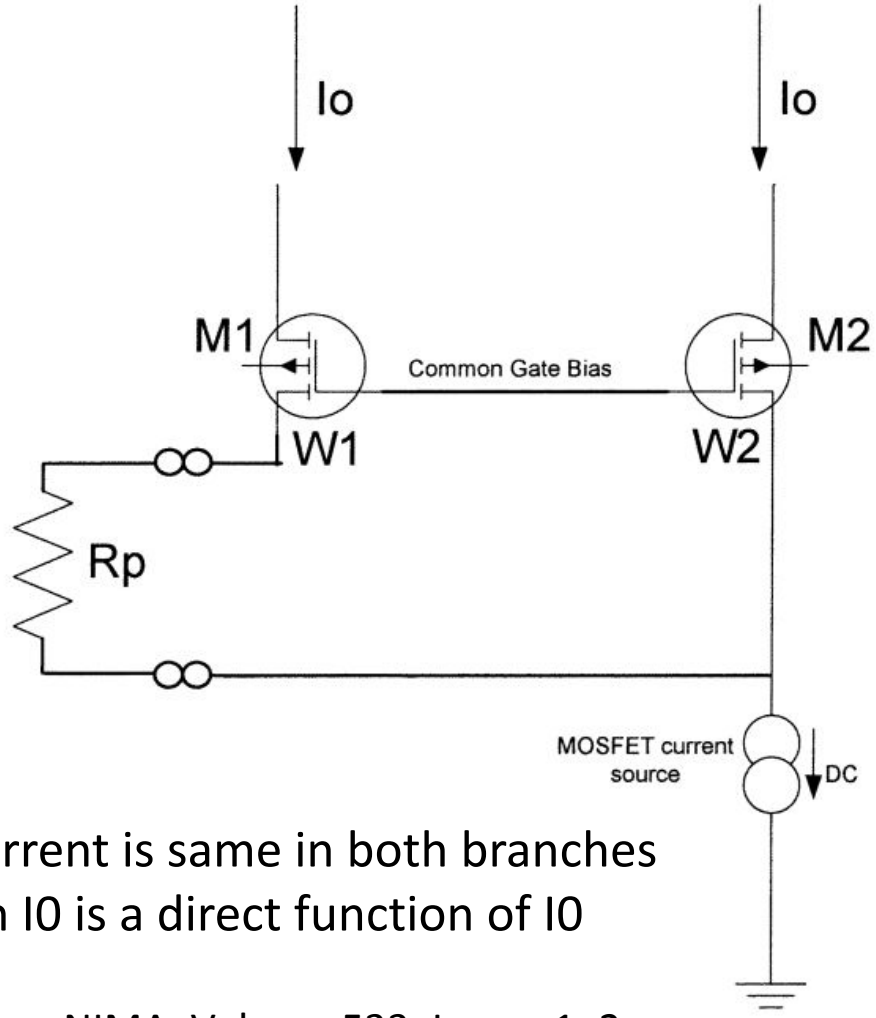


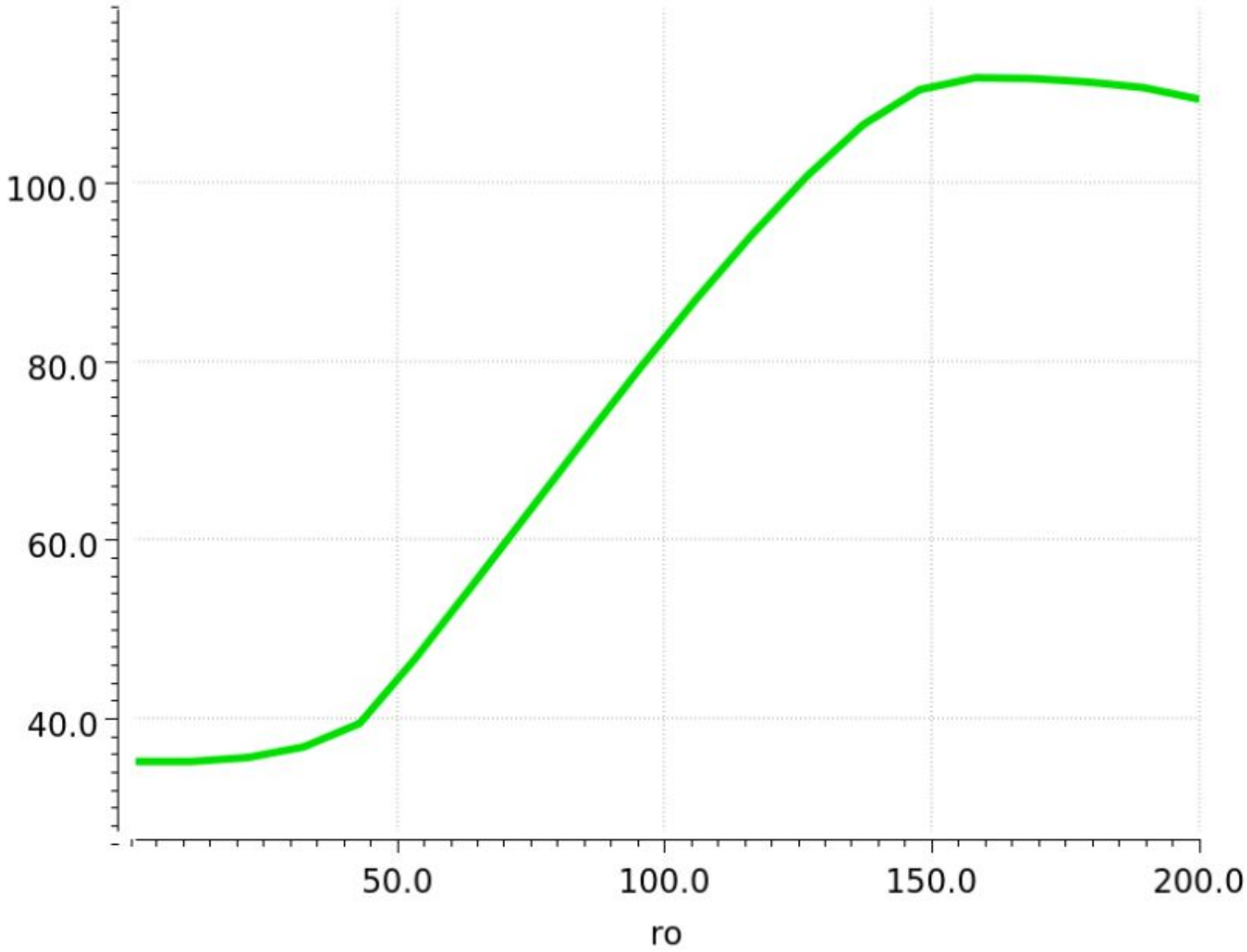
Channel layout (2)



Differential input impedance adjustment block

Rext block adjusts input impedance for all channels at once

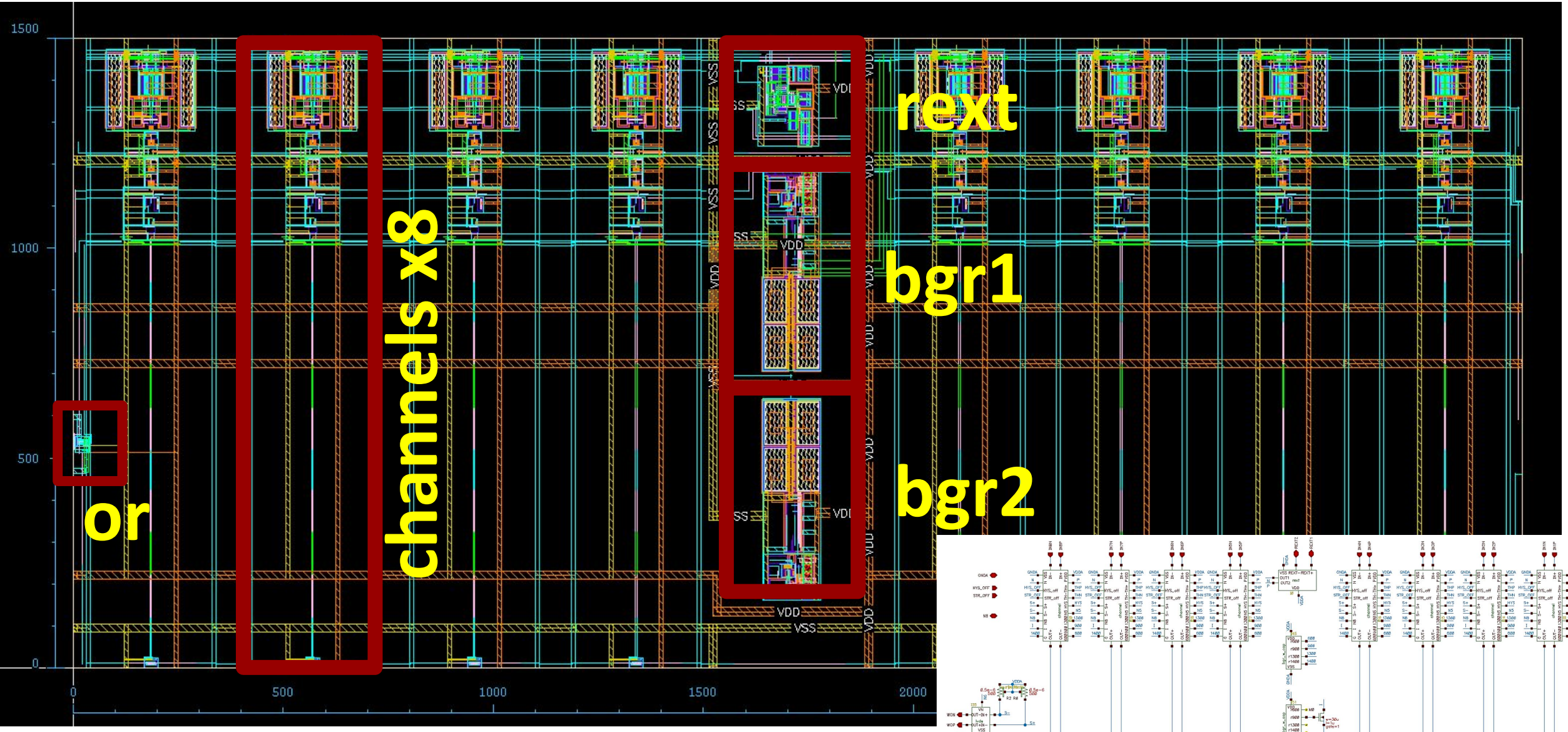




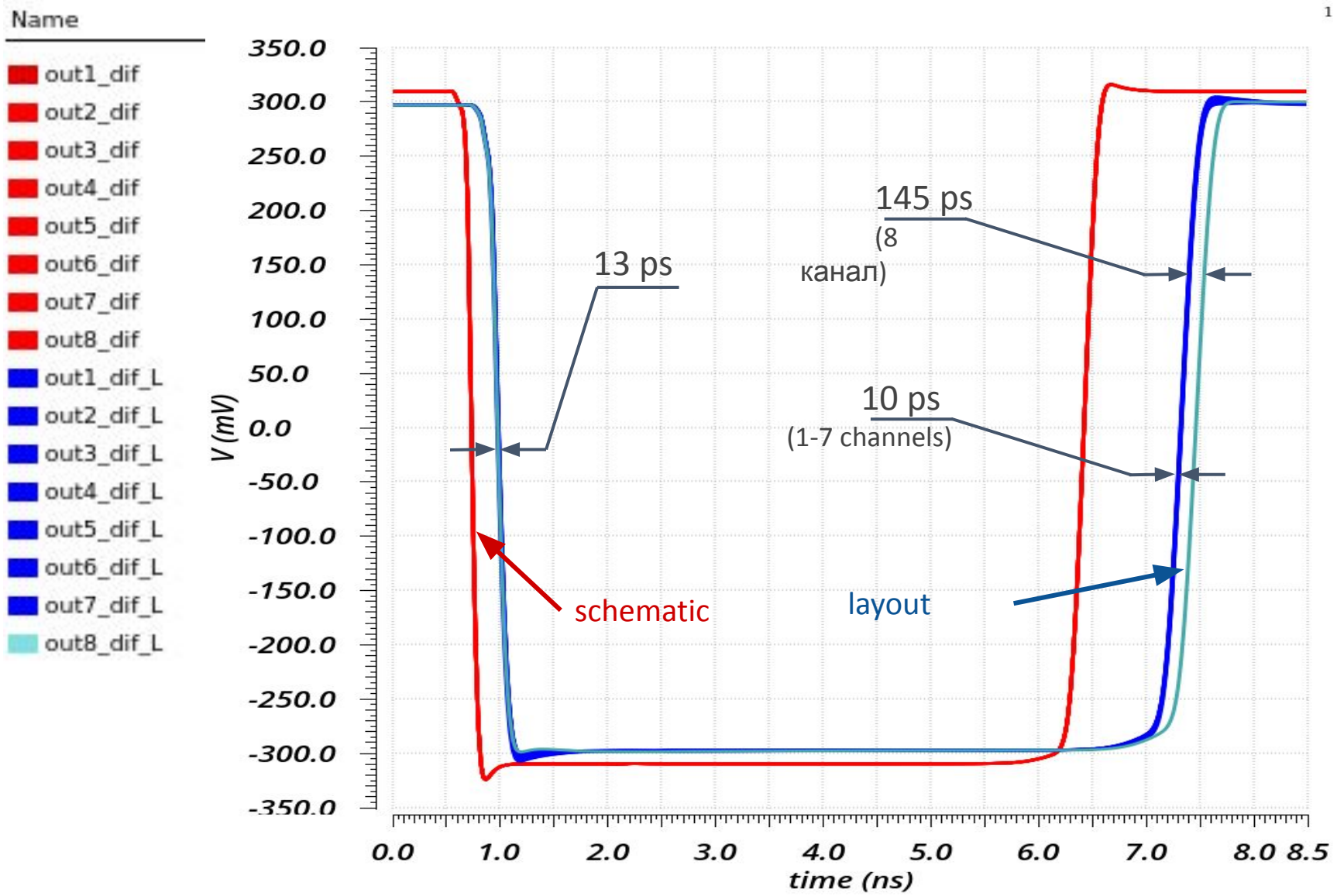
If current is same in both branches then I0 is a direct function of I0

NIMA, Volume 533, Issues 1–2, 2004, pp. 183-187

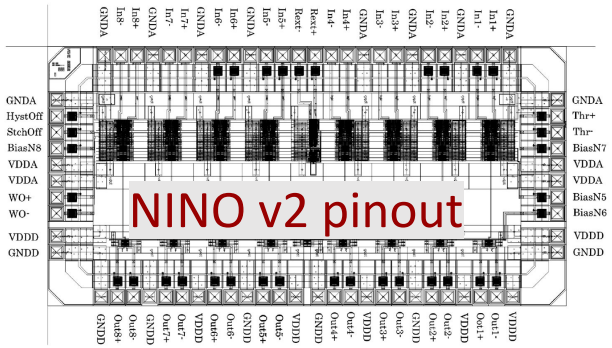
Prototype ASIC Layout



Schematic vs extraction of channels’ outputs



Top-level ASIC layout



The pinout of the chip is fully consistent with the NINO ver.2 chip

Basic parameters:

Layout size: 2 x 4 mm2 (10 µm clearance for scribe line);

HCMOS8D 180 nm technology;

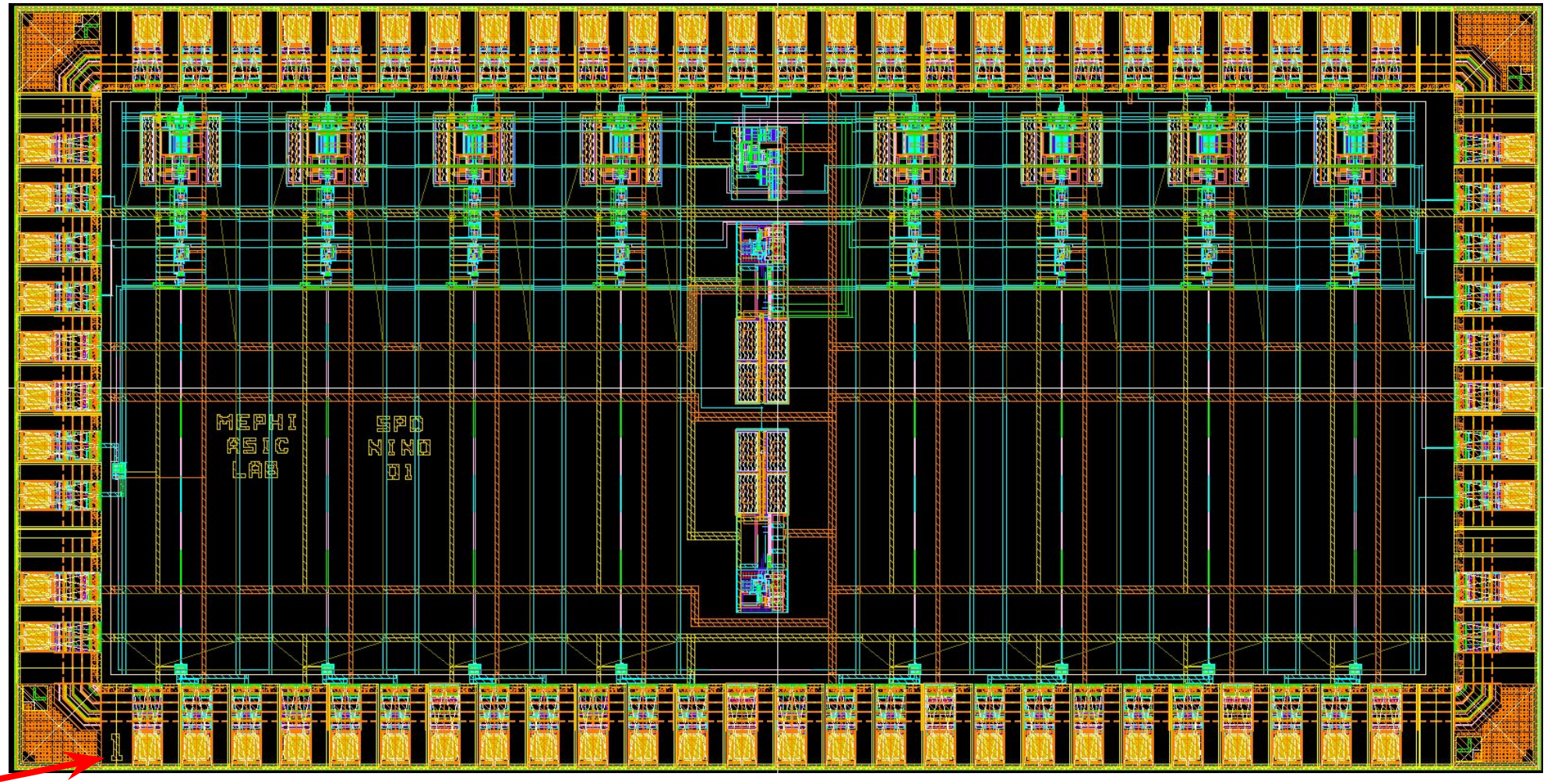
Area without pads: 1549 x 3549 µm2;

Pad spacing is 130 µm;

Pad contact area size - 80 x 75 µm;

Channel area - 1500 x 290 µm;

Channel spacing - 75 µm.



1st PAD

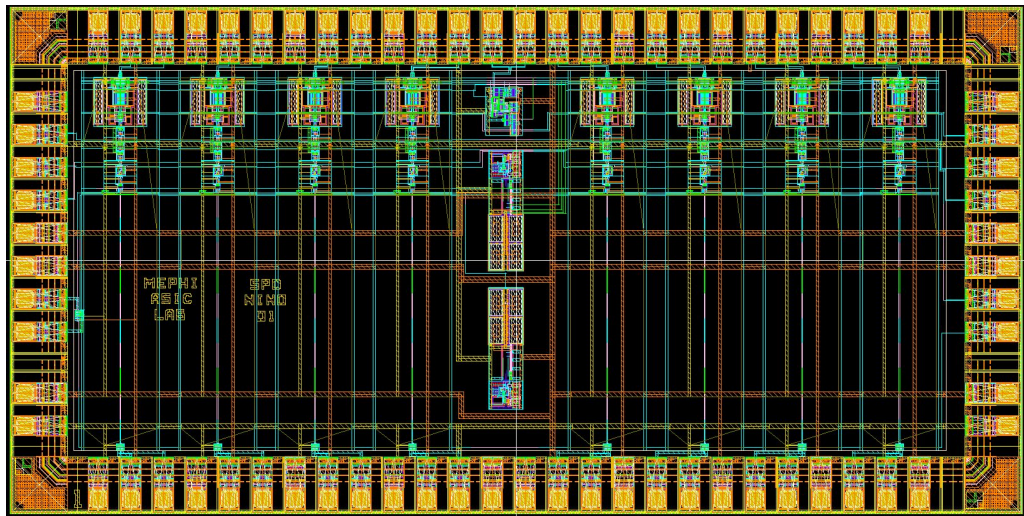
Conclusion

– Development of front-end chip for an SPD with a NINO-chip architecture and the corresponding design route based on 180 nm CMOS process PDK of the Mikron fab have been studied

– Design of all necessary building functional blocks for the FEE of NINO type has been made

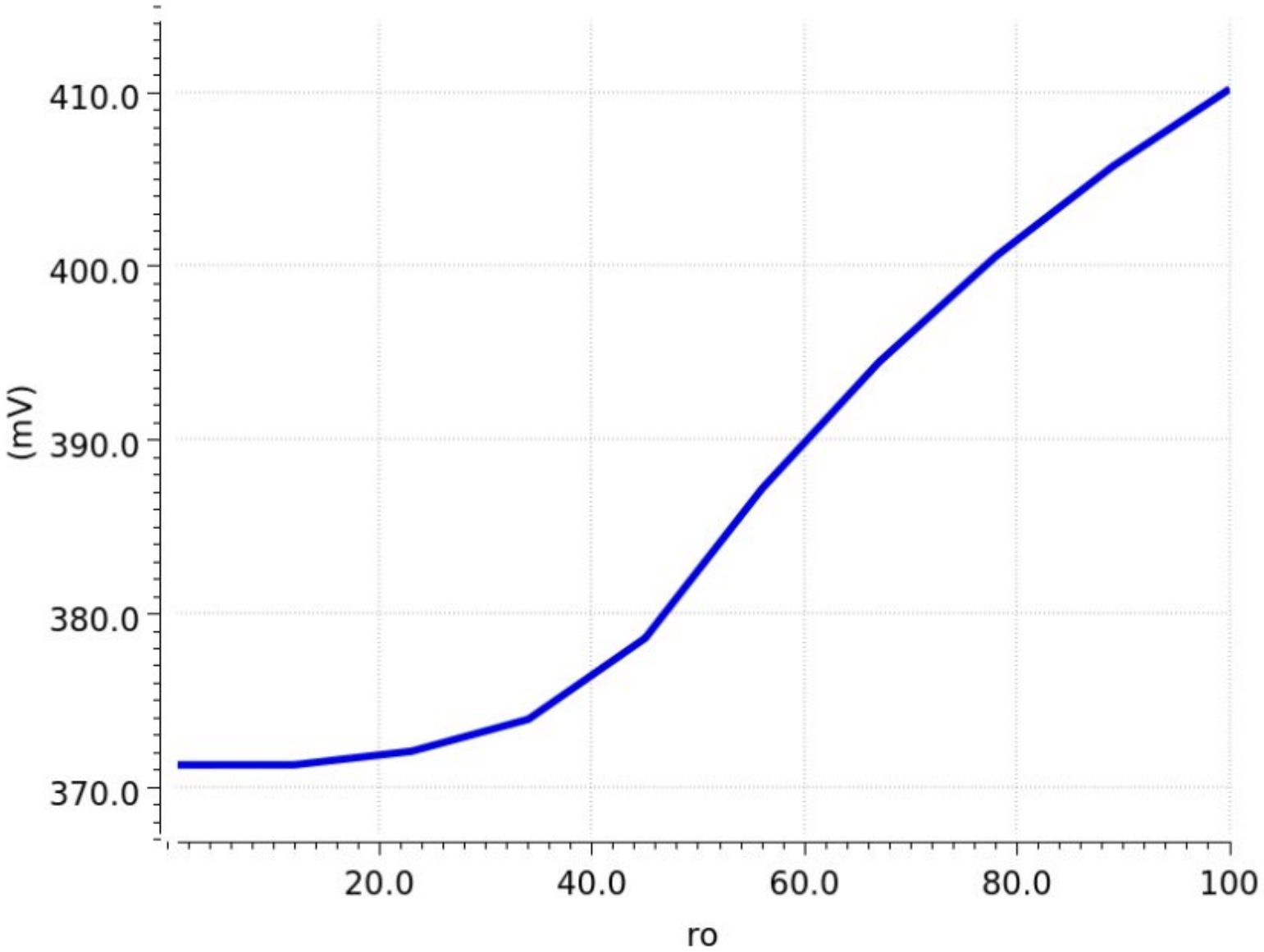
– GDSII file was submitted to the MPW service of Mikron on 25.08.22

– After fabrication in a year lab tests are foreseen

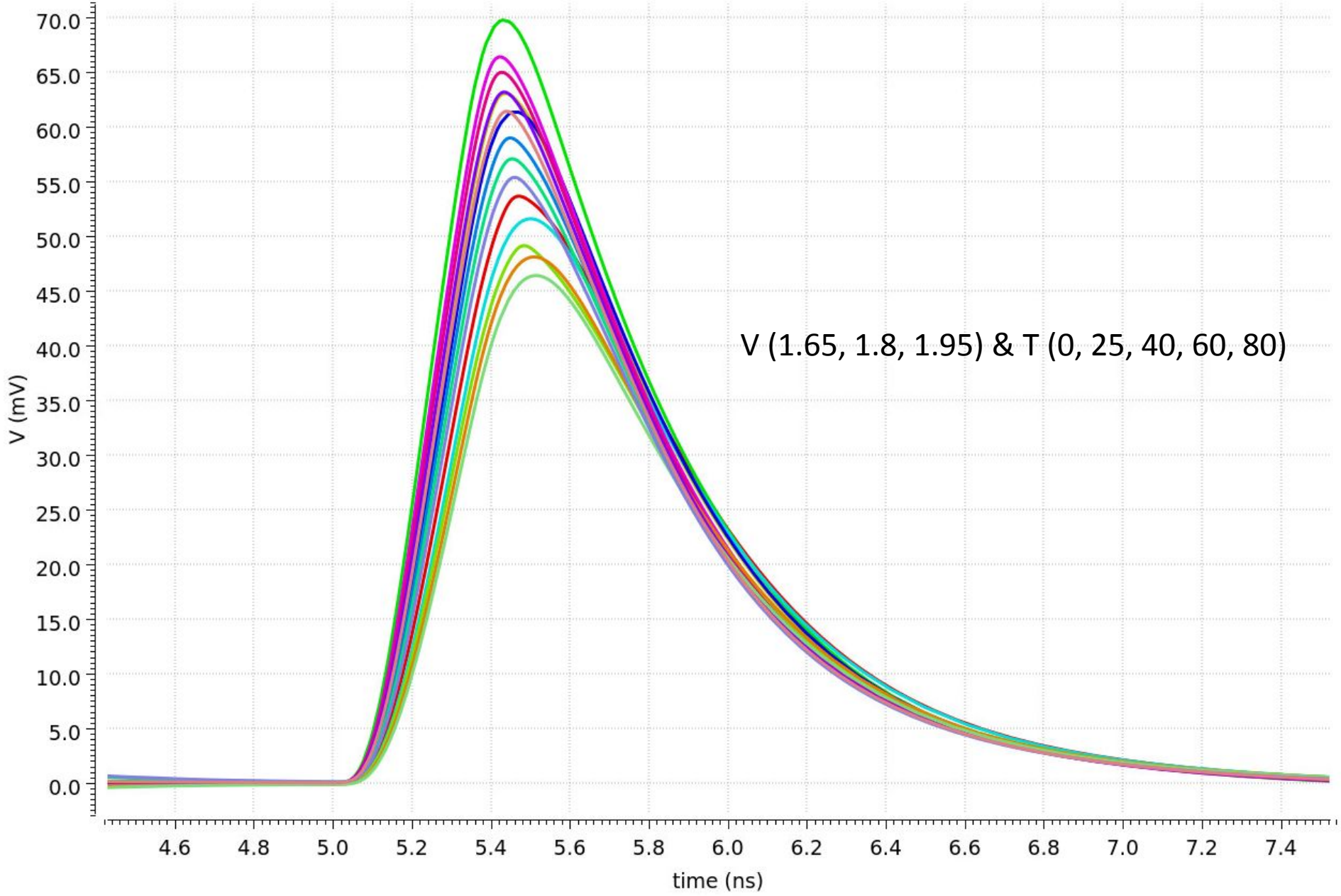


Back up slides

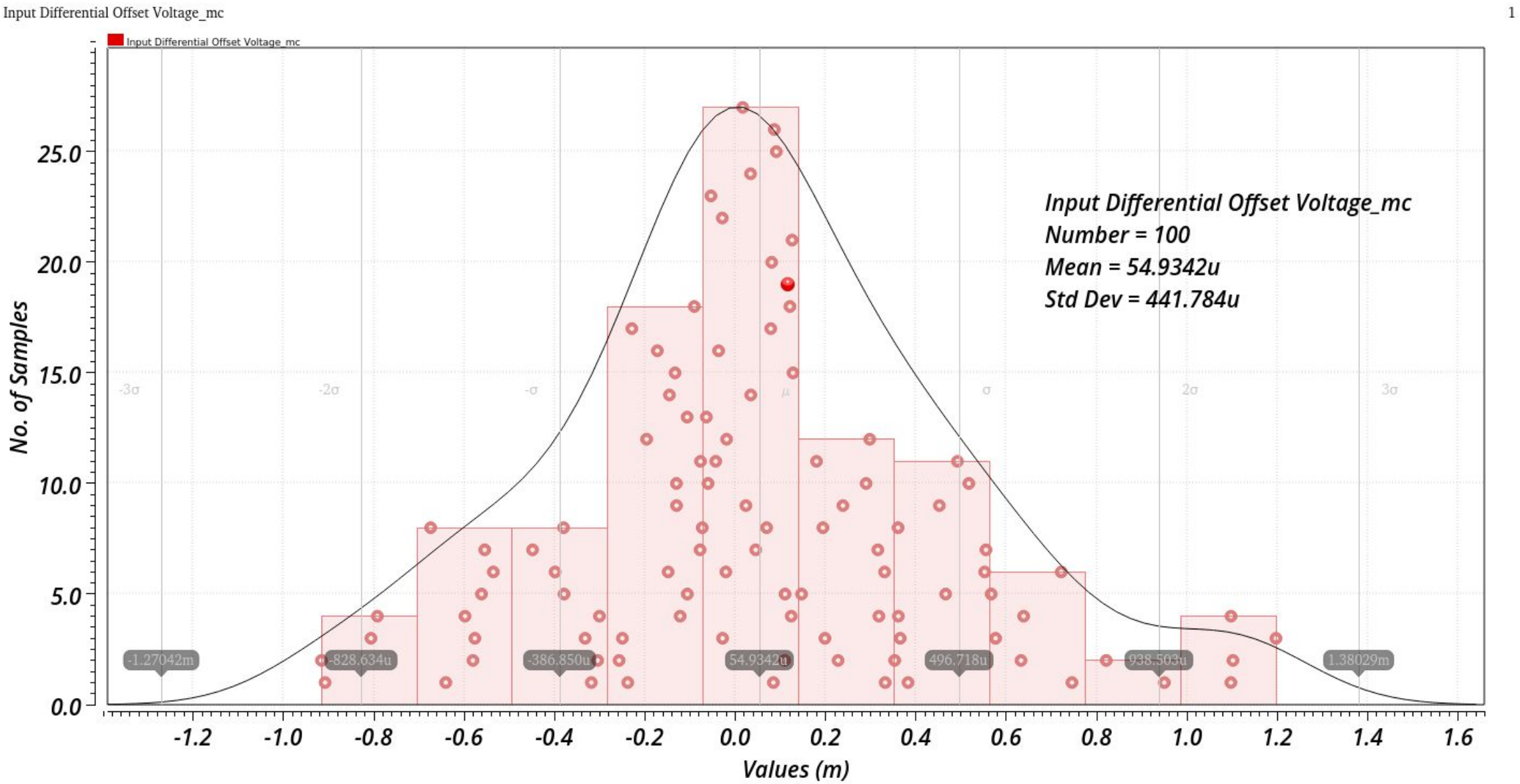
Режимный потенциал на



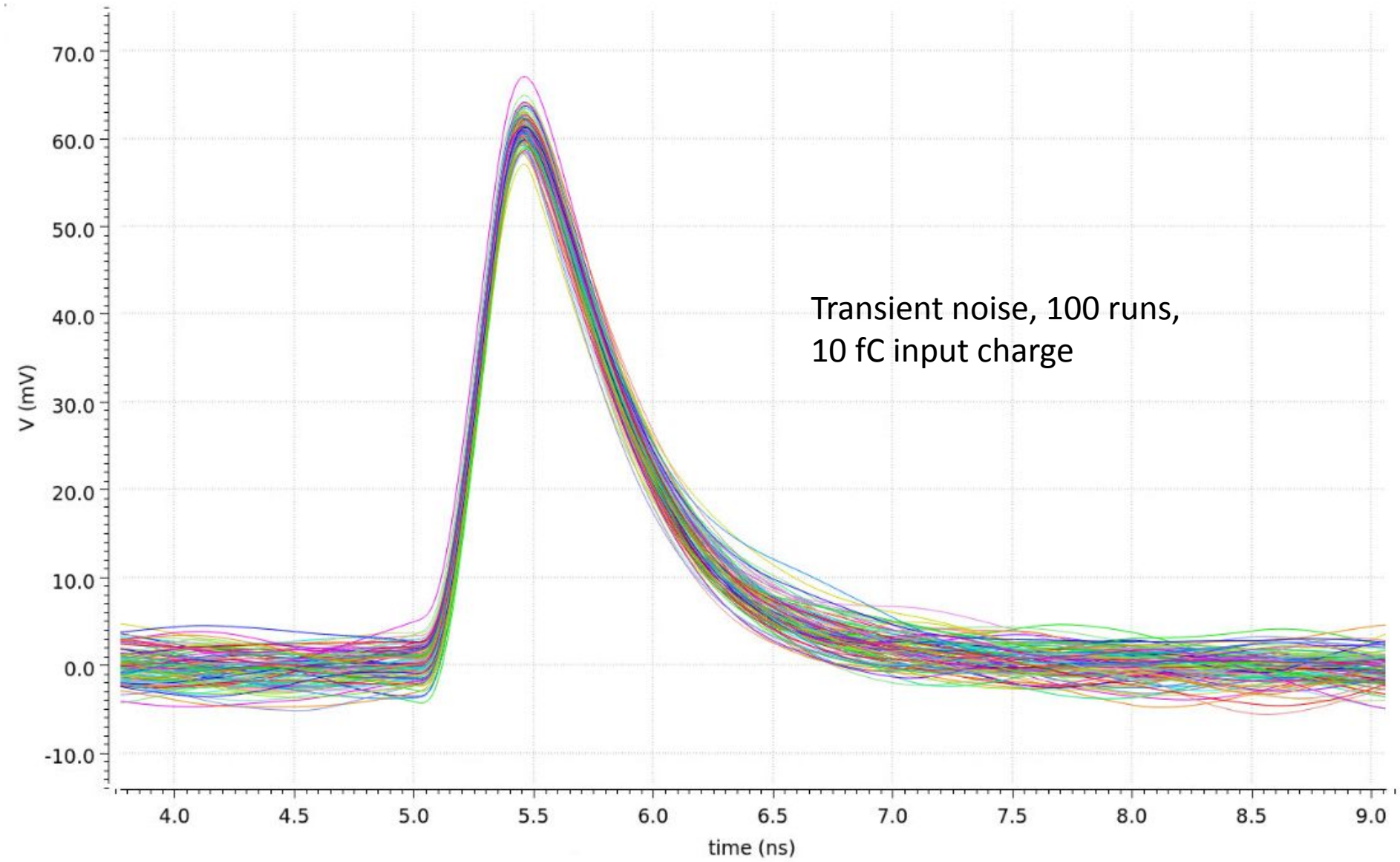
Preamplifier 3. VT variation



Режимный потенциал на входе (разброс дифференциального значения)



Шум (Transient noise) на выходе предусилителя



Сравнение ТЗ и моделирования

Параметр	ТЗ (NINO ver. 2)	Моделирование
Динамический диапазон	30-2000 фКл	30-2000 фКл
Джиттер (порог 120 мВ)	< 10 пс	< 15 пс (передний фронт) < 60 пс (задний фронт)
Шум при Сдет=0	< 2500 е	<2000 е
Peaking time	1 нс	500 пс
Перестраиваемое дифференциальное входное сопротивление	50-100 Ом	35-110 Ом
Регулируемый порог дискриминатора	10-100 фКл	10-450 фКл
Диапазон ширины импульсов на входе расширителя	1-6 нс	1-3 нс
Диапазон расширения импульсов на выходе	0-100 нс	0.5 - 100 нс