SPD COLLABORATION MEETING
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JINR, DUBNA

Development of an ASIC for straw and micromegas detectors of the NICA-SPD project

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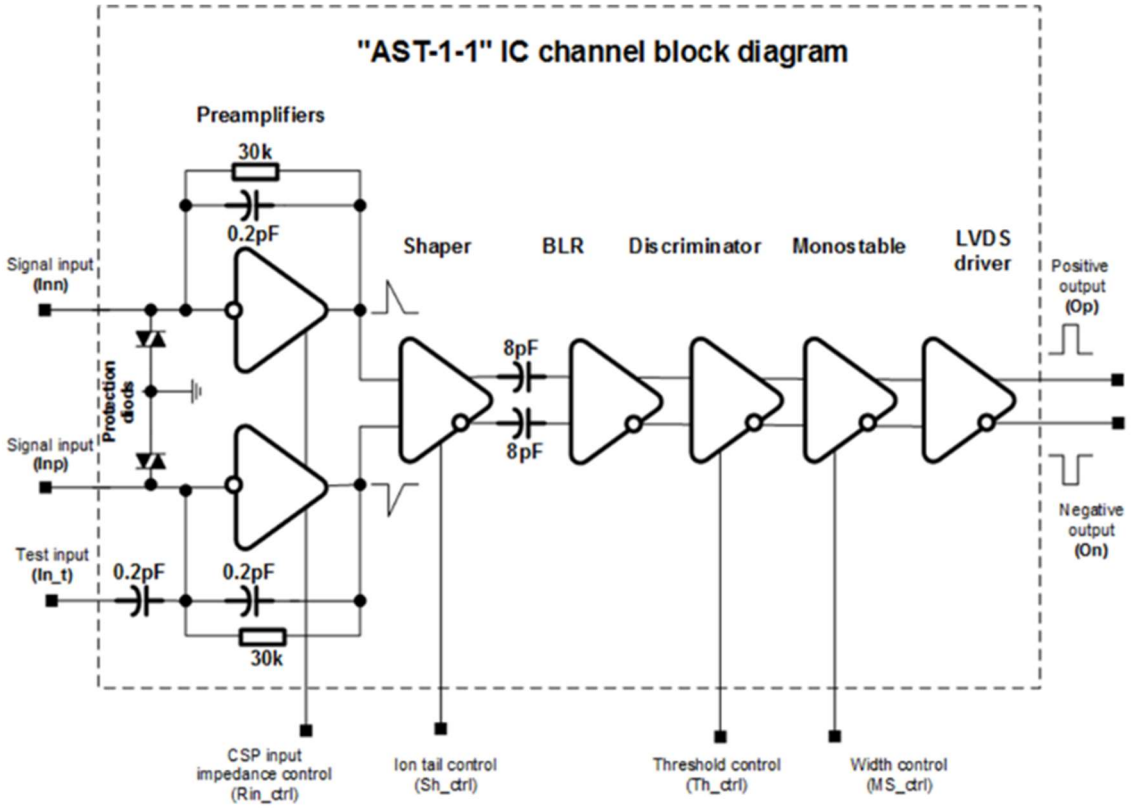
A front-end ASIC for CBM and NA64 straw detectors

A front-end called **AST-1-1** ASIC was developed for the straw detectors of the CBM experiment.

This chip is currently used in the straw detectors of the NA64 experiment and one of the silicon detectors of the BM@N experiment.

The main features of the AST-1-1 ASIC: eight channels, control of input resistance preamplifier, adjustment of the ion signal tail, BLR, two modes of discriminator operation: time over threshold and control of the output signal width, LVDS driver, the ninth channel for monitoring and shaping signal from the straw.

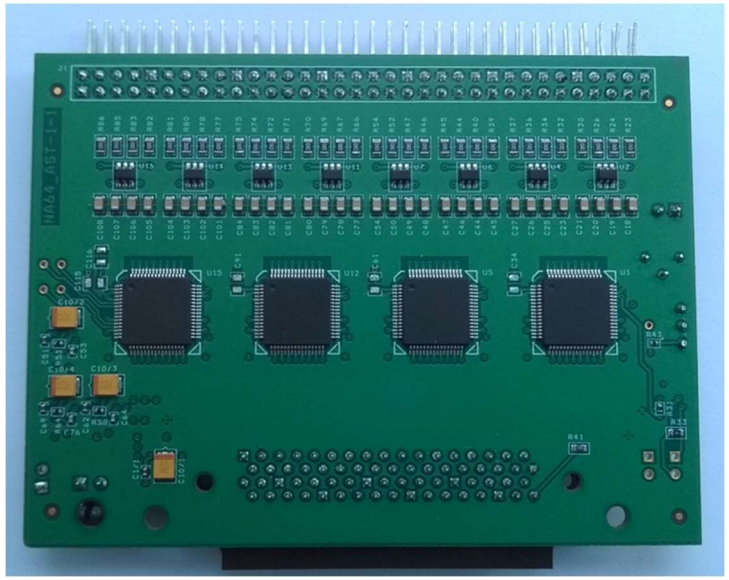


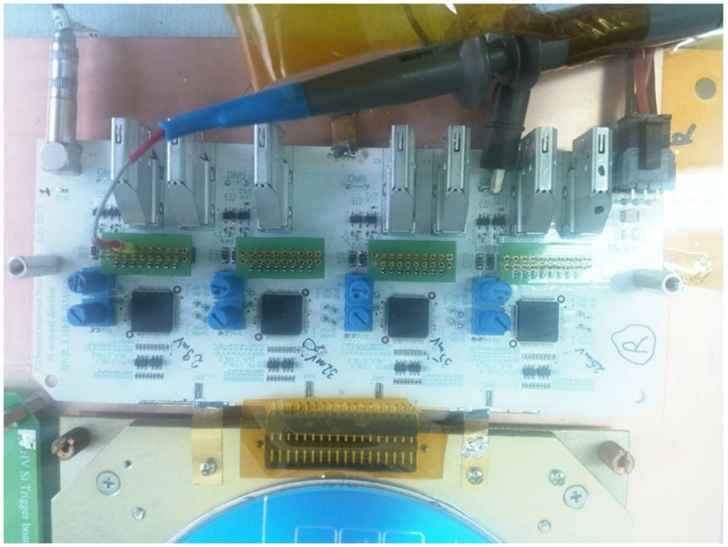
AST-1-1 ASIC block diagrams

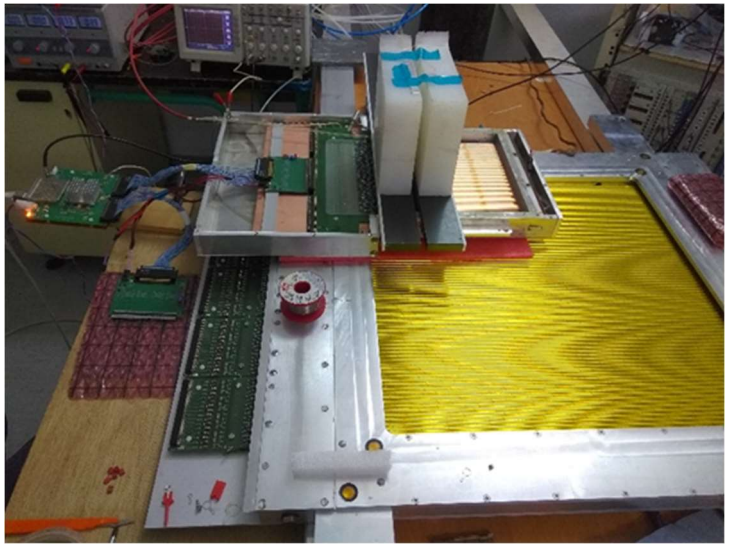
The main parameters of the AST-1-1

Package	LQFP64
Channels per chip	9
Main channels per chip	8
Main channel chain	CSP+Shaper+BLR+MS+LVDS
Ninth channel chain	CSP+Shaper+BLR
Chip technology	Bi-CMOS (0.6μm), X-FAB
Power supply	+(2.5÷3.3)V
Power consumption per channel	(12.2÷33.7) mW
Preamplifier input impedance, set by external resistor	(50÷560) Ohm
Differential gain	(25÷40.5) mV/fC *
Shaper (BLR) peaking time	(6÷8) ns*
Shaper (BLR) base-to-base	(11÷15) ns*
Threshold control	one for all channels
Minimum threshold	1fC
Threshold range	(1÷23) fC
Threshold spread	<10%
Noise frequency at the minimum threshold	<20 kHz
Output levels	LVDS
Minimum width of the output signal	5 ns
Output delay	6 ns
Test input	one for all channels
Internal test capacitor	0.2 pF

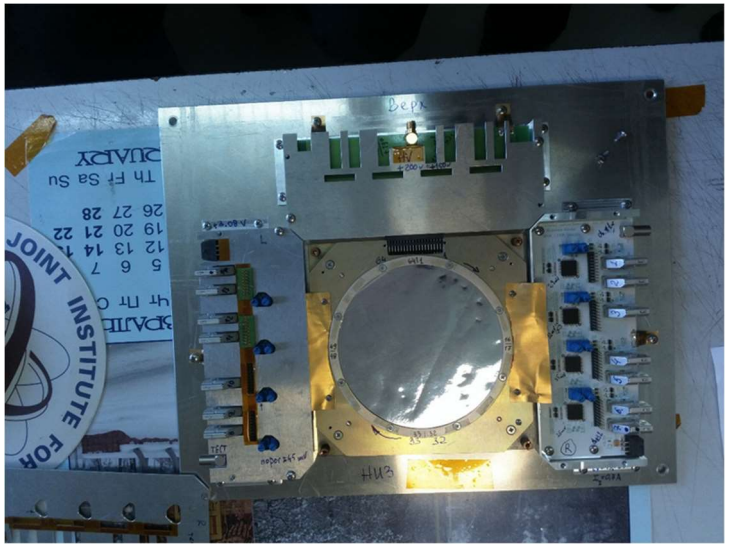
The readout PCB based on AST chips for NA64 experiment and B@NM experiments







NA 64



B@NM

The need for a new chip development is due to:

1) dE/dx measurements;

2) triggerless operation mode.

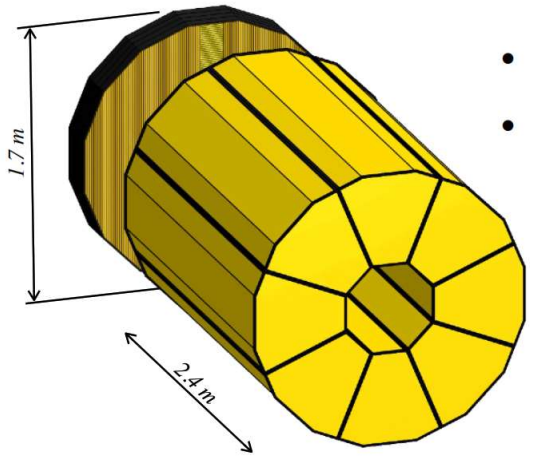
Measurements of dE/dx require measurement of the signal amplitude from the straw detector.

In the triggerless mode of operation, it is necessary to synchronize the data flow of the detector electronics with the time, according to which the SPD project will live, with external frequencies.

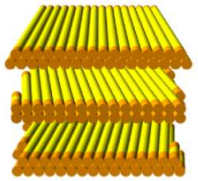
NICA-SPD Straw Tracker

Links:
https://disk.jinr.ru/index.php/s/MBwYDfCFAcQjdQt
http://spd.jinr.ru/wp-content/uploads/2021/04/SPD_Korzenev_DIS2021.pdf

Straw Tracker (ST)



- Barrel: 8 modules with up to 30 double-layers, *ZUV*
- Endcap: 12 double-layers, *XYUV* orientation



- Main tracker system of SPD
- Maximum drift time of 120 ns for ∅=10mm straw
- Spatial resolution of 150 μm
- Expected DAQ rate up to half MHz (electronics is limiting factor)
- Number of readout channels ~50k
- Can be used for PID if energy deposition if detected
- Extensive experience in straw production in JINR for various experiments (NA58, NA62, NA64…)

Summary table of straw detector parameters

Detector type	barrel	end-cap
Detector tasks	dE/dx	xy coordinates, dE/dx
Working mode	triggerless	triggerless
Detector inner diameter, mm	540	
Detector outer diameter, mm	1700	
Number of layers	30 (double layer)	2x, 2y, 2u, 2v
Number of stations, sections	8 sections	12 stations
Number of channels	32288	8192
Tube diameter, mm	10	10
Maximum tube length, mm	2400	1700
Central core diameter, mm	0.03	0.03
Maximum detector capacitance, pF	26	18,5
Gas detector	70 Argon, 30 CO_2	70 Argon, 30 CO_2
Operating voltage, V	+1650	+1650
Multiplication factor, HV=1750	4.5E4	4.5E4
Charge from the first electron, fC	7.7	7.7
Electron drift velocity, μm/ns	65	65
Electron drift time, ns	120	120
Ion drift time, μs	100	100
Spectral resolution, μm	150	150
Maximum load, kHz per tube	150	

Micromegas central tracker (MCT)

To provide a performance adequate for the physics tasks, it is proposed to install a relatively simple and cheap vertex detector based on micromegas technology. Such detector would be used during the first two or three years of the SPD running.

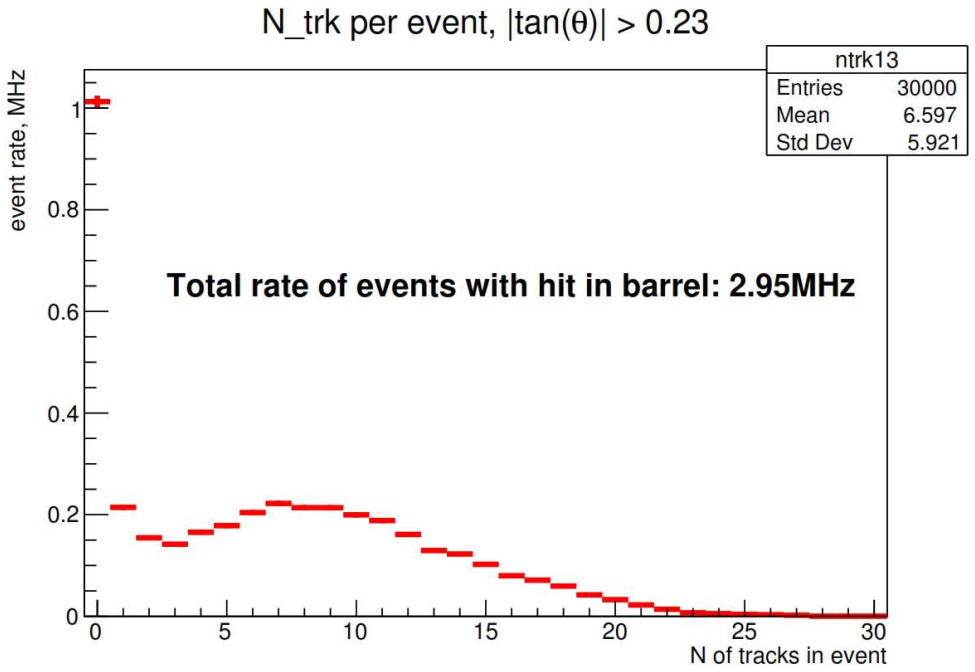
Detector tasks	xy coordinates method of weighted amplitude channel signals
Working mode	triggerless
Detector inner diameter, mm	54
Number of channels on the inner layer	728
Detector outer diameter, mm	188
The composition of the gas mixture (mobility of CO2+ ions 1.72 cm2/V*sec, electron drift velocity 0.3 cm/us)	70 Argon, 30 CO2
Anode capacity, pF	20÷200
Gap between cathode and grid, drift area, mm	5
Gap between grid and anodes, multiplication area, um (n is the number of layers of the photoresistor, the optimal value is n=2)	n*64
Multiplication factor	10000
Time of the electronic component in the drift region, us	2
Time of the electronic component in the multiplication region, ns	1÷2
Time of the ion component of the signal, ns	30÷140
Loading per channel, kHz	10÷100
Anode width, um	150÷300
Anode length, cm	до 100
Electrode potentials, V: cathode/grid/anode (capacitive coupling)	-350/0/+550
Design features	Charge distribution between 3÷5 anodes

Estimated event rate for staw detector

Simulation options:
- Pythia 8
- Magnetic field correction
- Pt>41MeV (hit threshold 40.5 MeV)
- Ecm=26GeV, L=10^32 cm^-2 s-1
- Inner layer of the detector: R=270, L=2360

Simulation results:
- Total event rate: 3.96 MHz
- Event rate with barrel tracks: 2.95 MHz
- Average tracks per barrel: 8.76
- Hit rate for innermost tubes (R=270, L=2360): **152 kHz**

Number of inner layer tubes: Nst=2*pi*27/1=170
Hit frequency for innermost tubes:
Fhit=2950*8.76/170=**152kHz**



Parameter accommodation for both straw and micromegas detectors

Parameter	straw	micromegas	Notes
Optimal number of channels	32 Channels step: 10 мм	32 Channel steps: 400 μm On the inner radius up to 502 channels or 16 chips	
Minimum number of channels	8	32	
Fast channel formation time, ns	6÷10	6÷10	Enough 8 bits
Slow channel formation time, ns	150	150, 250, 400	
Time channel resolution, ns	1	<5	
Amplitude channel resolution, bit	8÷10	8÷10	
ADC, bit	8÷10	8÷10	
Gain, mV/fC	1÷4	4÷10	Straw has 3 times more multiplication

AST-SPD chip specification

The working name of the new chip is AST-SPD (Amplifier for Straw Detectors-SPD)

Detector parameters		
Range of input charges, fC	+/-(0÷1000)	
Detector channel capacitance, pF	20÷100	
Loading per channel, kHz	150	
Working mode	triggerless	
Common chip parameters		
Technology	CMOS, 180 nm	
Number of channels	32	
Supply voltage, V	1.8	
Power dissipation, mW/ch	10	
Fast, time channel parameters		
Fast channel shaping time, ns	6÷10	
Time channel resolution, ns	1	
Discriminator threshold adjustment, fC	15	
ENC (r.m.s.), e Cd=60pF	<3000	
TAC time window, ns	500÷5000	
Parameters of the slow, amplitude channel		
Slow channel gain, mV/fC	straw	micromegas
	1/3	3/9
Slow channel shaping time, ns	straw	micromegas
	75/150	250/400
Base signal width, ns	300/600/	1000/1600
Shaper order	4	
ADC capacity, bit	10	
ENC (r.m.s.), e Cd=60pF	<3000	

AST-SPD chip block diagram

The block diagram will be fixed according to the simulation results

Channel options

Channel optimization criteria:
1) event rates
2) dead time
3) power dissipation
4) chip area

Abbreviation:
CMOS - field technology
CSP - Charge Sensing Amplifier
FS - fast shaper
SS - slow shaper
Dis - discriminator
MUX - multiplexer
TAC - time-to-amplitude converter
SAR ADC - Serial ADC
sLVDS - low-voltage LVDS

#1

<table>
<tr><td rowspan="2">CSP</td><td>FS</td><td>Dis</td><td>TAC</td><td>MUX 32:1</td><td>SAR ADC</td></tr>
<tr><td>SS</td><td colspan="2">PD</td><td>MUX 32:1</td><td>SAR ADC</td></tr>
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One SAR ADC in chip for time channel
One SAR ADC in the chip for the amplitude channel
Digitization time up to 100 ns
Readout up to 10 channels

#2

<table>
<tr><td rowspan="2">CSP</td><td>FS</td><td>Dis</td><td>TAC</td><td rowspan="2">MUX 2:1</td><td rowspan="2">SAR ADC</td></tr>
<tr><td colspan="2">SS</td><td>PD</td></tr>
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One SAR ADC per channel
Digitization time up to 500 ns

#3

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<tr><td rowspan="2">CSP</td><td>FS</td><td>Dis</td><td>TAC</td><td>SAR ADC</td></tr>
<tr><td colspan="2">SS</td><td>PD</td><td>SAR ADC</td></tr>
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Two ADC SARs per channel
Digitization time up to 1 μs

Other chip properties

Additional functions	OR output of discriminators Testing individual channels Disable noisy channels Выбор временного окна TAC
ADC data outputs	Parallel
Digital IO signals	sLVDS
Settings	Configuration register
Analog output	Multiplexer output for controlling the operation of the peak detector and connecting an external ADC
Test channel	Shape and gain control of analog signals: differential outputs of fast and slow drivers Control of the operation of the discriminator and time-to-amplitude converter

Development stages of the AST-SPD chip

1) Circuit design and simulation of the AST-SPD
Terms of work: from 01.09.2022 to 30.04.2023

2) AST-SPD topology development
Terms of work: from 05/01/2023 to 12/20/2023

3) Manufacturing of wafers with AST-SPD chips of the first iteration
Terms of work: 01/01/2024 to 12/20/2024

Wafer production is possible at semiconductor factories: X-FAB (Germany), Mikron (Russia)

AST-SPD chip development status

Work on the development of AST-SPD has started

JINR and INP BSU signed a contract for the execution of works on the first stage:
Circuit design and simulation of the AST-SPD

Works of the first stage:
1) Circuit design and simulation of the AST-SPD of individual blocks of the channel IS AST-SPD
2) Selection of the working option of the channel AST-SPD
3) Assembly and modeling of the top-level AST-SPD