ASIC for SPD project

to be continued

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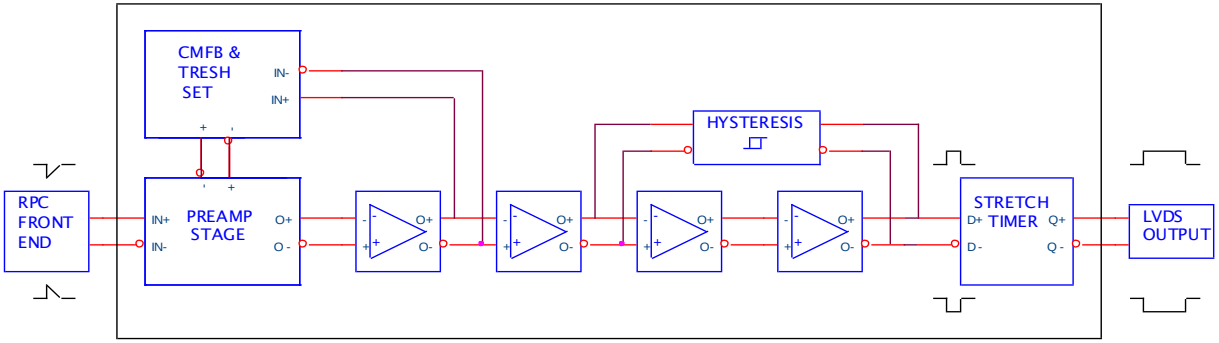
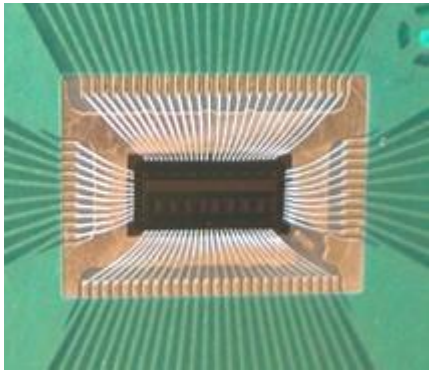
Introduction.

1. We started ASIC design from a TOF detector and ECAL for which the NINO chip is a good prototype.
2. NINO chip is amplifier-discriminator – it is cheapest solution for ASIC design.
3. Our task is to refuse the use of ADC-related solutions. The reason is optimization of price, power and space.
4. The implementation of TOT method will require upgrading the chip structure.

NINO ASIC for ALICE TOF specifications.

NINO ASIC is a first especial design for TOF application, CERN, 2002–2005

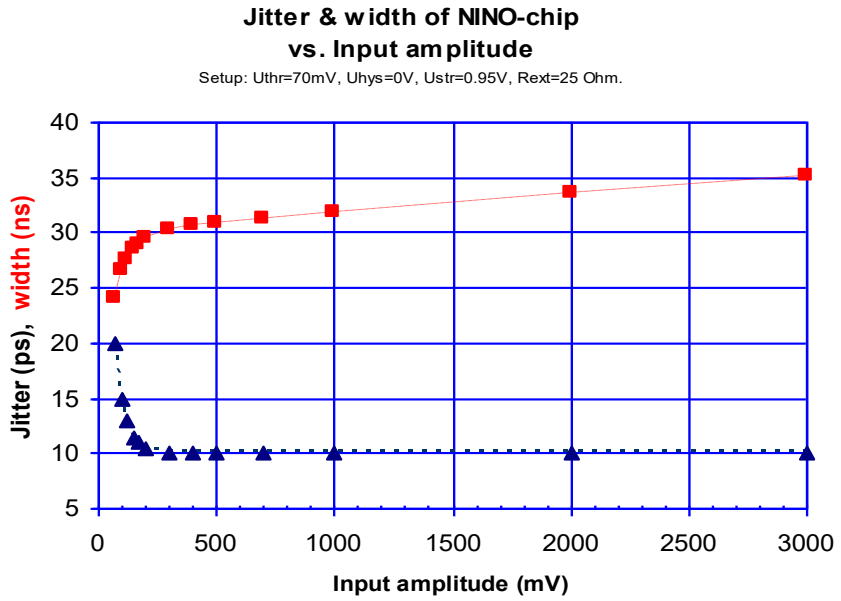




NINO ASIC electronic channel main specs:

- 8-channel differential input-output structure
- < 10ps time jitter
- 1-6ns TOT width
- input resistance matching from 40 to 75 Ohm
- stretch time expanding
- hysteresis adjustment

The main problem –
incorrect implementation of TOT method!



PADI, an ultrafast Preamplifier - Discriminator ASIC for Time-of-Flight Measurements

M. Ciobanu *, N. Herrmann, K.D. Hildenbrand, M. Kiš, A. Schüttauf, H. Flemming, H. Deppe,
S. Löchner, J. Frühauf, I. Deppner, P.A. Loizeau, M. Träger

Developing for CBM TOF, GSI, Darmstadt, Germany starting 2005, not finish now.

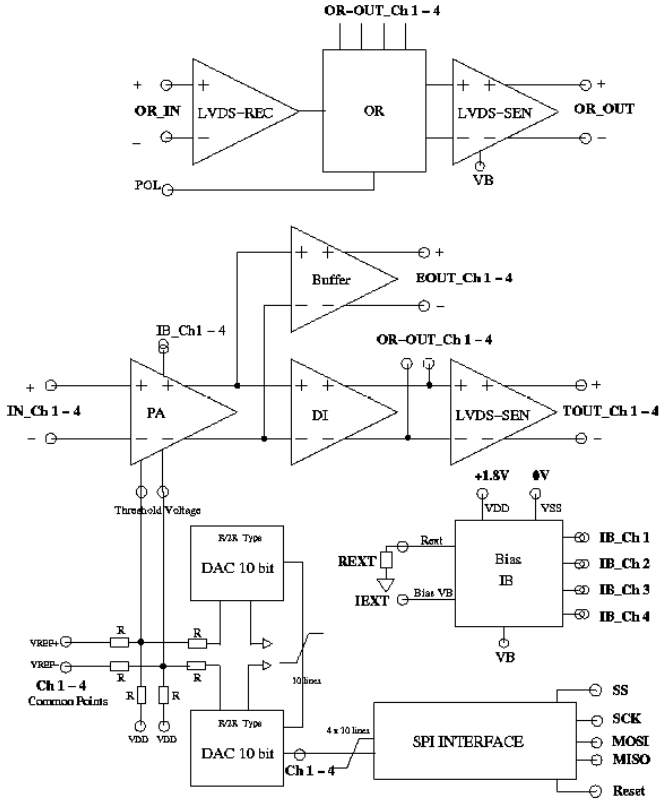
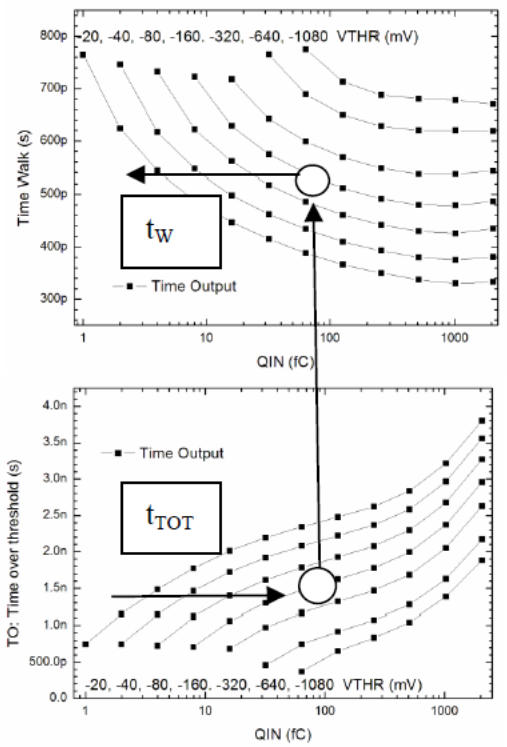


Figure 12: *Block diagram of PADI-6. In PADI-7 the SPI interface and the 2 DACs have been left out.*



MAIN PARAMETERS OF THE PADI FAMILIES

Main parameters comparison	PADI-1	PADI-2	PADI-6	PADI-8
Channels per chip	3	4	4	8
PA Bandwidth (MHz)	280	293	416	411
PA Voltage Gain	74	87	244	251
Conversion Gain (mV/fC)	6.3	7.8	35	30
Baseline DC offset, σ (mV)	6.7	21.9	5.9	1
PA Noise (mV_{RMS})	3.37	2.19	5.82	5.5
Equivalent Noise Charge (e_{RMS})	3512	1753	1039	1145
Threshold type	Extern	Extern	Ext. & DAC	DAC
Threshold dynamics (+/- mV)	Non.lin. 280	Non.lin. 300	Lin 500	Lin 750
Input Impedance Range (Ω)	30 - 450	37 - 370	38 - 165	30 - 160
Power consumption (mW/channel)	21.6	17.4	17.7	17

ASIC development – iterative process.

The usual number of iterations of ASIC creation is 3-5.

Each iteration lasts 1.5-2 years and consists of three phases each time:

1. **CADENCE schematic and topology design.**
2. **Production phase.**
3. **Testing:**
   - **Bounding on evolutions board,**
   - **Laboratory testing,**
   - **Beam testing.**
   - **Evaluation of results.**

Incomplete ASIC's account for 70% of those started

Why does the creation of ASIC fail?

ASIC is a complex chip that requires fundamental research and highly qualified specialists.

The main reasons for failures:

1. **Problem statement errors (For example, politicians manage the process).**
2. **Poor quality or neglecting of the research phase.**
3. **Lack of qualified personnel.**

The main reason for delaying the development time is poor-quality research

What ASIC do we still need to develop?

Let's be realistic and focus on two types. :

1. **Multichannel TDC – prototypes HPTDC (CERN), GET4 (GSI, Darmstadt).**
2. **Multichannel ASIC for APD and SiPM application prototype FastIC (CERN, Spain). It is possible to combine functions in one design with a new NINO-based chip.**

It is necessary to create a laboratory for the development and research of ASIC in Dubna.

The end.

To be continued?