MPD Data Acquisition System Status

Ilia Slepnev
MPD DAQ working group

A. Baskakov, S. Bazylev, A. Egorov, A. Fediunin, I. Filippov, S. Kuklin,
A. Shchipunov, A. Shutov, I. Slepnev, V. Slepnev, N. Tarasov, A. Terletskiy

Joint Institute for Nuclear Research

X Collaboration Meeting of the MPD Experiment
at the NICA Facility

MPD DAQ Design Goals

Properties

Reliable data transfer. Pipeline operation with synch and async stages.
Extensive diagnostics in hardware and software. Monitoring, logging.
Data integrity check on all levels. CRC, sequence numbers, FEC.
Fault tolerant, Highly available. Fast self recovery after SEU events.
Distributed, scalable, extendable. Based on open and industry standards.
Flexible architecture. Partitioning for independent subsystem operation.

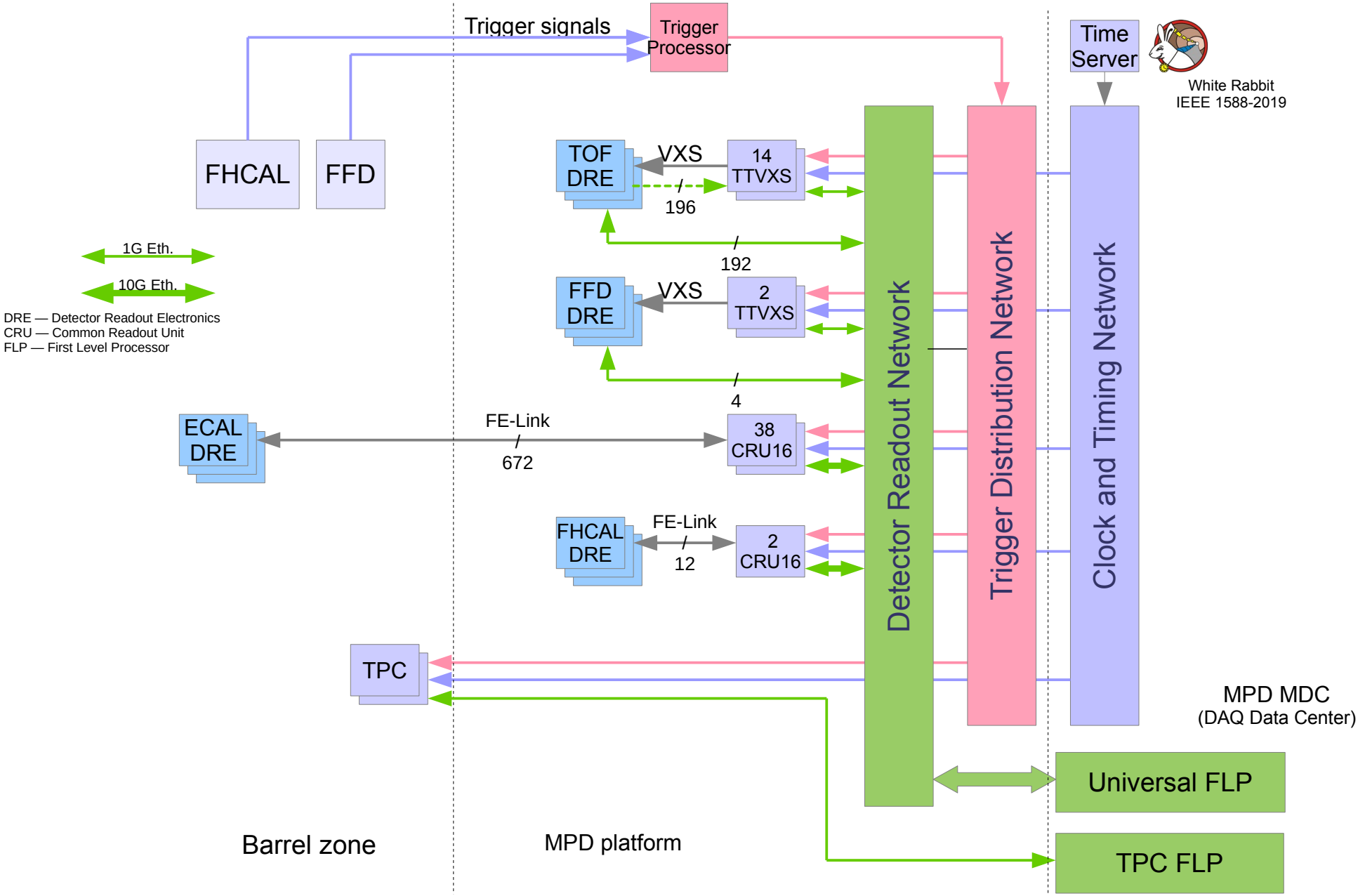
Operation Modes

Multiple hardware trigger classes
Uncompressed, full raw data during MPD commissioning
Large calibration data events at low trigger rate
High multiplicity events from central collisions at planned trigger rate

DAQ in numbers

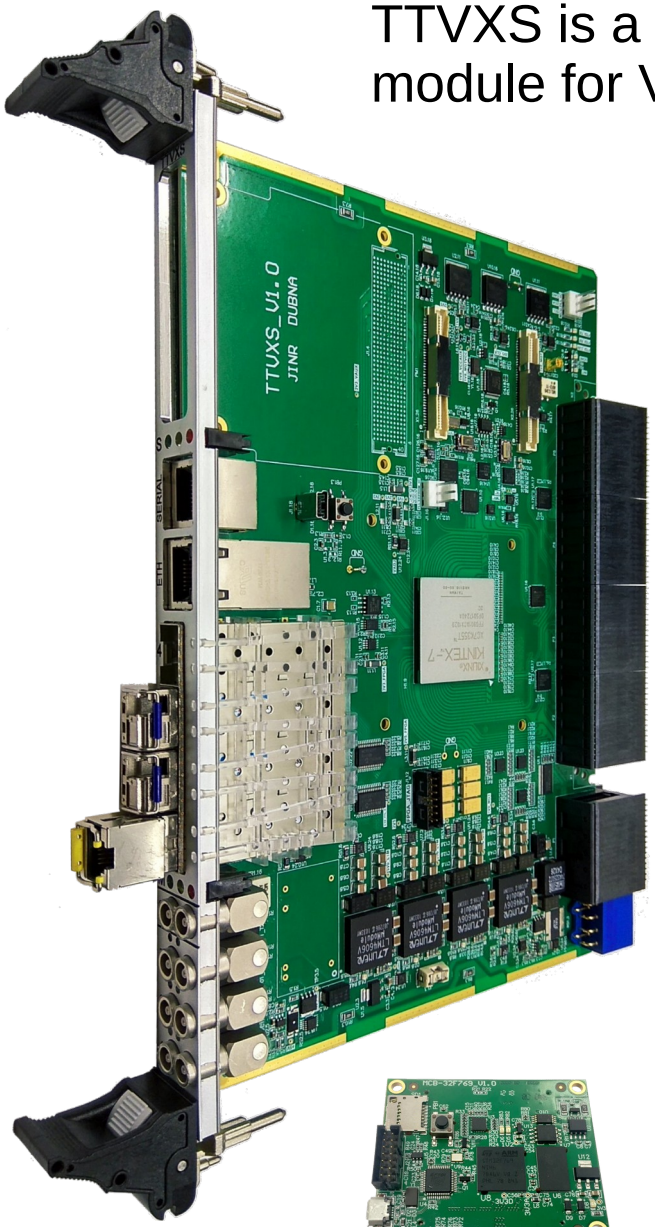
Up to 7 kHz trigger rate, over 1 MB compressed event size to storage device
From 5 to 30 GB/s uncompressed raw data rate from readout cards to FLP
Up to 20 PB per year of raw data

MPD DAQ Architecture



TTVXS — VXS Switch Board

TTVXS is a Time, Trigger and Management module for VXS crate



IPMI mezzanine board

- Clock, timestamp and trigger distribution to VXS payload boards: backplane FE-Link protocol
- 4 SFP+ sockets for Detector Readout, Trigger Distribution and Clock & Timing connections
- Reference frequency and timestamp provided by White Rabbit Network or FE-Link (with CRU-16)
- Additional clock and trigger interface by FMC (VITA-57) card slot – integration with other systems

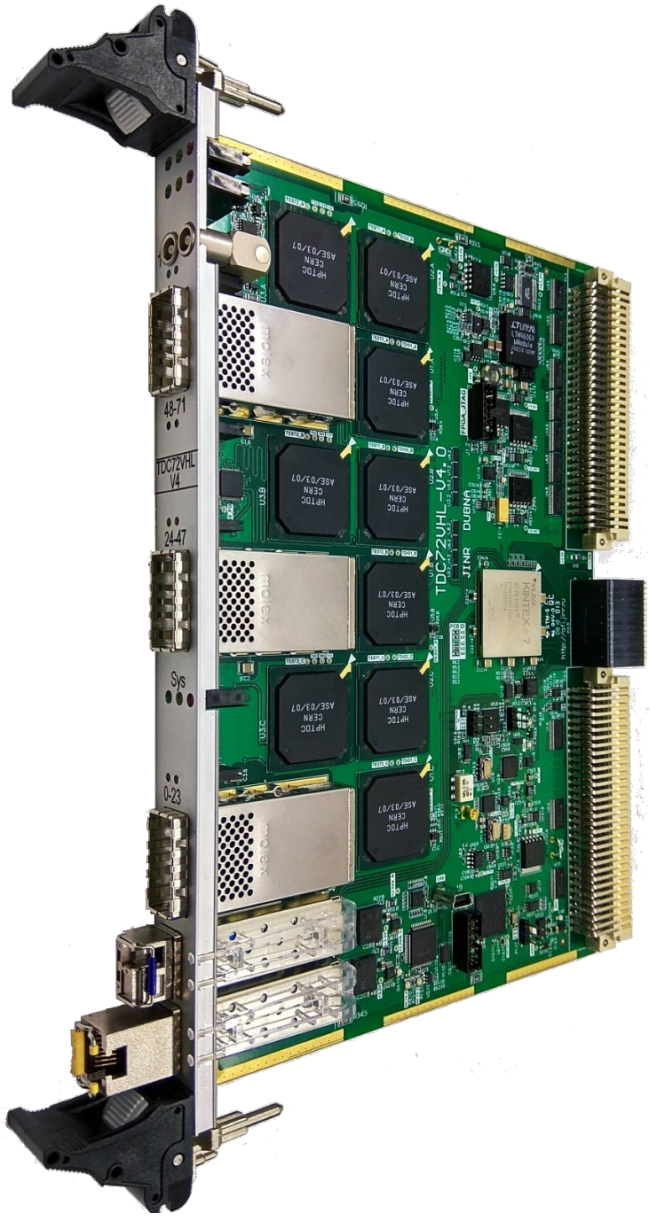
Status: 20 boards ready. Basic functions implemented.

IPMI mezzanine board

- IPMI (Intelligent Platform Management) function for automatic topology discovery, module status monitoring and control, firmware update

Status: basic functions implemented, improvements ongoing

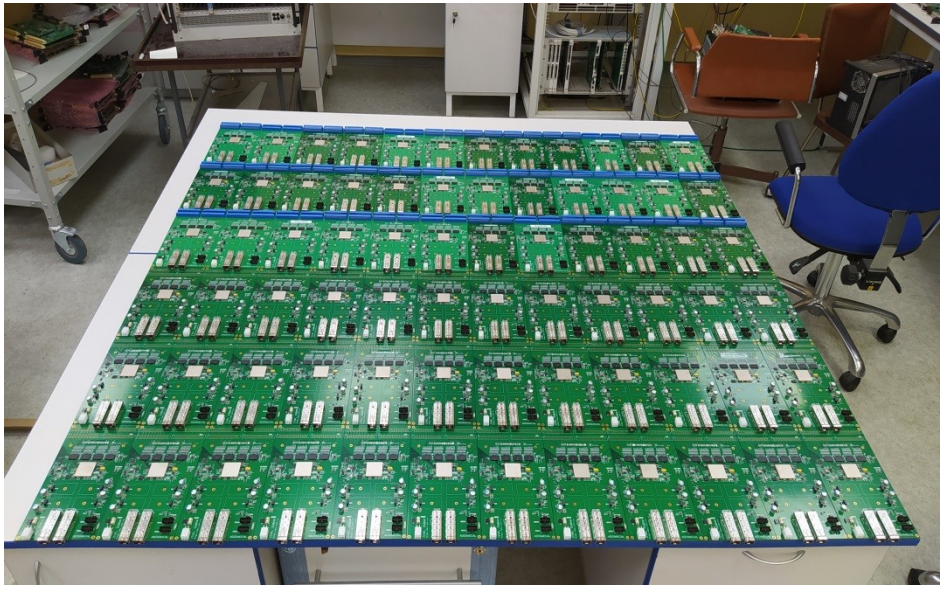
TDC72VHL — Multihit 25 ps Timestamping TDC



TDC72VHL board performs time-stamping of discrete signals (hits). It is based on HPTDC chip. Hit timestamps are kept for 104 μs in ring type memory.

Number of Channels	72
Input Signal	LVDS
Input Impedance	100 Ohm
Input Differential Voltage	25 mV min
Input Connector	CXP Interconnect System
Time Resolution with INL	~25 ps
Data Transfer Interface	1Gb/s Ethernet
Synchronization Interface	Backplane FE-Link

Waveform digitizer for ECAL – ADC64ECAL



Batch of 72 boards

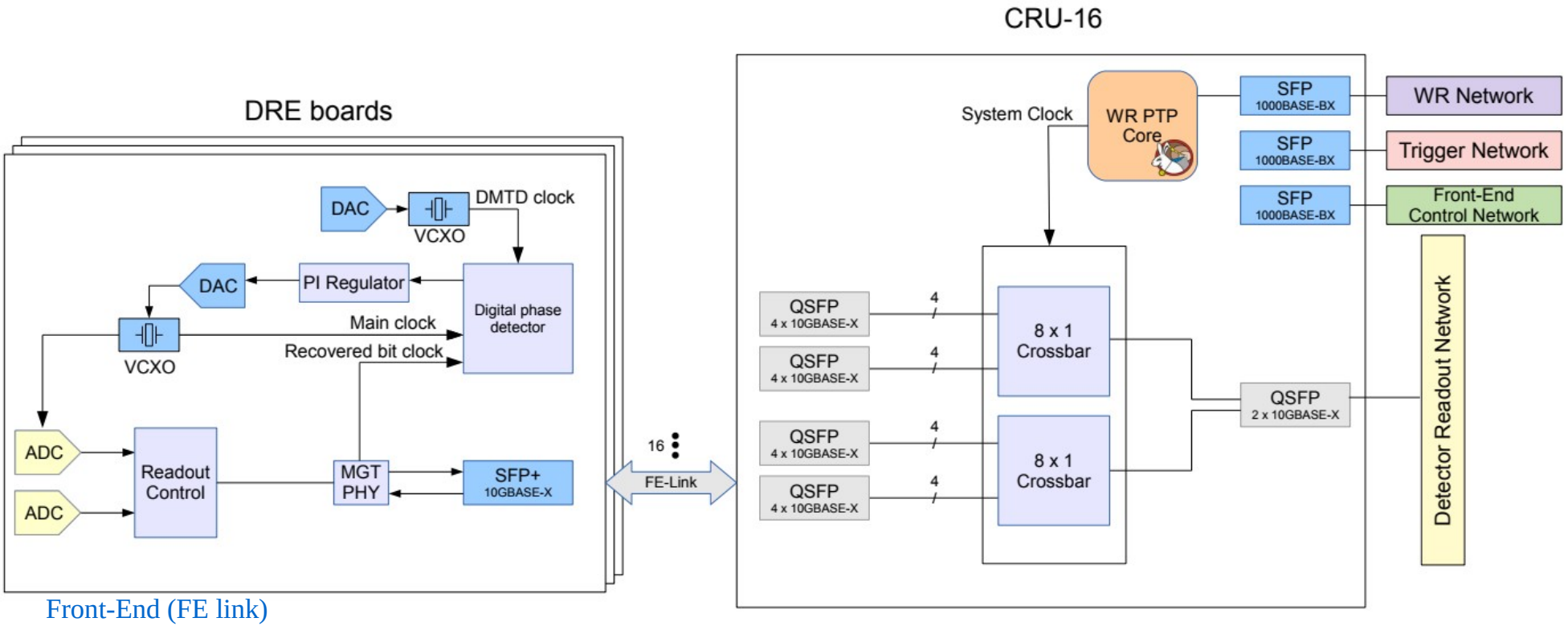
ADC64ECAL under test, passive air cooling

ADC64s2-v5 assembly
(FHCAL)

ADC64* board characteristics

	ADC64ECAL	*ADC64s2-v5*
Number of Channels	*64*	*64*
Sample rate	*62.5 MS/s*	*62.5 MS/s*
Resolution	*14 bit*	*14 bit*
Power consumption	*< 15 W*	*< 20 W*
Magnetic field tolerance	*by design*	*No*
Radiation hard DC/DC	*yes*	*No*

Common Readout (and everything else) Unit



Front-End (FE link)

"Variable-speed Synchronous Ethernet". Byte-oriented, 8b/10b Ethernet like encoding and framing

Maximum data rate: 2.5 Gb/s VXS backplane (TTVXS), 8 Gb/s (CRU-16) with commercial QSFP fiber-optical transceivers.

DRE clock synchronized to CRU with digital PLL. Short fixed cables – one time delay calibration.

Timestamps, trigger, data readout, control over same link

No TCP-IP stack complexity in DRE. Simple FGPA code with fail-safe FSM and data pipelines to mitigate SEU events.

Aggregation *"switch"* (CRU-16 core)

Not an Ethernet switch. Fixed traffic directions: left-right or right-left only. Connects to DAQ network with 10G Ethernet, UDP-IP.

Large FPGA on board running White Rabbit and service CPUs

Extensive diagnostics: hardware histograms, RAM-based multichannel counters

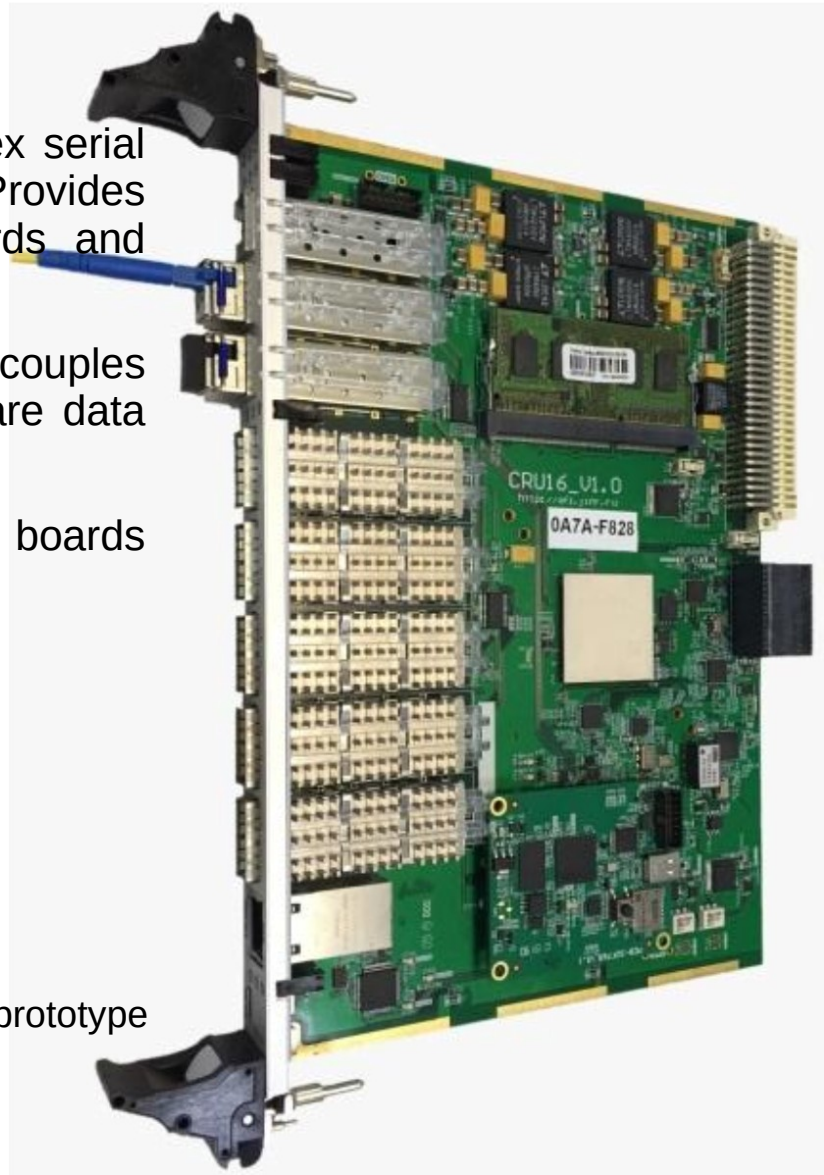
Use speed translation FIFOs. Arbitrated crossbars. DDR3 SDRAM onboard (packet buffers)

Future: hardware event merging for connected DRE boards

CRU-16

Common Readout Unit for 16 DRE boards

- FE-Link interface to DRE boards - multi-gigabit duplex serial synchronous interconnect with deterministic latency. Provides clock and trigger information for downstream boards and receives raw data stream
- 4 GB SO-DIMM DDR3 memory for data buffers. Decouples realtime hardware data flow from high latency software data receivers
- 4 QSFP downlink sockets for 16 Detector Readout boards connections grouped by 4
- 3 SFP sockets for Trigger Distribution, Clock & Timing
- Management mezzanine board
- Timing synchronization by White Rabbit Network



Status

- Hardware manufactured. All module components tested
- Some firmware parts ready. FE-Link designed and tested on prototype
- Control software under development

DAQ Electronic Modules Production

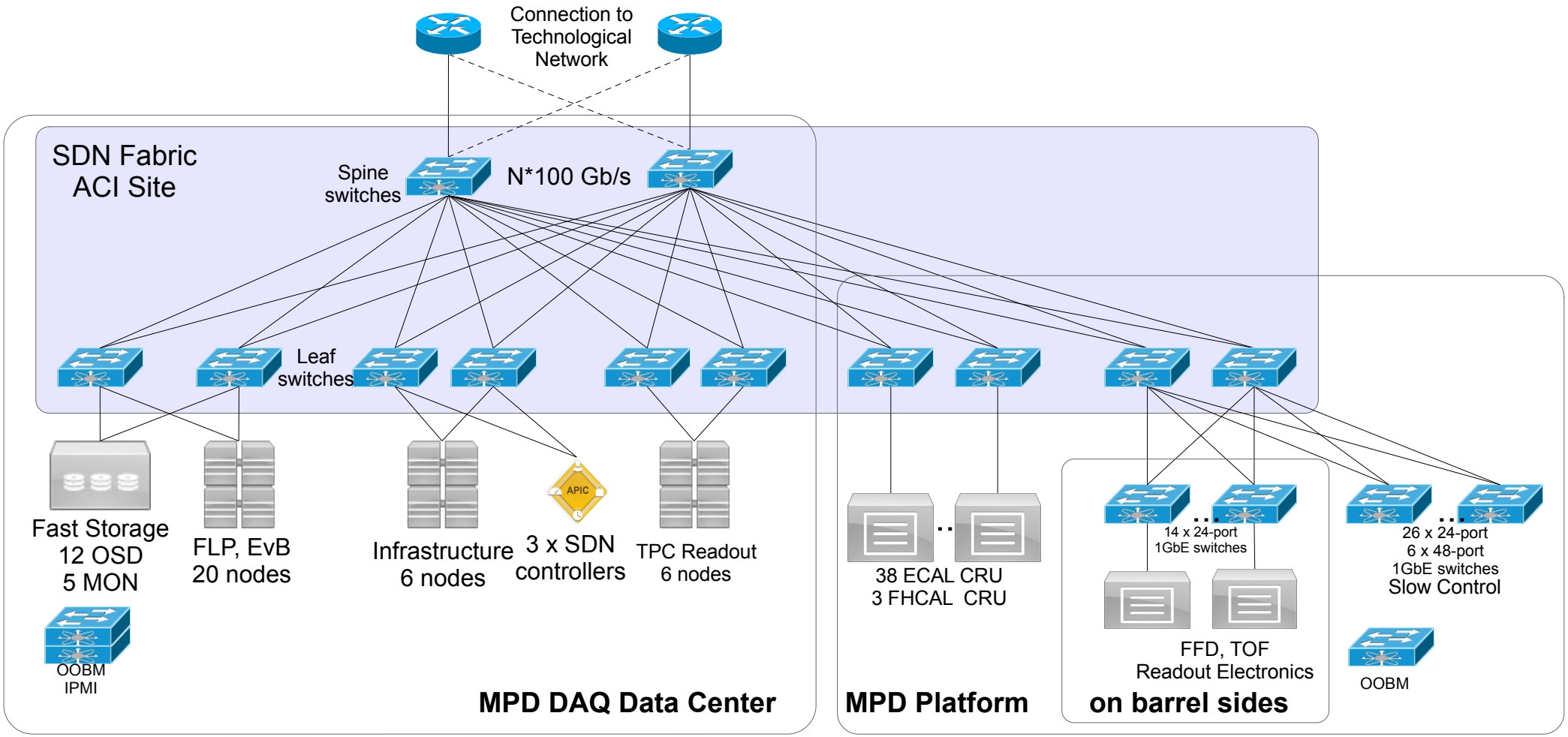
Product	Required boards						Manufactured and Tested Q4 2022	Progress
	ECAL	FHCAL	FFD	TOF	TPC	Trigger Distrib.		
TDC72VHL	—	—	10	196	—	—	219	106 %
TTVXS	—	—	2	14	—	—	20	125 %
ADC64-ECAL	600	—	—	—	—	—	500	83 %
ADC64S2 v5	—	10	—	—	—	—	10	100 %
CRU16	38	3	1	1	—	6	45	92 %

TDC72VHL, TTVXS:
- Hardware ready 100%
- Firmware with basic functions tested on TOF stand
- Software ready
- "FE-Link over VXS" firmware under development

CRU-16 status
- Hardware manufactured
- All on-board components tested
- Some firmware parts ready
- FE-Link designed and tested on prototype
- Control software under development

ADC64 family
- Hardware: need ADC64100 ECAL boards more
- Tested on stands and BMN
- Refactoring monolithic to modular design (firmware and software) in progress.

MPD DAQ Network



MPD DAQ Modular Data Center

2020-2021: Delivery, installation, testing
June 2021: Put in operation

MPD DAQ Data Center

MPD DAQ Data Center Infrastructure

- Entrance Area
- Automatics Rack

- Rack power switches: 2 independent lines
- Battery backup: 15 minutes at 100% load
- Main Switchboard: 110 kW input power

Quad Precision Air Conditioners
N+1 redundancy

- Maximum total rack power with N+1 redundancy: 50 kW
- Maximum measured rack power with installed hardware: 26 kW

MPD DAQ Control Room

Thank you!