

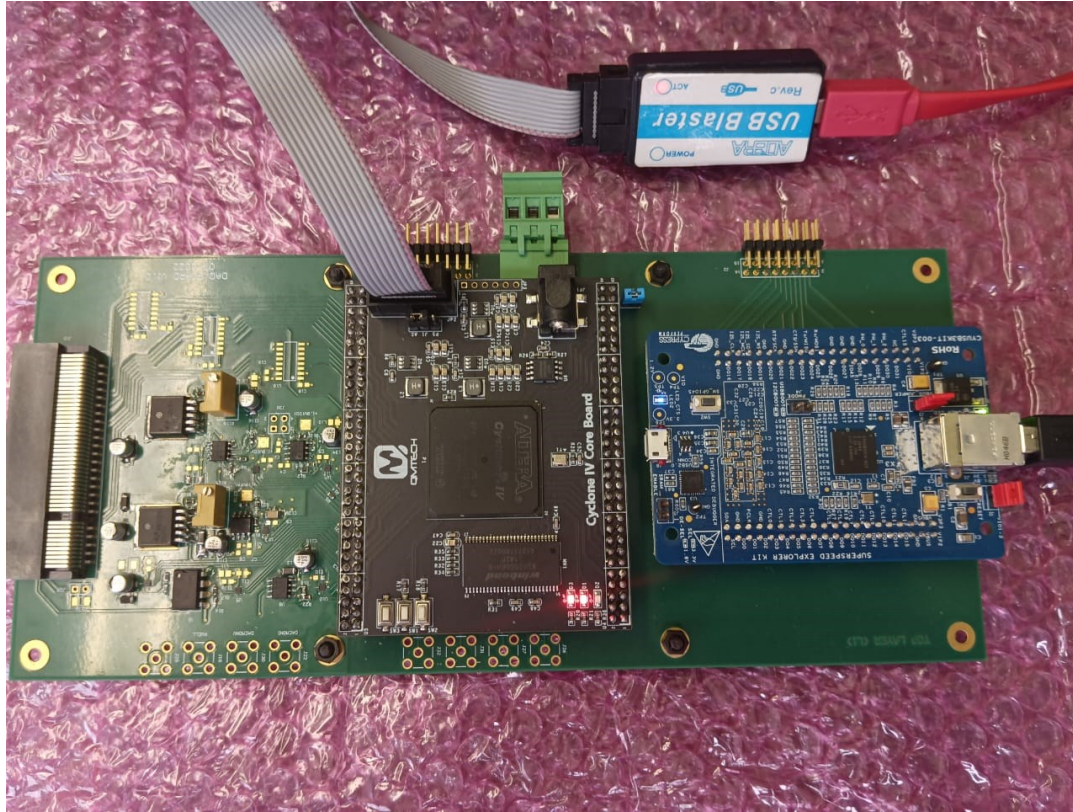


# Electronic Status

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Raúl Arteche Díaz

STS Department Meeting, 2021.10.03



- The digital part of the first DAQ board prototype is already mounted, the system is under test.
- The firmware running on the original DAQ board is already ported to this new board.
- The USB communication with the Altera FPGA is under test.
- The next step will be the testing of the interface with the analog part of the design.

## Chapter 1: Configuration Overview

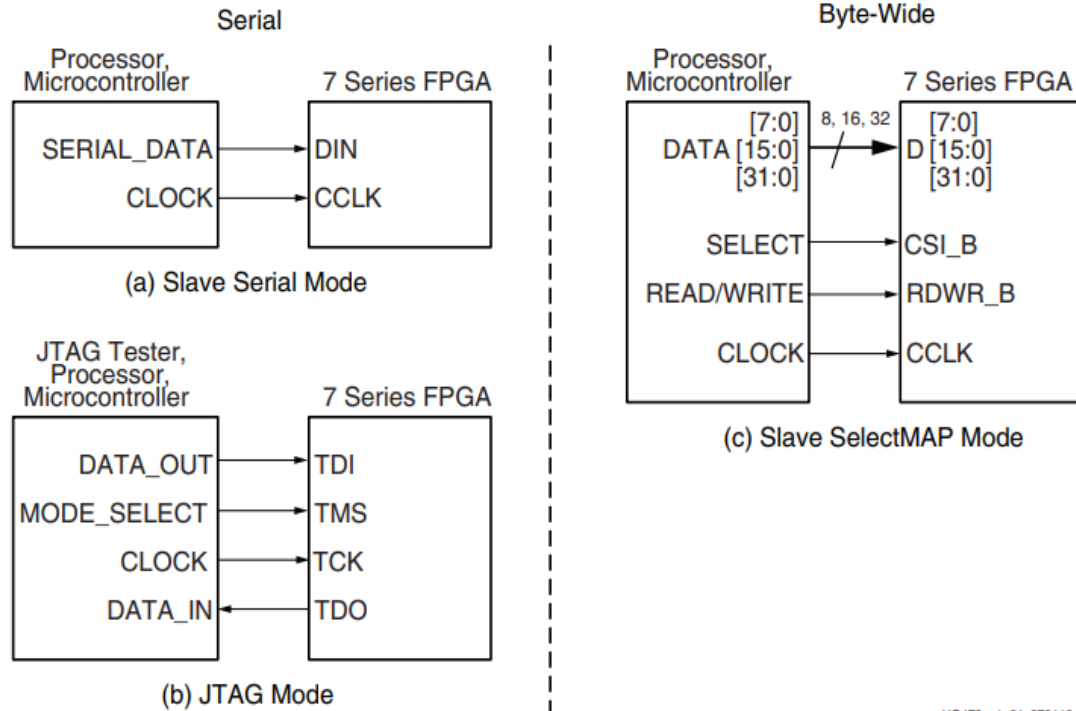
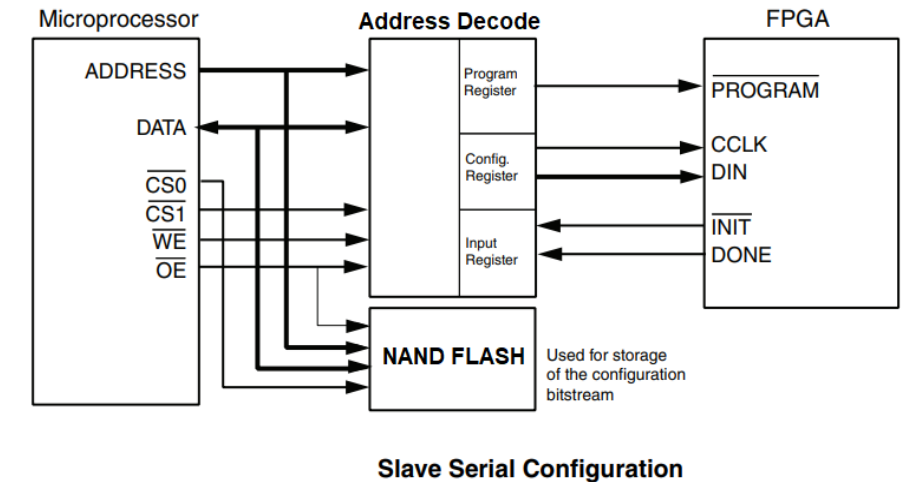
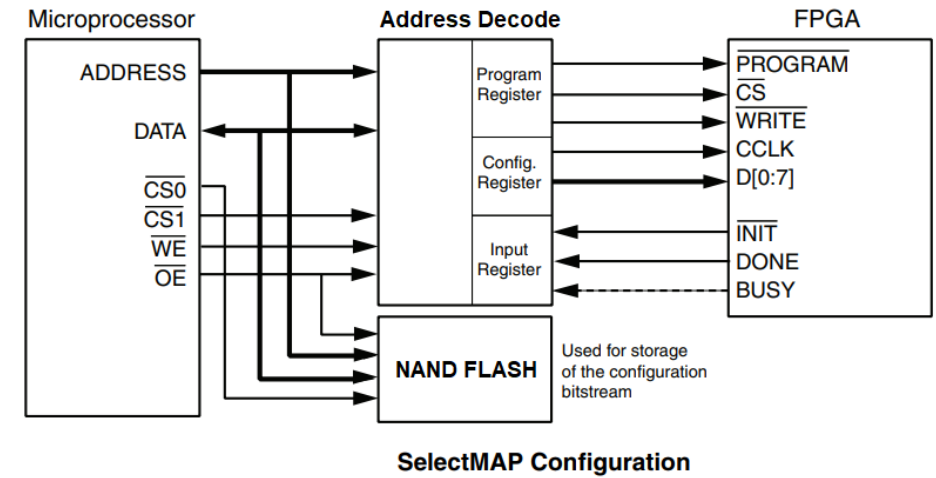


Figure 1-1: Slave Configuration Modes

The Slave Serial mode is extremely simple, consisting only of a clock and serial data input. The JTAG mode is also a simple serial configuration mode, popular for prototyping and highly utilized for board test. The Slave SelectMAP mode is a simple x8-, x16-, or x32-bit-wide processor peripheral interface, including a chip-select input and a read/write control input.

## 7 Series FPGAs Configuration User Guide (UG470)



## Using a Microprocessor to Configure Xilinx FPGAs via Slave Serial or SelectMAP Mode Application Note (XAPP502)

AnyDesk 904 788 548

904788548

Altium Designer (14.3) - E:\prj\FPGA\_PA3\_CONTROL\control.c - FPGA\_PA3\_CONTROL.PrfPg: Not signed in.

FlashPro - [FPGA\_PA3\_CONTROL] \*

Programmer List:

Programmer Name	Programmer Type	Port	Programmer Status	Programmer Enabled
1 95794	FlashPro4	usb95794 (USB 2.0)	RUN PASSED	<input checked="" type="checkbox"/>

Refresh/Rescan for Programmers

Messages:

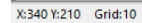
Class	Document	Source	Message	Time	Date	No.
ProcessFlowInfo	FPGA_PA3_CONTROL.SDF	Timing Analysis	designer - Completed Successfully	05:07:20	03/10/2022	190
ProcessFlowInfo	FPGA_PA3_CONTROL.SDF	Make Bit File	Running designer On E:\prj\FPGA_PA3_CONTROL\ProjectOutputs\Configuration\FPGA_PA3_CONTROL.SDF	05:07:20	03/10/2022	191
ProcessFlowProgress	FPGA_PA3_CONTROL.SDF	Make Bit File	Running E:\Microsem\Libero_SoC_v11.8\Designer\bin\designer.Exe...	05:07:20	03/10/2022	192
ProcessFlowInfo	FPGA_PA3_CONTROL.SDF	Make Bit File	Info: The design FPGA_PA3_CONTROL.ADB was last modified by software version 11.8.0.26.	05:07:24	03/10/2022	193
ProcessFlowWarning	FPGA_PA3_CONTROL.SDF	Make Bit File	Warning: Overwriting the existing file: E:\prj\FPGA_PA3_CONTROL\ProjectOutputs\Configuration\FPGA_PA3_CONTROL.pdb.	05:08:07	03/10/2022	194
ProcessFlowInfo	FPGA_PA3_CONTROL.SDF	Make Bit File	designer - Completed Successfully	05:08:07	03/10/2022	195

Windows PowerShell

```
***** Xilinx hw_server v2019.2.1
**** Build date : Dec 5 2019 at 05:23:28
** Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.

INFO: hw_server application started
INFO: Use Ctrl-C to exit hw_server application

INFO: To connect to this hw_server instance use url: TCP:DESKTOP-4U6DPFF:3121
```





Altium Designer (16.1) - D:\work\MPD-ITS-RU\FPGA\_PA3\_CONTROL\control.c - FPGA\_PA3\_CONTROL.PrjFpg. Not signed in.

Workspace1.DsnWrk | Workspace

FPGA\_PA3\_CONTROL.PrjFpg | Project

Files | Structure

FPGA\_PA3\_CONTROL.PrjFpg

- Source Documents
  - Top.SchDoc
  - nand\_flash\_interface.V
  - nand\_interface\_core.V
  - CLKBUF\_LVDS\_IN.Vhd
  - DECODE.Vhd
  - control.c
- Settings
- Generated (Configuration)

```

SCRUB_CTL_T = 0x00;
SCRUB_CTL   = 0xff;

SCRUB_DEBUG = NAND_RB_Y_1 | NAND_RB_Y_2;

while(1)
{
    counter=0;
    Data_Rcv=CheckUART();
    if(Data_Rcv==1)
    {
        bank1=CheckUART();
        bank2=CheckUART();
        Block_No=(bank1 + (bank2 <<8));
        rc =NAND_EraseBlock(Block_No);
        if(rc!=NAND_IO_RC_PASS)
        {
            Uart_Tx(0xff);
        }
        else
        {
            Uart_Tx(0x01);

            Data_Type=CheckUART();
            if(Data_Type==1)
            {
                Data_Rd=CheckUART();
                for (j=0; j<NAND_PAGE_SIZE_BYTE; j++)
                {
                    ucPageProgBuf[j] =0x01;
                }
            }
            else
            if(Data_Type==2)
            {
                Count_flag=1;
            }
            bank_addr=(Block_No*64);
            for (i=0; i<NAND_PAGE_COUNT_PER_BLOCK; i++)
            {
                NAND_ProgramPage((bank_addr+i), 0, 2112, ucPageProgBuf);
            }
            Uart_Tx(0x0A);
            Count_flag=0;
        }
    }
    else
    if(Data_Rcv==2)
    {
        bank1=CheckUART();
        bank2=CheckUART();
        Block_No=(bank1 + (bank2 <<8));
        bank_addr=Block_No*64;
    }
}
    
```

Code Explorer

- Defines
- Routines
  - unsigned char CheckUART()
  - void init\_srl(void)
  - void main\_loop(void)
- Variables
  - unsigned char bank1
  - unsigned char bank2
  - unsigned long bank\_addr
  - unsigned int bb[NAND\_BLOCK\_COUNT]
  - unsigned short count
  - uint8\_t i
  - uint8\_t j
  - uint8\_t k
  - uint8\_t rc
  - unsigned char ucPageProgBuf[2112]
  - unsigned char ucPageReadBuf[2112]
  - int NAND\_EraseBlock(unsigned long a\_uiBlockNum)
  - int NAND\_ProgramPage(unsigned long a\_uiPageNum, unsigned short a\_usColNum, unsigned short a\_usRowNum)
  - int NAND\_ReadPage(unsigned long a\_uiPageNum, unsigned short a\_usColNum, unsigned short a\_usRowNum)
  - int NAND\_ReadStatus(void)
  - unsigned char srl\_getchar(void)
  - void srl\_putchar(unsigned char c)
  - void Uart\_Tx(unsigned char ch)
- Variables
  - \_\_NAND volatile uint8\_t Ale\_Offset
  - unsigned long Block\_No
  - \_\_SRLO volatile uint8\_t BRG0
  - \_\_SRLO volatile uint8\_t BRG1
  - \_\_SRLO volatile uint8\_t BRG2
  - \_\_NAND volatile uint8\_t Ce\_Offset
  - \_\_NAND volatile uint8\_t Cle\_Offset
  - unsigned char counter
  - unsigned char Count\_flag
  - unsigned char Data\_Rcv
  - unsigned char Data\_Rd
  - unsigned char Data\_Type
  - \_\_NAND volatile uint8\_t Gpio\_Port
  - \_\_SRLO volatile uint8\_t HSK
  - \_\_SRLO volatile uint8\_t INTCTRL
  - \_\_SRLO volatile uint8\_t INTSTATUS
  - input bool NAND\_RB\_Y\_1
  - input bool NAND\_RB\_Y\_2
  - unsigned char rbuf[RBUF\_SIZE]
  - \_\_NAND volatile uint8\_t Rd\_Dbg\_Offset
  - \_\_NAND volatile uint8\_t Rd\_Offset
  - \_\_SRLO volatile uint8\_t RXDIO
  - \_\_SRLO volatile uint8\_t RXHIGHMARK
  - \_\_SRLO volatile uint8\_t RXLOWMARK
  - unsigned char r\_in
  - unsigned char r\_out
  - \_\_SRLO volatile uint8\_t SBUF
  - \_\_SCRUB volatile uint8\_t SCRUB\_CTL

Files | Projects | Navigator

Output

166: 1 | Insert

System | Design Compiler | Embedded | Instruments | Shortcuts | VHDL | >>

Altium Designer (14.3) - Workgroup [Workspace1.DsnWrk] - Devices - FPGA\_PA3\_CONTROL.PrjFpg. Not signed in.

Devices.FpgaFlow?PortID=VIRTUAL

Virtual Device List

Not Live

Workspace1.DsnWrk Workspace

FPGA\_PA3\_CONTROL.PrjFpg Project

File View Structure Editor

FPGA\_PA3\_CONTROL.PrjFpg

- Source Documents
  - VHDLTestBench1.VHDTST
  - Top.SchDoc
    - nand\_flash\_interface.V
    - nand\_interface\_core.V
    - CLKBUF\_LVDS\_IN.Vhd
    - DECODE.Vhd
    - control.c
- Settings
- Generated (Configuration)

Compile Synthesize Build Program FPGA

ProASIC3E A3PE3000-FG484

FPGA\_PA3\_CONTROL / Configuration

No Soft Devices

Nexus Core Components	Type	Source	Source Location
FPGA_PA3_CONTROL.PrjFpg			E:\prj\FPGA_PA3_CONTROL\

Files Projects Navigator

Messages

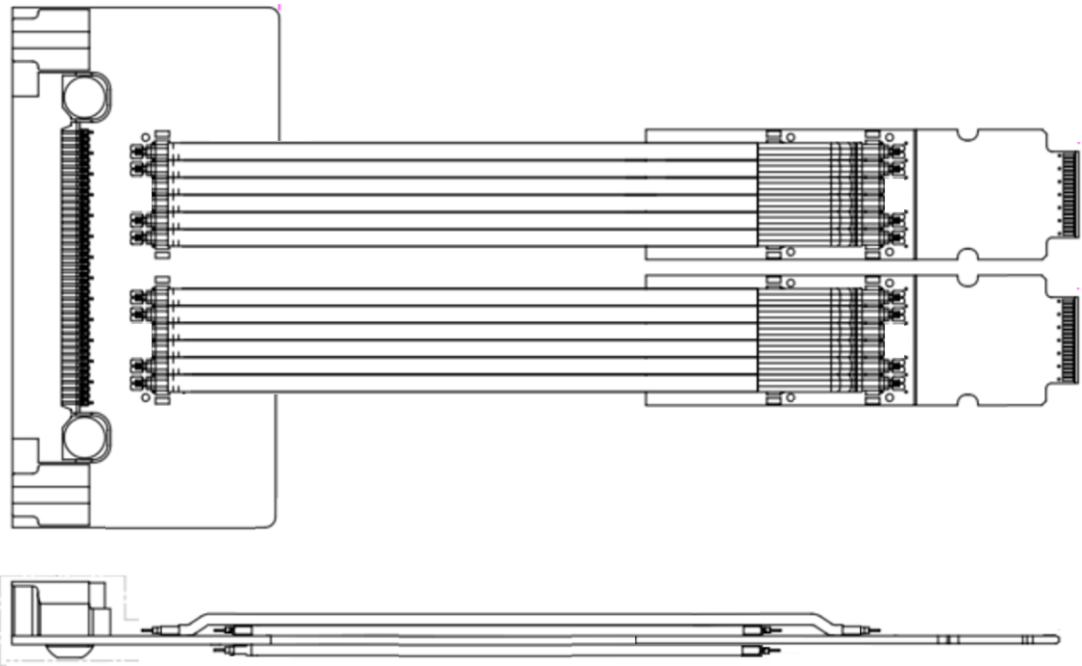
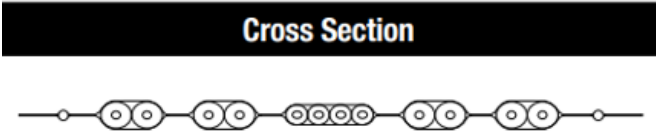
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ProcessFlowInfo	FPGA_PA3_CONTROL.SDF	Timing Analysis	designer - Completed Successfully	05:07:20	03/10/2022	190
ProcessFlowInfo	FPGA_PA3_CONTROL.SDF	Make Bit File	Running designer On E:\prj\FPGA_PA3_CONTROL\ProjectOutputs\Configuration\FPGA_PA3_CONTROL.SDF	05:07:20	03/10/2022	191
ProcessFlowProgress	FPGA_PA3_CONTROL.SDF	Make Bit File	Running E:\Microsemi\Liberio_SoC_v11.8\Designer\bin\designer.Exe...	05:07:20	03/10/2022	192
ProcessFlowInfo	FPGA_PA3_CONTROL.SDF	Make Bit File	Info: The design FPGA_PA3_CONTROL.ADB was last modified by software version 11.8.0.26.	05:07:24	03/10/2022	193
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ProcessFlowInfo	FPGA_PA3_CONTROL.SDF	Make Bit File	designer - Completed Successfully	05:08:07	03/10/2022	195

System Design Compiler Instruments Shortcuts VHDL >>

Part Number	Plating	Typical application	Drawing
SL8801/12-10DA5-00 SL8801/12-11DA5-00	Silver Tin	MiniSAS SFF 8087 with sidebands	78-5100-2412-4

Tree different length of prototype cables base on the 3M cable SL8801/12-11DA5, will be constructed and tested.

3M Twinax Cable .



The current status of the cable is as follows.

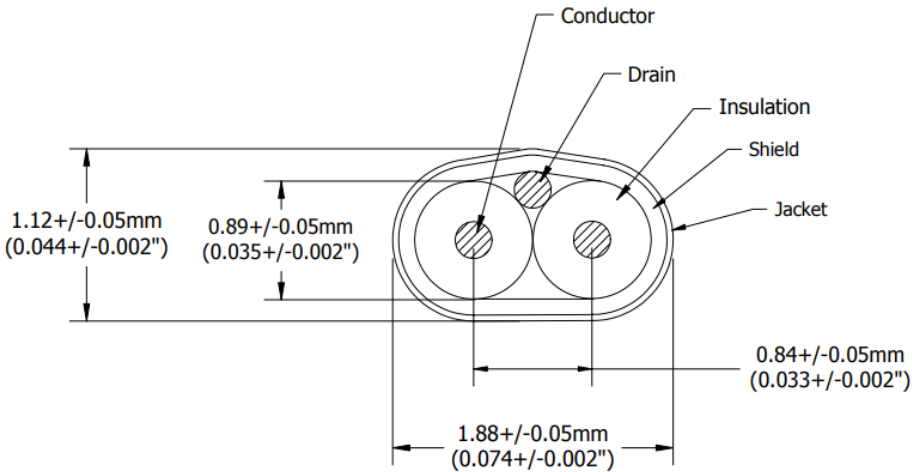
- 1. 3M cable SL8801/12-11DA5-00 - we need more than 60 rolls in total. Right now only 30 rolls are in the stocks. We asked for 3 rolls only at the moment.



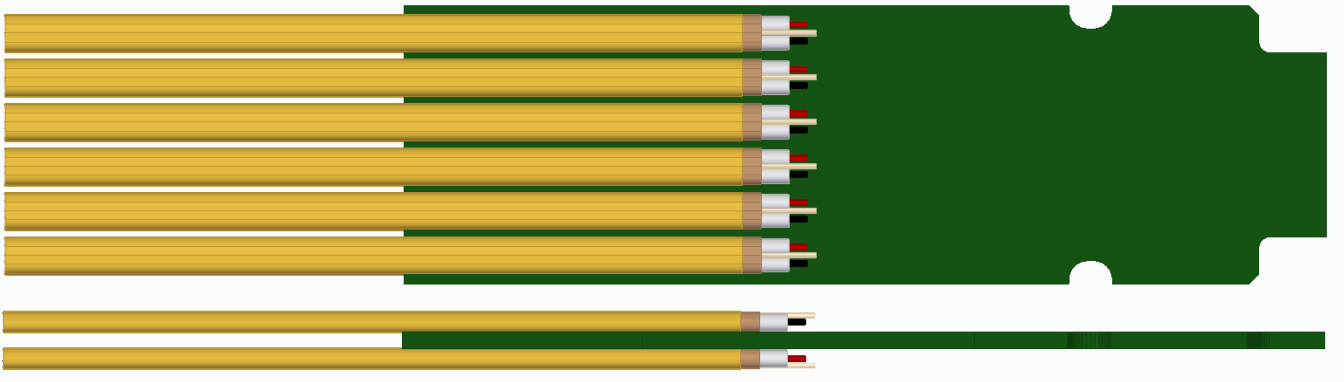
Temp-Flex TwinMax High-Temperature, Low-Loss Twinax Cable .



TITLE	PART No.	REV	PAGE
Shielded Pair 30 AWG, 100 Ohm Twinax	1000680107	C	1 of 1



Construction:  
Conductor: 30 AWG, 0.27mm (0.0107") Solid SPC.  
Insulation: Fluoropolymer  
Drain Wire: 30 AWG, 0.25mm (0.010") Solid SPC.  
Shield: Aluminum / Polyester Foil, 0.023mm (0.0009") Thickness Ref.  
Jacket: Polyester, Heat Sealed, 0.08mm (0.0007") Thickness Ref.  
Safety Compliance: AWM STYLE 22058



4 unit per stave.

We have to check the actual availability, we need around 20,2 Km for 42 stave.  
Molex produce roles of 60m.

# Backup

00009045	<b>DATA SHEET</b>	
Valid from: 23.05.2022	<b>EPIC® SIGNAL R 3.0 D PG 16</b>	

**Description**

- Circular connectors with solder termination
- 21-pin and 26-pin
- highest contact density at small space requirements
- Connector in solder version for easy maintenance

**General Characteristics**

Series	SIGNAL R 3.0 D
Number of contacts	21-pin / 26-pin
Pin configuration	Male E-part / Female P-part
Coding	N
Rated voltage (V)	24V AC / 60VDC
Rated impulse voltage	1,5 kV
Rated current (A)	7,5 A
Contact resistance	< 3 mOhm
Contacts	Copper alloy, gold plated
Termination methods	Solder termination: up to 1.0 mm²
Cable clamping range	6,5-16
Protection	IP 67 (maximum, dependant on cable gland used)
Cycle of mechanical operation	500
Temperature range	-40°C to +100°C, short-term up to +125°C



00009371	<b>DATA SHEET</b>	
Valid from: 23.05.2022	<b>EPIC® SIGNAL R 3.0 G1</b>	

**Description**

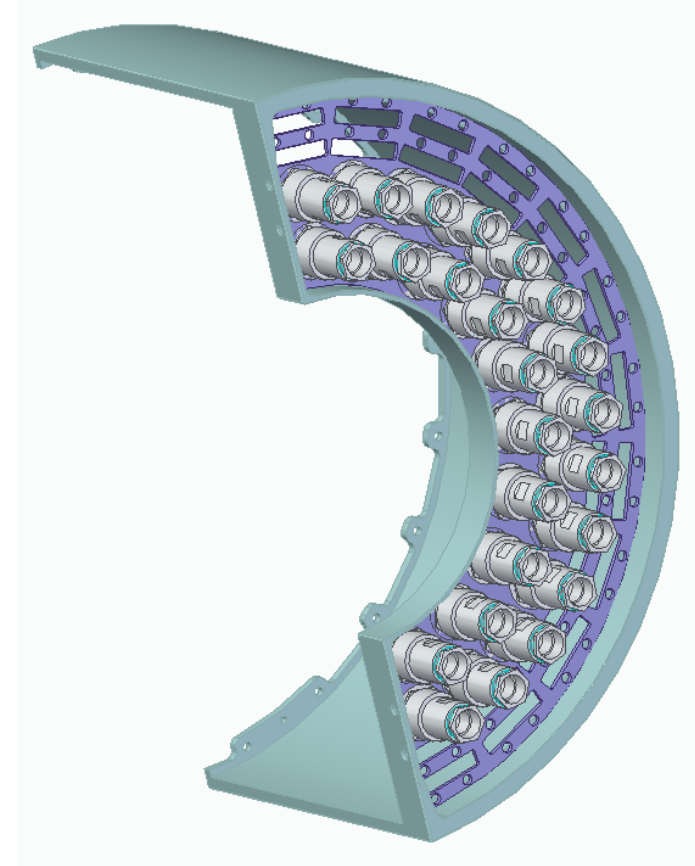
- Circular connectors with solder termination
- 21-pin and 26-pin
- highest contact density at small space requirements
- Connector in solder version for easy maintenance

**General Characteristics**

Series	SIGNAL R 3.0 G1
Number of contacts	21-pin / 26-pin
Pin configuration	Male E-part / Female P-part
Coding	N
Rated voltage (V)	24V AC / 60VDC
Rated impulse voltage	1,5 kV
Rated current (A)	7,5 A
Contact resistance	< 3 mOhm
Contacts	Copper alloy, gold plated
Termination methods	Solder termination: up to 1.0 mm²
Fastening type	Ø25mm (1x)
Protection	IP 67 (maximum, dependant on cable gland used)
Cycle of mechanical operation	500
Temperature range	-40°C to +100°C, short-term up to +125°C



Arranging the data and power connector in the patch panel is possible supply power to 48 staves



If the data connector is rearranged to the lateral surface it is possible to increase the number of power connectors

## REVISION

0	RS	J LAMBERT
12/5/2017	ECN-315019	ISSUE FOR REVIEW
1	RS	J LAMBERT
2/9/2018	ECN-319537	BOM: ADD PCB-109007 AND PCB-109008 DETAILS; TB2: UPDATE PINOUT; RELEASE FOR LIMITED PRODUCTION
2	RS	J LAMBERT
6/14/2018	ECN-329975	TABULATE CABLE LENGTH AND ADD CONFIGS: -01 (6000MM), -02 (4300MM), -03 (4800MM), -04 (5300MM) CONFIGS
3	RS	J LAMBERT
9/10/2018	ECN-336361	UPDATE NOTE 6, LINE 3 TO: LINE 3 - DATE CODE SERIAL NUMBER "XXXX-SSS" WHERE "XXXX" IS DATE CODE & "SSS" IS UNIQUE SEQUENTIAL NUMBER FOR ASSEMBLY IN THE SHOP ORDER IE. 001, 002, 003... "SSS" RESETS EACH SHOP ORDER

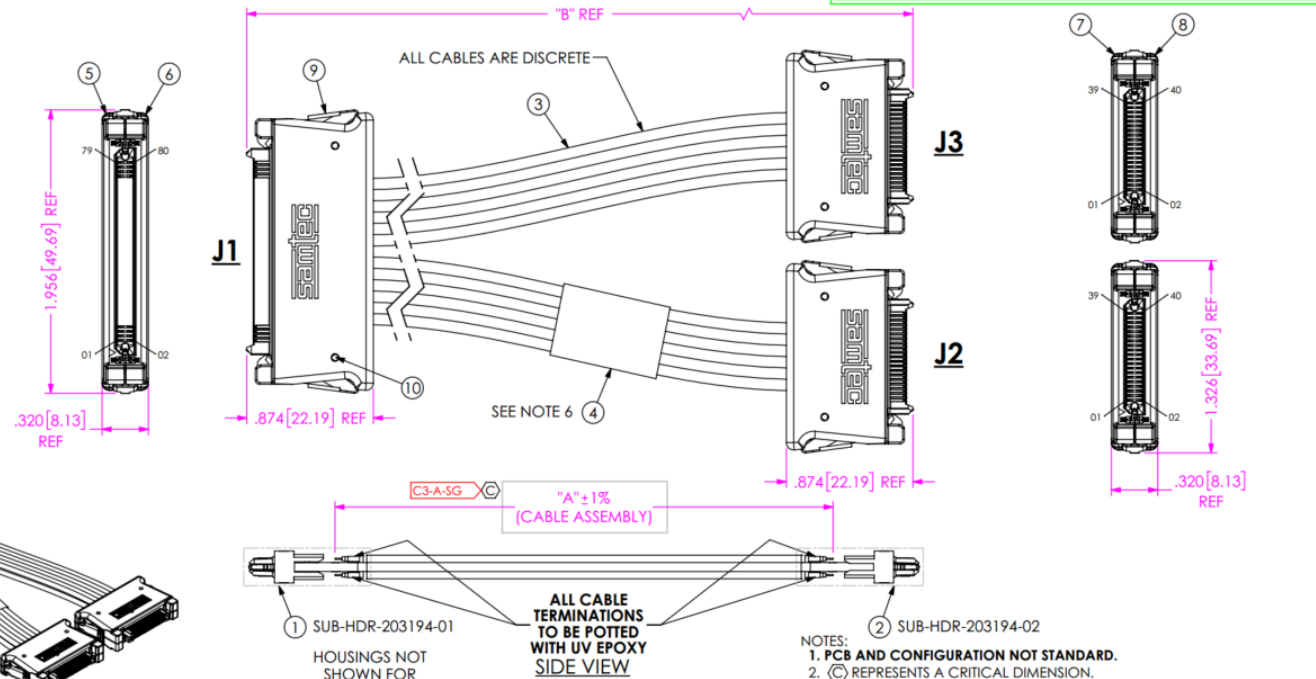
RELEASED FOR  
LIMITED PRODUCTIONUSE FOR QUOTING, PRELIMINARY  
DESIGN, INITIAL BUILDS AND  
INFORMATIONAL PURPOSES ONLY

TABLE 1		
PART #	"A"	"B"
HDR-203194-01	236.22 [6,000.0]	237.42 [6,030.5]
HDR-203194-02	169.29 [4,300.0]	170.49 [4,330.4]
HDR-203194-03	188.98 [4,800.0]	190.18 [4,830.4]
HDR-203194-04	208.66 [5,300.0]	209.86 [5,330.4]

HDR-203194-XX BOM

ITEM NO.	PART NUMBER	DESCRIPTION	QTY	MATERIAL
1	SUB-HDR-203194-01	SUB ASSEMBLY	1	SUB ASSEMBLY
2	SUB-HDR-203194-02	SUB ASSEMBLY	2	SUB ASSEMBLY
3	SUB-CCS-183564-06-03-TB-236.22	TWINAX CABLE	4	SUB ASSEMBLY
4	HDR-11	LABEL	1	SELF LAMINATING VINYL
5	ERH-40-03-T	HOUSING	1	IDEMITSU XAREC EA 522 BK, COLOR: BLACK
6	ERH-40-03-B	HOUSING	1	IDEMITSU XAREC EA 522 BK, COLOR: BLACK
7	ERH-20-03-B	HOUSING	2	IDEMITSU XAREC EA 522 BK, COLOR: BLACK
8	ERH-20-03-T	HOUSING	2	IDEMITSU XAREC EA 522 BK, COLOR: BLACK
9	LTC-16-01	LATCH	6	STAINLESS STEEL
10	STS-04	FASTENER	6	LOW CARBON STEEL

TOLERANCES DO NOT APPLY TO REFERENCE DIMENSIONS, UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES ARE:

DECIMALS: .XX ± .01 [3]

ANGLES: 2° ± .005 [13]

XXXX: ± .0020 [051]

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**samtec**

520 PARK EAST BLVD, NEW ALBANY, IN 47150  
PHONE: 812-944-6733 FAX: 812-948-5047  
e-Mail: info@SAMTEC.com code 55322

DO NOT SCALE DRAWING SHEET SCALE: 1:2

DESCRIPTION:  
CUSTOM HDR CABLE ASSEMBLYDWG. NO.  
HDR-203194-XX

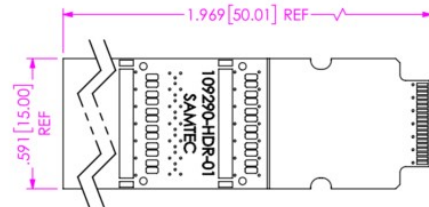
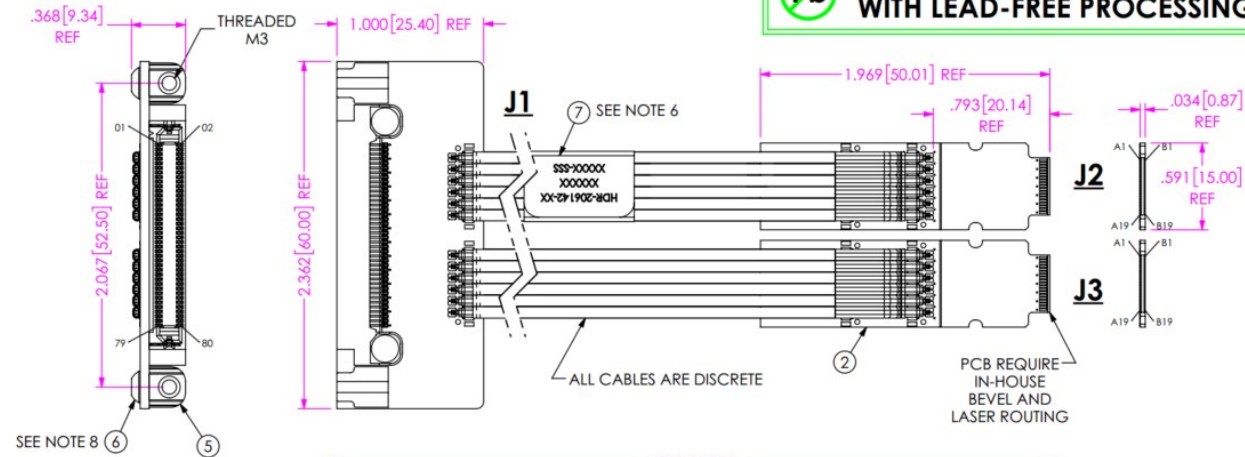
BY: RSANTOS 12/05/2017 SHEET 1 OF 2

## REVISION

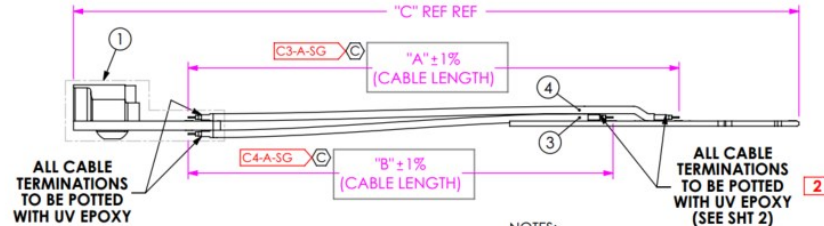
0	RS	J LAMBERT
5/21/2018	ECN-328302	ISSUE FOR REVIEW
1	RS	J LAMBERT
5/22/2018	ECN-330519	ADD EPOXY KEEP OUT AT 19MM
2	RS	J LAMBERT
9/10/2018	ECN-336359	UPDATE NOTE 6 TO INCLUDE LINE 3 - DATE CODE SERIAL NUMBER "XXXX-SSS" WHERE "XXXX" IS DATE CODE & "SSS" IS UNIQUE SEQUENTIAL NUMBER FOR ASSEMBLY IN THE SHOP ORDER I.E. 001, 002, 003... "SSS" RESETS EACH SHOP ORDER ADD EPOXY APPLICATION VIEW TO SHEET 2, ADD CRITICAL CS TO KEEP OUT, AND CS CRITICAL TO TABLE 3

RELEASED FOR LIMITED PRODUCTION

USE FOR QUOTING, PRELIMINARY DESIGN, INITIAL BUILDS AND INFORMATIONAL PURPOSES ONLY



S-PCB-109290-HDR-01 VIEW



## NOTES:

1. PCB AND CONFIGURATION IS NOT STANDARD.
2. (C) REPRESENTS A CRITICAL DIMENSION
3. PARTS TO BE PROCESSED PER SAMTEC WORKMANSHIP GUIDELINES
4. ALL ASSEMBLIES TO BE 100% ELECTRICALLY TESTED
5. ALL ASSEMBLIES TO BE 100% HI-POT TESTED AT 300V
6. ITEM 7 TO BE CENTERED ON ITEM 4 AS SHOWN ITEM 7 TO CONTAIN:  
LINE 1 - PART NUMBER "HDR-XXXXXX-XX"  
LINE 2 - SHOP ORDER NUMBER "XXXXXX"  
LINE 3 - DATE CODE SERIAL NUMBER "XXXX-SSS" WHERE "XXXX" IS DATE CODE & "SSS" IS UNIQUE SEQUENTIAL NUMBER FOR ASSEMBLY IN THE SHOP ORDER I.E. 001, 002, 003... "SSS" RESETS EACH SHOP ORDER
7. FOR SUB-ASSEMBLY AND FINISHED GOOD PACKAGING REQUIREMENTS, REFERENCE SAMTEC PACKAGING STANDARD
8. TIGHTEN FASTENERS TO 1.4-1.7 IN-LBS (2 PLCS)
9. PANEL PCB-109006-HDR-XX YIELDS (8) PCB-109006-HDR-01 BOARDS
10. PANEL PCB-109290-HDR-XX YIELDS (14) PCB-109290-HDR-01 BOARDS

TABLE 1			
PART #	"A"	"B"	"C"
HDR-206142-01	91.57 [2,326.0]	89.95 [2,284.7]	93.11 [2,364.9]
HDR-206142-02	84.65 [2,150.0]	83.02 [2,108.8]	86.18 [2,189.0]
HDR-206142-03	96.46 [2,450.0]	94.83 [2,408.8]	97.99 [2,489.0]
HDR-206142-04	104.33 [2,650.0]	102.71 [2,608.8]	105.87 [2,689.0]

HDR-206142-XX BOM				
ITEM NO.	PART NUMBER	DESCRIPTION	QUANTITY	MATERIAL
1	SUB-HDR-206142-01	SUB ASSEMBLY	1	SUB ASSEMBLY
2	S-PCB-109290-HDR-01	SUB ASSEMBLY	2	SUB ASSEMBLY
3	SUB-CCS-183564-06-03-TB-XX-XX	TWINAX, 32A WG	2	SUB ASSEMBLY
4	SUB-CCS-183564-06-03-TB-XX-XX	TWINAX, 32A WG	2	SUB ASSEMBLY
5	CCS-204400-01-MP	ANCHOR BLOCK	2	BRA SS
6	90910A783	SHCS	2	STAINLESS STEEL
7	HDRL-11	LABEL	1	SELF LAMINATING VINYL

F:\dwg\hdr\206000\hdr-206142-xx\HDR-206142-XX.SLDDRW

TOLERANCES DO NOT APPLY TO REFERENCE DIMENSIONS, UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES ARE:

DECIMALS ANGLES

XX ± .01 [3]

XXX ± .005 [13]

XXXX ± .0020 [051]

DO NOT SCALE DRAWING

SHEET SCALE: 1:2

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520 PARK EAST BLVD, NEW ALBANY, IN 47150  
PHONE: 812-944-6733 FAX: 812-948-5047  
e-Mail info@SAMTEC.com code 55322

DESCRIPTION: CUSTOM HDR CABLE ASSEMBLY

DWG. NO. HDR-206142-XX

BY: RMSANTOS 05/21/2018 SHEET 1 OF 2